Am93L24

Low-Power Five–Bit Comparator

Distinctive Characteristics

- 38 ns typical compare time.
- 32 mw typical power dissipation.
- 100% reliability assurance testing in compliance with MIL STD 883

FUNCTIONAL DESCRIPTION

The Am93L24 is a high-speed expandable comparator which compares two 5-bit words, A and B, and gives outputs of "A greater than B," "A equal to B" and "A less than B." An active LOW enable is provided which forces the three outputs LOW when the enable goes HIGH.

Comparators can be connected in series or parallel to obtain comparison over large word lengths. For series connection the A > B and A < B outputs are connected to the least significant A_0 and B_0 inputs of the next most significant comparator. Parallel connection uses the same number of devices as the series method and is considerably faster when comparing over large word lengths. Parallel connection is accomplished by comparing the A > B, A < B outputs of several comparators by additional comparators.

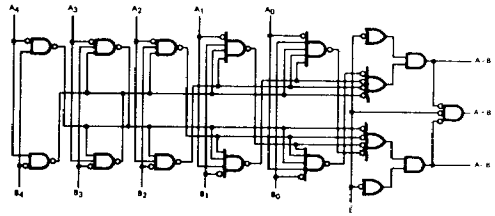
TRUTH TABLE

Inputs		Outputs		
Data	$\bar{E}$	A > B	A = B	A < B
X	H	L	L	L
A > B	L	H	L	L
A = B	L	L	H	L
A < B	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Table I

LOGIC DIAGRAM



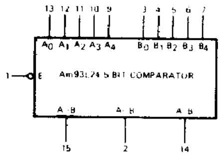
LOADING RULES
In Unit Loads (Notes)

Input Load Factor	TTL LOADS HIGH	TTL LOADS LOW	93L LOADS HIGH	93L LOADS LOW
All inputs	1.0	0.5	2.0	2.0
Output Drive	**HIGH**	**LOW**	**HIGH**	**LOW**
A > B, A < B	10	3	20	12
A = B	9	3	18	12

NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

PC
DC
DM
FM

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Am93L24 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
16-Pin Molded DIP	0°C to +75°C	U6M93L2459X
16-Pin Hermetic DIP	0°C to +75°C	U7B93L2459X
16-Pin Hermetic DIP	−55°C to +125°C	U7B93L2451X
16-Pin Hermetic Flat Pak	−55°C to +125°C	U4L93L2451X
Dice	Note	UXX93L24XXD

Part No chg in sec 9.

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL C TERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L2459X $T_A = 0°C$ C $V_{CC} = 4.75$ V to 5.25 V
Am93L2451X $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.50$ V to 5.50 V

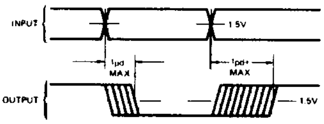
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -0.4$ mA $V_{IN} = V_{IH}$ or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $I_{OL} = 4.92$ mA $V_{IN} = V_{IH}$ or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.3$ V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.4$ V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5$ V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., $V_{OUT} = 0.0$ V	−2.5		−25	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		10.4	21	mA

Notes: 1) Typical limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

Parameters		Description		Test Conditions	Min	Typ	Max	Units
t_{pd+} ($\bar{E}$-A = B)		Turn Off Delay	Enable Input to A = B Output	$V_{CC} = 5.0$ V, $C_L = 15$ pF	10	21	32	ns
t_{pd-} ($\bar{E}$-A = B)		Turn On Delay	Enable Input to A = B Output		15	30	45	ns
t_{pd+} ($\bar{E}$-A ≠ B)		Turn Off Delay	Enable to A < B and A > B	$V_{CC} = 5.0$ V, $C_L = 15$ pF	15	20	30	ns
t_{pd-} ($\bar{E}$-A ≠ B)		Turn On Delay	Enable to A < B and A > B		12	24	36	ns
t_{pd+} (A_2-A>B)		Turn Off Delay	A_2 Input to A > B Output	$V_{CC} = 5.0$ V, $C_L = 15$ pF	18	36	54	ns
t_{pd-} (A_2-A>B)		Turn On Delay	A_2 Input to A > B Output		22	43	65	ns
t_{pd+} (A_2-A<B)		Turn Off Delay	A_2 Input to A < B Output	$V_{CC} = 5.0$ V, $C_L = 15$ pF	22	44	66	ns
t_{pd-} (A_2-A<B)		Turn On Delay	A_2 Input to A < B Output		25	49	74	ns
t_{pd+} (A_2-A=B)		Turn Off Delay	A_2 Input to A = B Output	$V_{CC} = 5.0$ V, $C_L = 15$ pF	34	68	102	ns
t_{pd-} (A_2-A=B)		Turn On Delay	A_2 Input to A = B Output		26	51	76	ns
t_{pd+}	(A_4 or B_4)	Turn Off Delay	Any Input to A<B Output	Worst case maximum propagation delay.	23	45	67	ns
t_{pd-}	to A < B	Turn On Delay	Any Input to A<B Output		34	67	90	ns
t_{pd+}	(A_4 or B_4)	Turn Off Delay	Any Input to A>B Output		27	54	80	ns
t_{pd-}	to A > B	Turn On Delay	Any Input to A>B Output		28	56	84	ns

SWITCHING TIME WAVEFORMS



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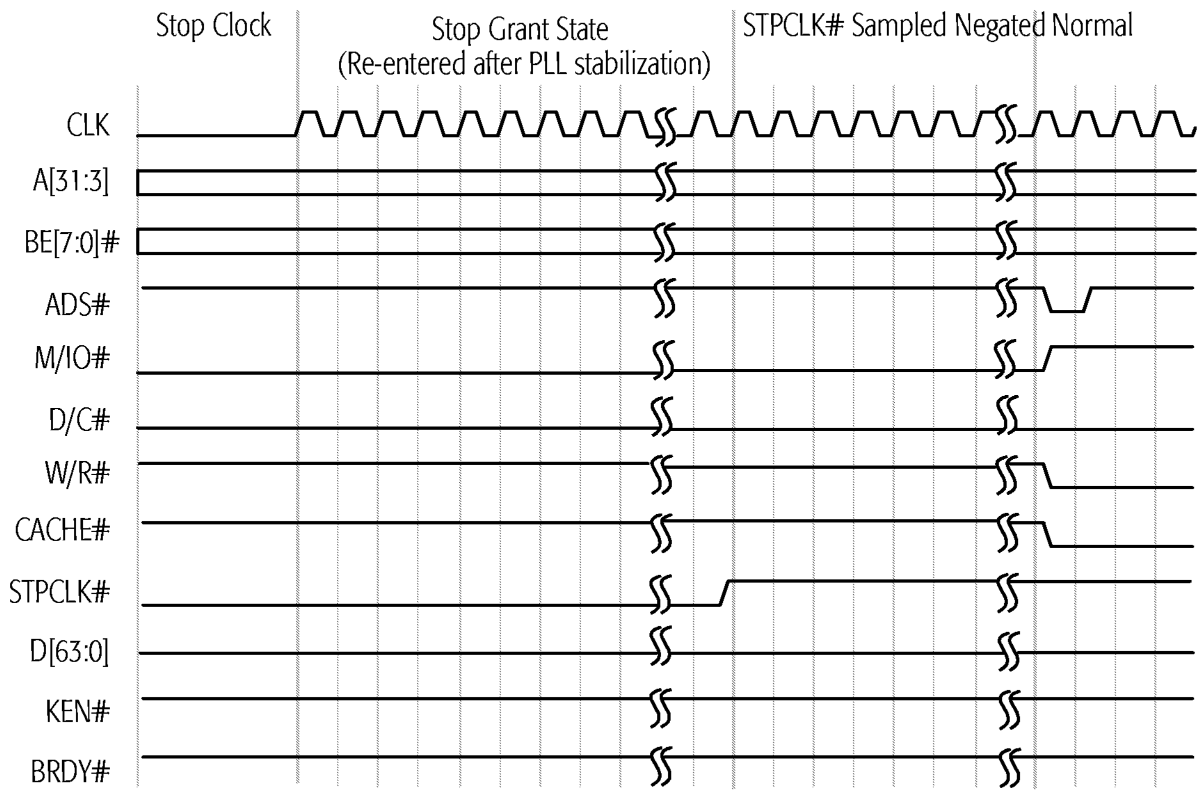

Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

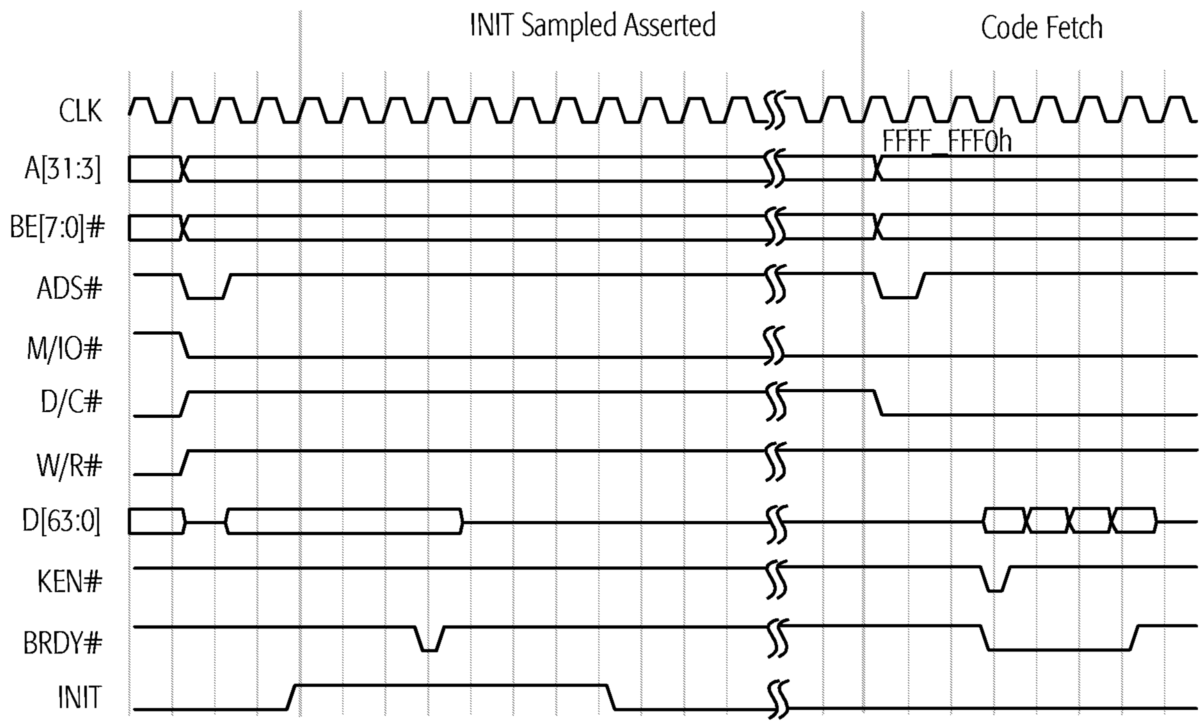

Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See “CLK Switching Characteristics” on page 255 for clock specifications. See “Electrical Data” on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.