Freescale Semiconductor
Technical Data

Document Number: MC100ES8011P
Rev 2, 09/2005

Low Voltage 1:2 Differential PECL-to-HSTL Clock Fanout Buffer

The MC100ES8011P is a low voltage 1:2 Differential PECL-to-HSTL clock fanout buffer. Designed for the most demanding clock distribution systems, the MC100ES8011P supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are in high performance clock distribution in computing, networking and telecommunication systems.

Features

- 1:2 differential clock fanout buffer
- 20 ps maximum device skew
- SiGe Technology
- Supports DC to 625 MHz operation
- HSTL compatible differential clock outputs
- PECL compatible differential clock inputs
- 3.3V power supply
- Supports industrial temperature range
- Standard 8 lead SOIC package
- 8-lead Pb-free package available

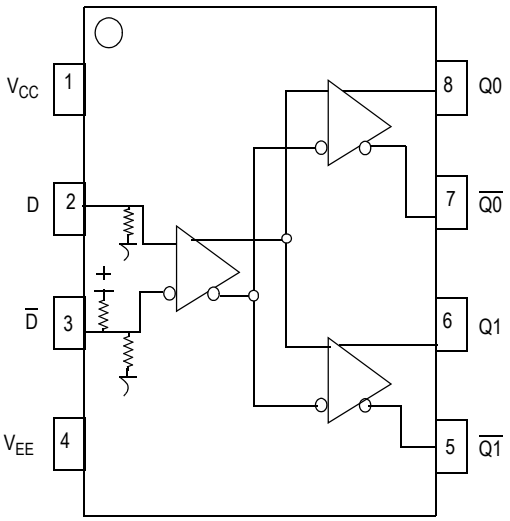


Figure 1. 8-Lead Pinout (Top View) **and Logic Diagram**

MC100ES8011P

1:2 DIFFERENTIAL PECL TO HSTL CLOCK FANOUT DRIVER

D SUFFIX
8-LEAD SOIC PACKAGE
CASE 751-07

EF SUFFIX
8-LEAD SOIC PACKAGE
Pb-FREE PACKAGE
CASE 751-07

ORDERING INFORMATION	
Device	**Package**
MC100ES8011PD	SO-8
MC100ES8011PDR2	SO-8
MC100ES8011PEF	SO-8 (Pb-Free)
MC100ES8011PEFR2	SO-8 (Pb-Free)

PIN DESCRIPTION	
Pin	**Function**
D, $\overline{D}$	ECL Data Inputs
Qn, $\overline{Qn}$	LVDS Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

Table 1. Absolute Maximum Ratings[1]

Symbol	Parameter	Conditions	Rating	Unit
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6V$	V_{CC} + 0.3 V_{EE} – 0.3	V V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 2. DC Characteristics (V_{CC} = 3.3 V ± 5%; T_J = 0°C to 110°C)[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
PECL differential input signals (D, $\overline{D}$)						
V_{PP}	Differential Input Voltage[2]	0.15		1.0	V	Differential Operation
V_{CMR}	Differential Cross Point Voltage[3]	1.0		V_{CC} – 0.6	V	Differential Operation
I_{IN}	Input Current			±150	mA	V_{IN} = V_{IH} or V_{IN}
HSTL clock outputs (Q[0:1], $\overline{Q[0:1]}$)						
$V_{X, OUT}$	Output Differential Crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1			V	
V_{OL}	Ouput Low Voltage			0.4	V	
Supply Current						
I_{CC}	Maximum Quiescent Supply Current without output termination current		80	105	mA	V_{CC} pin (core)

1. DC characteristics are design targets and pending characterization.
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 3. AC Characteristics (V_{CC} = 3.3 V ± 5%; T_J = 0°C to 110°C)[1] [2]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
PECL differential input signals (D, $\overline{D}$)						
V_{PP}	Differential Input Voltage (peak-to-peak)[3]	0.2		1.0	V	
V_{CMR}	Differential Cross Point Voltage[4]	1		V_{CC} – 0.6	V	
f_{CLK}	Input Frequency			625	MHz	Differential
t_{PD}	Propagation Delay D to Q[0:1]	600	760	940	ps	Differential
HSTL clock outputs (Q[0:1], $\overline{Q[0:1]}$)						
$V_{X, OUT}$	Output Differential Crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1			V	
V_{OL}	Ouput Low Voltage			0.5	V	
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak)	0.5			V	
$t_{SK(O)}$	Output-to-Output Skew			20	ps	Differential
$t_{SK(PP)}$	Output-to-Output Skew (part-to-part)			340	ps	Differential
$t_{SK(P)}$	Output Pulse Skew			75	ps	
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter			1	ps	
t_r / t_f	Output Rise/Fall Times	150		800	ps	20% to 80%

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
3. V_{PP} (AC) is the minimum differential PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
4. V_{CMR} (AC) is the crosspoint of the differential PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP}(AC) impacts the device propagation delay, device and part-to-part skew.

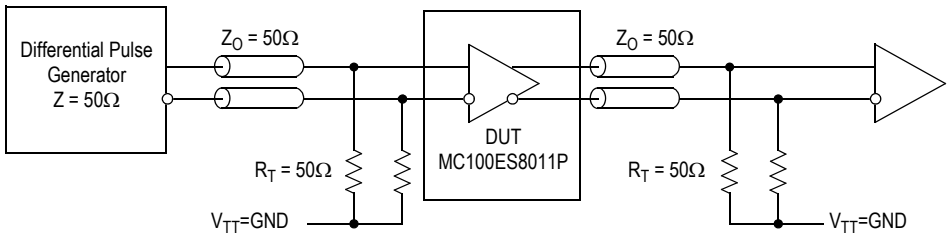


Figure 2. MC100ES8011P AC Test Reference

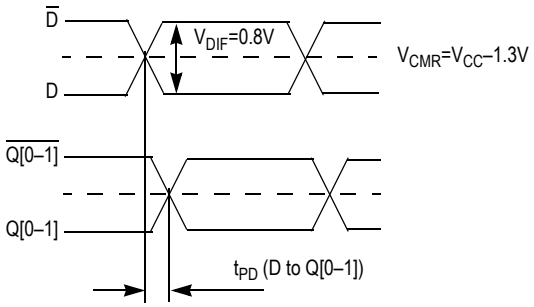
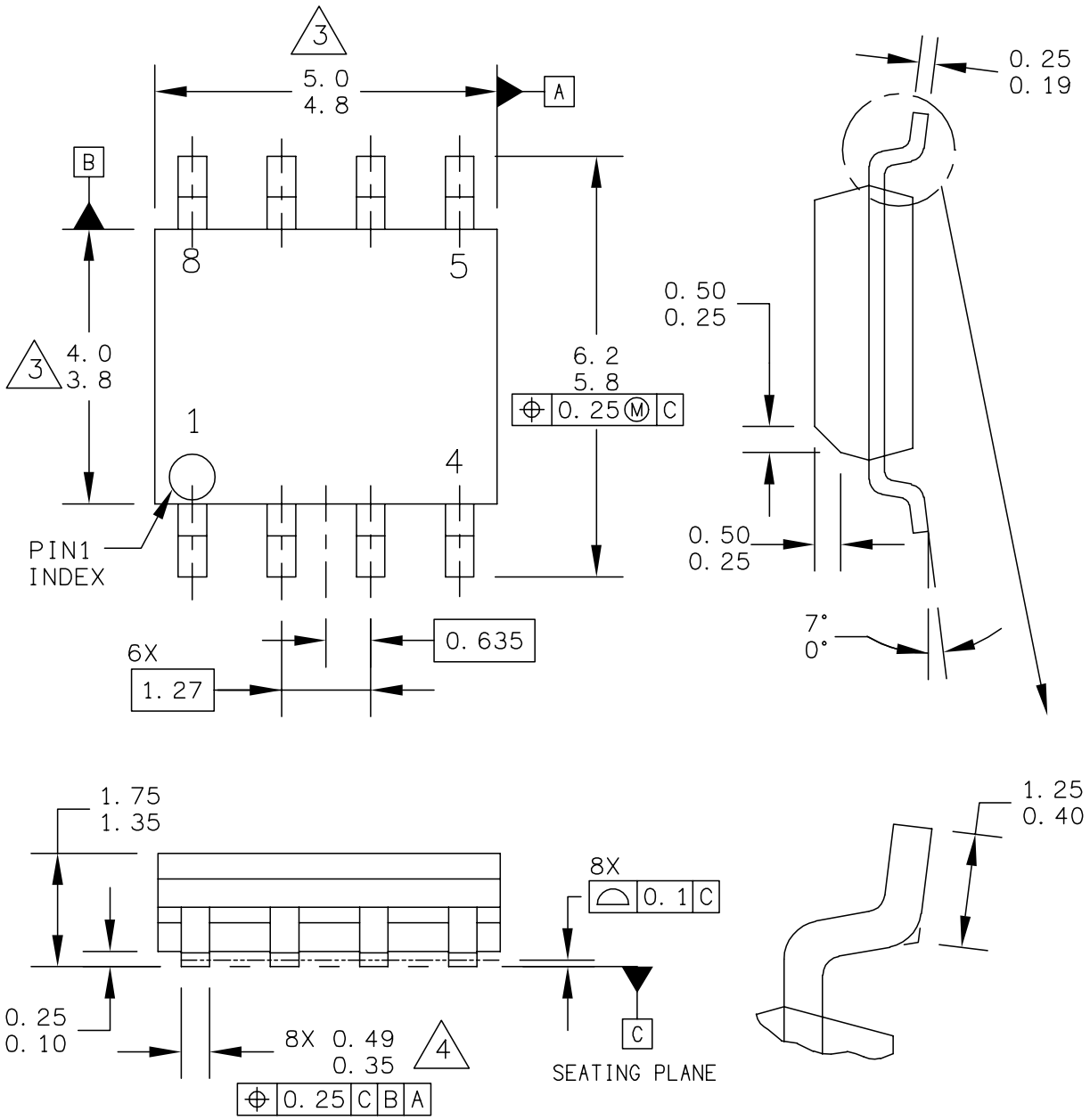


Figure 3. MC100ES8011P AC Reference Measurement Waveform (PECL Input)

PACKAGE DIMENSIONS



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	CASE NUMBER: 751-07	07 APR 2005
	STANDARD: JEDEC MS-012AA	

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CASE 751-07
ISSUE U
8-LEAD SOIC PACKAGE

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

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8-LEAD SOIC PACKAGE

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