

SLIC
Subscriber Line Interface Circuit

HC-5502A

T-75-11-17

Features

- Monolithic Integrated Device
- DI High Voltage Process
- Compatible With Worldwide PBX Performance Requirements
- Controlled Supply of Battery Feed Current for Short Loops (30mA)
- Internal Ring Relay Driver
- Low Power Consumption During Standby
- Switch Hook, Ground Key and Ring Trip Detection Functions
- Selective Denial of Power to Subscriber Loops

Applications

- Solid State Line Interface Circuit for Analog and Digital PBX Systems
- Direct Inward Dial (DID) Trunks
- Voice Messaging PBX's

Description

The Harris SLIC incorporates many of the BORSHT function on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents. Using the unique Harris dielectric isolation process, the SLIC can operate directly with a wide range of station battery voltages.

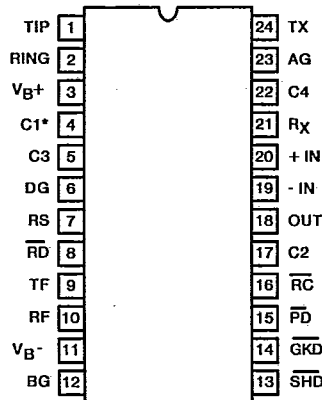
The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

The Harris SLIC is ideally suited for the design of new digital PBX systems, by eliminating bulky hybrid transformers.

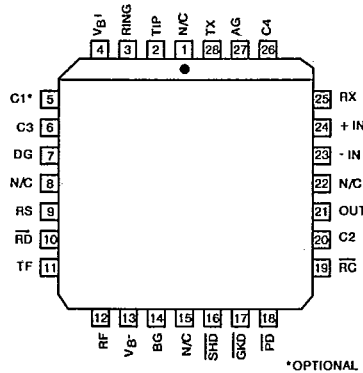
SLIC is available in either a 24 pin Dual-in-Line Plastic or Ceramic package, and a 28 pin PLCC package. The SLIC is also available as unpackaged die.

Pinouts

HC-5502A
 (CERAMIC/PLASTIC DIP)
 TOP VIEW



HC4P5502A
 (PLCC)
 TOP VIEW

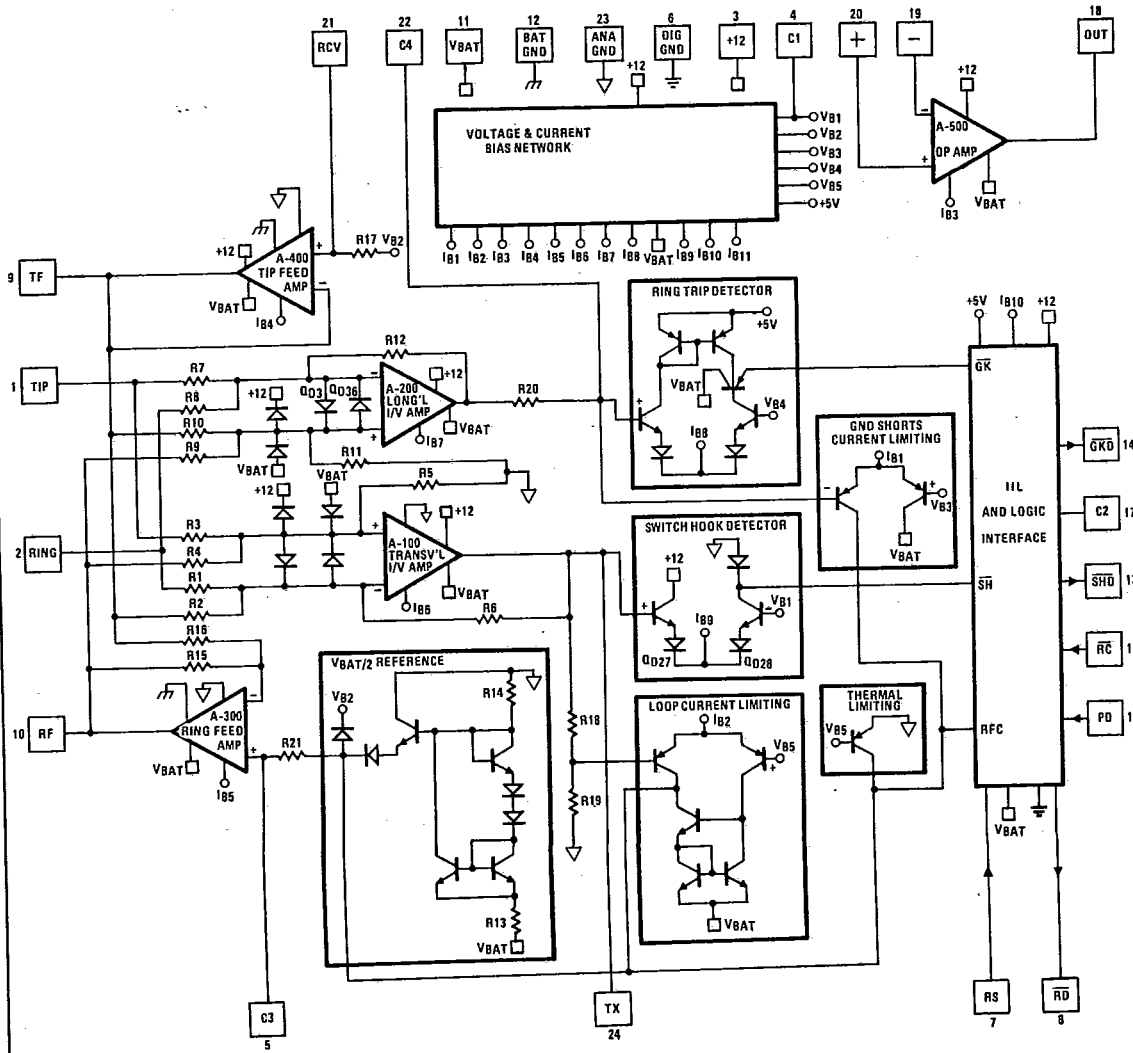


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CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

T-75-11-17.

Schematic



HC-5502A SLIC FUNCTIONAL SCHEMATIC.

Die Characteristics

Transistor Count	181	
Diode Count	27	
Die Dimensions	169 x 112	
Substrate Potential	Unconnected	
Process	Bipolar-DI	
Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	51	16
Plastic DIP	52	24

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HC-5502A

Absolute Maximum Ratings (Note 1)

Maximum Continuous Supply Voltages (V_{B-}) -60 to +0.5 V
 (V_{B+}) -0.5 to +15 V
 (V_{B+} - V_{B-}) 75V
 Relay Drive Voltage (V_{RD}) -0.5 to +15V
 Storage Temperature Range -65°C to +150°C
 Junction Temperature +175°C

Recommended Operating Conditions

Relay Driver Voltage (V_{RD}) +5 to +12V
 Positive Supply Voltage (V_{B+}) 10.8 to 13.2V
 Negative Supply Voltage (V_{B-}) -42 to -58V
 Minimum High Level Logic Input Voltage 2.4V
 Maximum Low Level Logic Input Voltage 0.6V
 Loop Resistance (R_L) 200 to 1200 Ohms
 Operating Temperature Range
 HC-5502A-5,-7 0°C to +75°C
 HC-5502A-9 -40°C to +85°C

Electrical Specifications

V_{B-} = -48V, V_{B+} = +12V, AG = BG = DG = 0V, Unless Otherwise Noted,
 Typical Parameters +25°C. Min-Max Parameters are Over Operating Temperature Range.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation	I _{Long} = 0	-	135	174	mW
Off Hook Power Dissipation	R _{LINE} = 600 Ohms, I _{Long} = 0	-	450	580	mW
Off Hook IB+	R _{LINE} = 600 Ohms, I _{Long} = 0 @ -40°C	-	-	5.0	mA
Off Hook IB+	R _{LINE} = 600 Ohms, I _{Long} = 0 @ +25°C	-	-	4.3	mA
Off Hook IB-	R _{LINE} = 600 Ohms, I _{Long} = 0	-	-	38	mA
Off Hook Loop Current	R _{LINE} = 1200 Ohms, I _{Long} = 0	-	21	-	mA
Off Hook Loop Current	R _{LINE} = 1200 Ohms, V _{B-} = -42V, I _{Long} = 0 T _A = 25°C	17.5	-	-	mA
Off Hook Loop Current	R _{LINE} = 200 Ohms, I _{Long} = 0	25.5	30	34.5	mA
Fault Currents					
TIP to Ground		-	14	-	mA
RING to Ground		-	47	-	mA
TIP to RING		-	30	-	mA
TIP and RING to Ground		-	47	-	mA
Ring Relay Drive V _{OL}	I _{OL} = 62mA	-	0.2	0.5	V
Ring Relay Driver Off Leakage	V _{RD} = +12V, RC = 1 = HIGH, T _A = 25°C	-	-	100	µA
Ring Rip Detection Period	R _{LINE} = 600 Ohms, T _A = +25°C	-	2	3	Ring Cycles
Switch Hook Detection Threshold	$\overline{SHD} = V_{OL}$	10	-	-	mA
	$\overline{SHD} = V_{OH}$	-	-	5	mA
Ground Key Detection Threshold	$\overline{GKD} = V_{OL}$	20	-	-	mA
	$\overline{GKD} = V_{OH}$	-	-	10	-
Loop Current During Power Denial		-	±2	-	mA
Dial Pulse Distortion		0	-	5	ms
Receive Input Impedance		-	90	-	kOhms
Transmit Output Impedance		-	5	20	Ohms
Two Wire Return Loss	(Return Loss Referenced to 600Ω +2.16µF)	-	15.5	-	dB
SRL LO		-	24	-	dB
ERL		-	31	-	dB
SRL HI		-	-	-	dB
Longitudinal Balance	1V Peak-Peak 200Hz - 3400Hz 0°C ≤ T _A ≤ 75°C	58	65	-	dB
2 Wire Off Hook		60	63	-	dB
2 Wire On Hook		50	58	-	dB
4 Wire Off Hook		-	-	23	dBmC
Low Frequency Longitudinal Balance	R.E.A. Method, 0°C ≤ T _A ≤ 75°C	-	-	-67	dBmOp

NOTES: 1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

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Electrical Specifications (Continued)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss	@1kHz, OdBm Input Level	-	±0.05	±0.2	dB
2 Wire - 4 Wire		-	±0.05	±0.2	dB
4 Wire - 2 Wire		-	±0.02	±0.05	dB
Frequency Response	200 - 3400Hz Referenced to Absolute Loss at 1kHz and OdBm Signal Level				dB
Idle Channel Noise	0°C ≤ T _A ≤ 75°C	-			
2 Wire - 4 Wire	0°C ≤ T _A ≤ 75°C	-	1	5	dBrnC
4 Wire - 2 Wire		-	-89	-85	dBmOp
Absolute Delay	0°C ≤ T _A ≤ 75°C	-	-	2	μs
2 Wire - 4 Wire		-	-	2	μs
4 Wire - 2 Wire		36	40	-	dB
Trans Hybrid Loss	Balance Network Set Up for 600 Ohm Termination at 1kHz				dB
Overload Level	0°C ≤ T _A ≤ 75°C	1.75	-	-	Vpeak
2 Wire - 4 Wire		1.75	-	-	Vpeak
4 Wire - 2 Wire					
Level Linearity	at 1kHz, 0°C ≤ T _A ≤ 75°C				
2 Wire - 4 Wire	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB
4 Wire - 2 Wire	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB
Power Supply Rejection Ratio	0°C ≤ T _A ≤ 75°C				
V _{B+} to 2 Wire	30 - 60Hz, R _{LINE} = 600Ω	15	-	-	dB
V _{B+} to Transmit		15	-	-	dB
V _{B-} to 2 Wire		15	-	-	dB
V _{B-} to Transmit		15	-	-	dB
V _{B+} to 2 Wire	200 - 16kHz	30	-	-	dB
V _{B+} to Transmit	R _{LINE} = 600Ω	30	-	-	dB
V _{B-} to 2 Wire		30	-	-	dB
V _{B-} to Transmit		30	-	-	dB
Logic Input Current (RS, RC, PD)	0V ≤ V _{IN} ≤ 5V	-	-	±100	μA
Logic Inputs					
Logic '0' V _{Ij}		-	-	0.8	Volts
Logic '1' V _{Ij}		2.0	-	5.5	Volts
Logic Outputs					
Logic '0' V _{OL}	I _{LOAD} 800μA	-	0.1	0.5	Volts
Logic '1' V _{OH}	I _{LOAD} 80μA	2.7	5.0	5.5	Volts

Uncommitted Op Amp Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Input Bias Current		-	20	-	nA
Differential Input Resistance		-	1	-	MΩ
Output Voltage Swing	R _L = 10K	-	±5	-	Vpeak
Output Resistance	A _{VCL} = 1	-	10	-	Ω
Small Signal GBW		-	1	-	MHz

Pin Assignments HC-5502A

T-75-11-17

HARRIS SEMICOND SECTOR

28 PIN PLCC	24 PIN DIP	SYMBOL	DESCRIPTION
2	1	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay. Functions with the Ring terminal to receive voice signals from the telephone and for Loop Monitoring Purposes.
3	2	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.
4	3	V _{B+}	Positive Voltage Source - Most positive supply. V _{B+} is typically 12 volts with an operational range of 10.8 to 13.2 volts.
5	4	C1	Capacitor #1 - Optional Capacitor used to improve power supply rejection. This pin should be left open if unused.
6	5	C3	Capacitor #3 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering V _{B-} supply. Typical value is 0.3μF, 30V.
7	6	DG	Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC.
9	7	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock is arranged such that a positive transition occurs on the negative going zero crossing of the ring voltage source, ensuring that the ring relay is activated and deactivated when the instantaneous ring voltage is near zero. If synchronization is not required, tie to +5V.
10	8	RD	Relay Driver - A low active open collector logic output. When enabled, the external ring relay is energized.
11	9	TF	Tip Feed - A low impedance analog output connected to the TIP terminal through a 150Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.
12	10	RF	Ring Feed - A low impedance analog output connected to the RING terminal through a 150Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal currents.
13	11	V _{B-}	Negative Voltage Source - Most negative supply. V _{B-} is typically -48 volts with an operational range of -42 to -58 volts. Frequently referred to as "battery".
14	12	BG	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
16	13	SHD	Switch Hook Detection - A low active LS TTL - compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.
17	14	GKD	Ground Key Detection - A low active LS TTL - compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA, and disabled if this current difference is less than 10mA.
18	15	PD	Power Denial - A low active TTL - Compatible logic input. When enabled the switch hook detect (SHD) and ground key detect (GKD) are not necessarily valid, and the relay driver, (RD) output is disabled.
19	16	RC	Ring Command - A low active TTL - Compatible logic input. When enabled, the relay driver (RD) output goes low on the next rising edge of the ring sync (RS) input, as long as the SLIC is not in the power denial state (PD = 0) or the subscriber is not already off-hook (SHD = 0).
20	17	C2	Capacitor #2 - An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15μF, 10V. This capacitor is not used if ground key function is not required.
21	18	OUT	The analog output of the spare operational amplifier.
23	19	-IN	The inverting analog input of the spare operational amplifier.
24	20	+IN	The non-inverting analog input of the spare operational amplifier.
25	21	RX	Receive Input, Four Wire Side - A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed amplifiers, which in turn drive tip and ring through 300 Ohms of feed resistance on each side of the line.
26	22	C4	Capacitor #4 - An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from near proximity power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5μF, to 1.0μF, 20V. This capacitor should be nonpolarized.
27	23	AG	Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
28	24	TX	Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.
1,8,15,22		NC	No Internal Connection.

HC-5502A

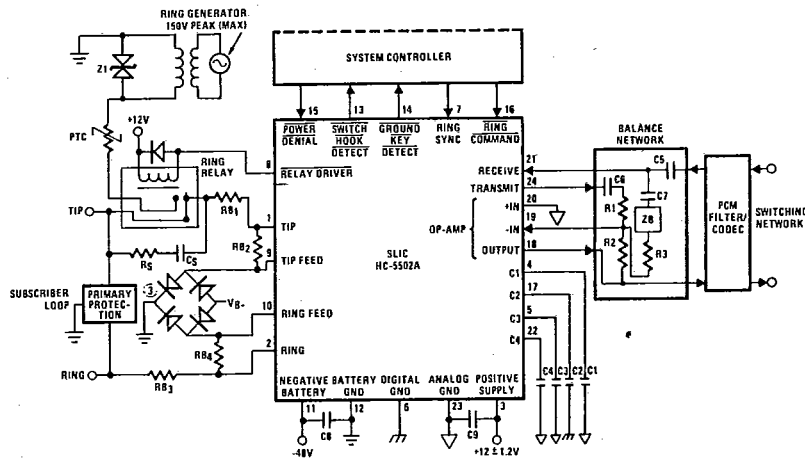
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NOTE: All grounds (AG, BG, & DG) must be applied before V_{B+} or V_{B-}. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

HARRIS SEMICOND SECTOR
Applications Diagram

TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC



TYPICAL COMPONENT VALUES

- C1 = 0.5μF (Note 1)
- C2 = 0.15μF, 10V
- C3 = 0.3μF, 30V
- C4 = 0.5μF to 1.0μF, ±10%, 20V (Should be nonpolarized)
- C5 = 0.5μF, 20V
- C6 = C7 = 0.5μF (10% Match Required) (Note 2), 20V
- C8 = 0.01μF, 100V
- C9 = 0.01μF, 20V, ±20%

R1 → R3 = 100kΩ (0.1% Match Required, 1% absolute value), ZB = 0 for 600Ω Terminations (Note 2)
 RB1 = RB2 = RB3 = RB4 = 150Ω (0.1% Match Required, 1% absolute value)
 RS = 1kΩ, CS = 0.1μF, 200V typically, depending on V_{Ring} and line length.
 Z1 = 150V to 200V transient protector. PTC used as ring ballast.

NOTE 1: C1 is an optional capacitor used to improve +12V supply rejection. This pin must be left open if unused.

NOTE 2: To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C6-R1 and R2 and C7-ZB-R3, to match in impedance to within 0.3%. Thus, if C6 and C7 and 1μF each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a ~10.5 to -21 volt step when the loop is closed and that too large a value for C6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.

A 0.5μF and 100kΩ gives a time constant of 50msec. The uncommitted op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.

NOTE 3: Secondary protection diode bridge recommended is MDA 220 or equivalent.

ADDITIONAL INFORMATION IS CONTAINED IN APPLICATION NOTE 649, "THE HC-550X TELEPHONE SLICs"
 BY GEOFF PHILLIPS

Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum of 30mA RMS, 15mA RMA per leg, without any performance degradation.

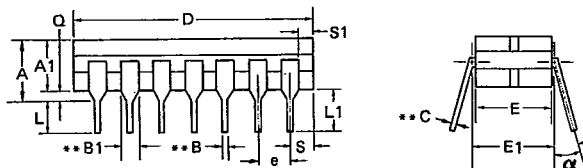
TABLE 1

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10μs Rise/	±1000 (Plastic)	V Peak
	1000μs/Fall	±500 (Ceramic)	V Peak
Metallic Surge	10μs Rise/	±1000 (Plastic)	V Peak
	1000μ Fall	±500 (Ceramic)	V Peak
T/GND	10μs Rise/	±1000 (Plastic)	V Peak
R/GND	1000μs Fall	±500 (Ceramic)	V Peak
50/60Hz Current	700V rms Limited to 10A rms	11	Cycles

Package Configuration

A B C D E .300 CERAMIC DUAL-IN-LINE

T-90-20

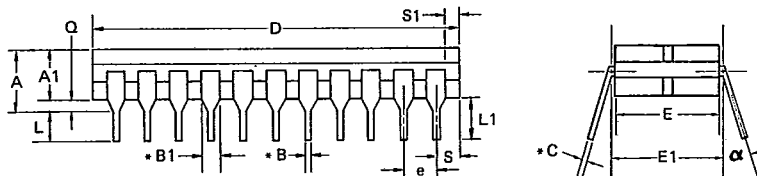


PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q	DIM. α
A	8 SSI	—	.140 .160	.016 .023	.050 .065	.008 .015	.375 .395	.245 .265	.290 .310	.100 BSC	.125 .150	.150 —	— .055	.005 —	.015 .060	0° 15°
B1	14 MSI	—	.140 .170	.016 .023	.050 .065	.008 .015	.763 .785	.265 .285	.290 .310	.100 BSC	.125 .180	.150 —	— .098	.005 —	.015 .060	0° 15°
B2	14 LSI	—	.140 .170	.016 .023	.050 .065	.008 .015	.753 .785	.285 .305	.300 .320	.100 BSC	.125 .180	.150 —	— .098	.005 —	.015 .060	0° 15°
C1	16* MSI	—	.140 .170	.016 .023	.050* .065*	.008 .015	.753 .785	.265 .285	.290 .310	.100 BSC	.125 .180	.150 —	— .080	.005 —	.015 .060	0° 15°
C2	16* LSI	—	.140 .170	.016 .023	.050* .065*	.008 .015	.753 .785	.285 .305	.300 .320	.100 BSC	.125 .180	.150 —	— .080	.005 —	.015 .060	0° 15°
D	18 LSI	—	.140 .170	.016 .023	.050* .065*	.008 .015	.882 .915	.285 .305	.300 .320	.100 BSC	.125 .180	.150 —	— .098	.005 —	.015 .060	0° 15°
E	20 LSI	—	.140 .170	.016 .023	.050* .065*	.008 .015	.940 .970	.285 .305	.300 .320	.100 BSC	.125 .180	.150 —	— .080	.005 —	.015 .060	0° 15°

* End leads are half leads where B remains the same and B1 is 0.035
 ** Solder dip finish add +0.003 inches 0.045

F .400 CERAMIC DUAL-IN-LINE

G H .600 CERAMIC DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q	DIM. α
F .400	22 LSI	— .225	.150 .180	.016 .023	.050 .065	.008 .015	1.055 1.085	.375 .395	.395 .415	.100 BSC	.125 .180	.150 —	— .080	.005 —	.015 .060	0° 15°
G .600	24 LSI	— .225	.150 .180	.016 .023	.050 .065	.008 .015	1.24 1.27	.515 .535	.595 .615	.100 BSC	.125 .180	.150 —	— .098	.005 —	.015 .060	0° 15°
H .600	26 LSI	— .225	.160 .190	.016 .023	.050 .065	.008 .015	1.44 1.47	.515 .535	.595 .615	.100 BSC	.125 .180	.150 —	— .098	.005 —	.015 .060	0° 15°

* Solder dip finish add +0.003 inches.

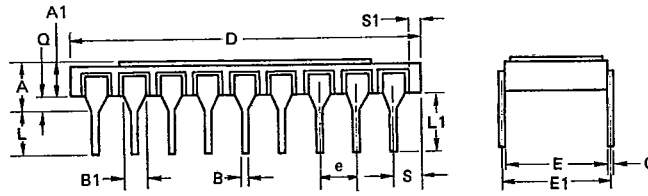
NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$ Dimensions are in inches.

BSC means basic spacing between centerlines.

Package Configuration

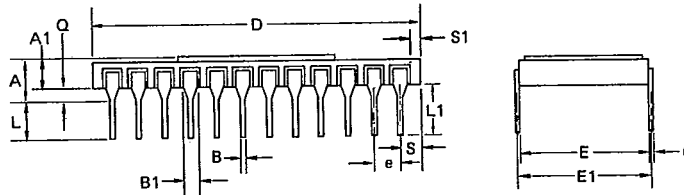
T-90-20

I .300 SIDEBRAZE DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q
I	18	— .200	.080 .110	.016 .023	.045 .060	.008 .015	.890 .910	.280 .300	.290 .310	.100 BSC	.125 .180	.150 —	— .098	.005 —	.025 .045

J-K-L .600 SIDEBRAZE DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q
J	24	— .225	.080 .110	.016 .023	.040 .054	.008 .015	1.185 1.215	.587 .603	.598 .612	.100 BSC	.125 .180	.150 —	— .080	.005 —	.040 .060
K	28	— .225	.080 .110	.016 .023	.040 .054	.008 .015	1.385 1.415	.587 .603	.598 .612	.100 BSC	.125 .180	.150 —	— .080	.005 —	.030 .060
L	40	— .225	.080 .110	.016 .023	.040 .054	.008 .015	1.980 2.020	.587 .603	.598 .612	.100 BSC	.125 .180	.150 —	— .080	.005 —	.040 .060

NOTE: Dimensions are $\frac{\text{Min.}}{\text{Max}}$. Dimensions are in inches.

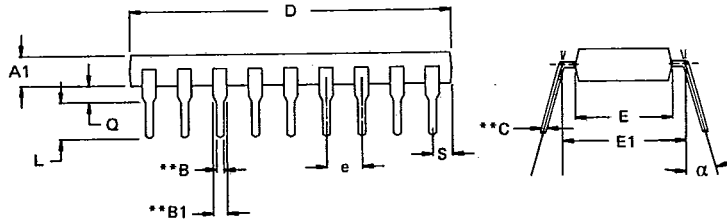
BSC means basic spacing between centerlines.

PACKAGING

Package Configuration

T-90-20

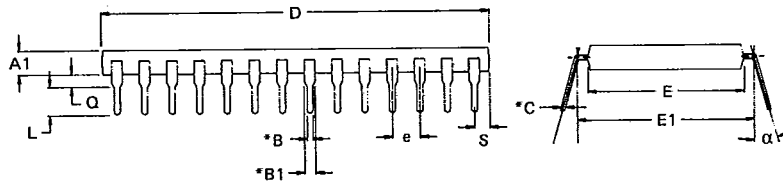
M N O P Q .300 PLASTIC DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. S	DIM. Q	DIM. alpha
M	8	.125 .140	.016 .023	.050 .070	.008 .015	.370 .390	.245 .265	.290 .310	.090 .110	.110 .150	.030 .050	.020 .040	0° 15°
N	14	.125 .140	.016 .023	.050 .070	.008 .015	.750 .770	.245 .265	.290 .310	.090 .110	.110 .150	.030 .050	.020 .040	0° 15°
O	16*	.125 .140	.016 .023	.050 .070	.008 .015	.750 .770	.245 .265	.290 .310	.090 .110	.110 .150	.025 .035	.020 .040	0° 15°
P	18	.125 .140	.016 .023	.050 .070	.008 .015	.900 .920	.245 .265	.290 .310	.090 .110	.110 .150	.040 .060	.020 .040	0° 15°
Q	20	.130 .145	.016 .023	.050 .070	.008 .015	1.030 1.050	.250 .270	.290 .310	.090 .110	.110 .150	.060 .080	.020 .040	0° 15°

* End leads are half leads where B remains the same and B1 is $\frac{0.035}{0.045}$
 ** Solder dip finish add 0.003 inches.

R S .600 PLASTIC DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. S	DIM. Q	DIM. alpha
R	24	.145 .155	.016 .023	.050 .070	.008 .015	1.24 1.26	.540 .560	.590 .610	.090 .110	.110 .150	.045 .095	.020 .040	0° 15°
S	28	.145 .155	.016 .023	.050 .070	.008 .015	1.54 1.57	.540 .560	.590 .610	.090 .110	.110 .150	.110 .160	.020 .040	0° 15°

* Solder dip finish add 0.003 inches.

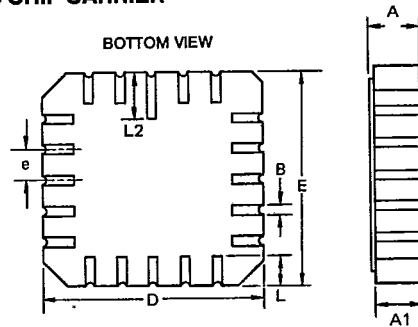
NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

BSC means basic spacing between centerlines.

Package Configuration

T-90-20

- T** .350 CERAMIC LEADLESS CHIP CARRIER*
- U** .450 CERAMIC LEADLESS CHIP CARRIER*
- V** .650 CERAMIC LEADLESS CHIP CARRIER*

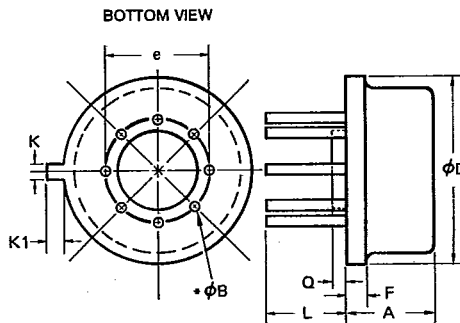


PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. D	DIM. E	DIM. e	DIM. L	DIM. L2
T	20	.073	.063	.022	.342	.342	.050	.045	.075
	.350 SQ	.089	.077	.028	.358	.358	BSC	.055	.095
U	28	.074	.064	.022	.442	.442	.050	.045	.075
	.450 SQ	.088	.076	.028	.458	.458	BSC	.055	.095
V	44	.073	.063	.022	.643	.643	.050	.045	.075
	.650 SQ	.089	.077	.028	.662	.662	BSC	.055	.095

* Solder dip finish for military parts conform to MIL-M-38510, Type A.

W TO-99 METAL CAN

X TO-100 METAL CAN



PKG. CODE	LEAD COUNT	DIM. A	DIM. φB	DIM. φD	DIM. e	DIM. F	DIM. K	DIM. K1	DIM. L	DIM. Q
W	8	.165	.016	.345	.190	.020	.028	.028	.505	.015
	TO-99	.185	.018	.365	.210	.040	.034	.040	.550	.040
X	10	.165	.016	.345	.220	.020	.028	.028	.505	.015
	TO-100	.185	.018	.365	.240	.040	.034	.040	.550	.040

* Solder dip finish add +0.003 inches.

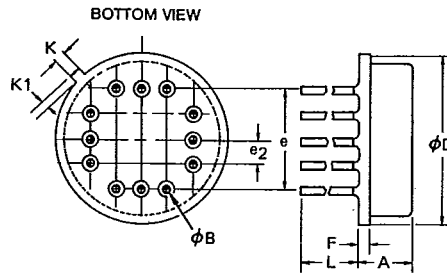
NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

BSC means basic spacing between centerlines.

Package Configuration

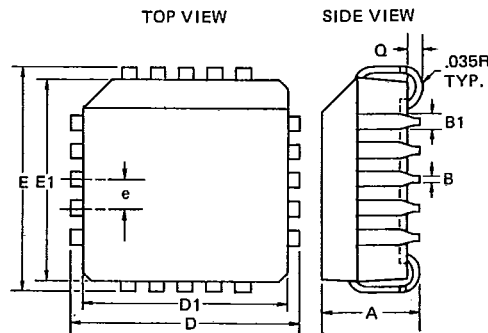
T-90-20

Y TO-8 METAL CAN



PKG. CODE	LEAD COUNT	DIM. A	DIM. phi B	DIM. phi D	DIM. e	DIM. e2	DIM. F	DIM. K	DIM. K1	DIM. L
Y	12 TO-8	.130 .150	.016 .021	.585 .615	.400 BSC	.100 BSC	.020 .040	.027 .034	.027 .045	.500 .550

AA AB AC PLASTIC LEADED CHIP CARRIER



PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. B1	DIM. D/E	DIM. D1/E1	DIM. e	DIM. Q
AA	20	.165 .180	.013 .021	.026 .032	.385 .395	.350 .356	.050 BSC	.020 —
AB	28	.165 .180	.013 .021	.026 .032	.485 .495	.450 .456	.050 BSC	.020 —
AC	44	.165 .180	.013 .021	.026 .032	.685 .695	.650 .656	.050 BSC	.020 —

NOTE: Dimensions are $\frac{\text{Min.}}{\text{Max.}}$ Dimensions are in inches.

BSC means basic spacing between centerlines.