

# OKI Semiconductor

## MSM5416263

262,144-Word × 16-Bit Multiport DRAM

preliminary

### DESCRIPTION

The MSM5416263 is a 4-Mbit CMOS multiport DRAM composed of a 262,144-word by 16-bit dynamic RAM and a 512-word by 16-bit SAM. Its RAM and SAM operate independently and asynchronously.

The MSM5416263 supports three types of operations: random access to RAM port, high speed serial access to SAM port and bidirectional transfer of data between any selected row in the RAM port and the SAM port. In addition to the conventional multiport DRAM operating modes, the MSM5416263 features the block write, flash write functions and extended page mode on the RAM port and a split data transfer capability, programmable stops on the SAM port. The SAM port requires no refresh operation because it uses static CMOS flip-flops.

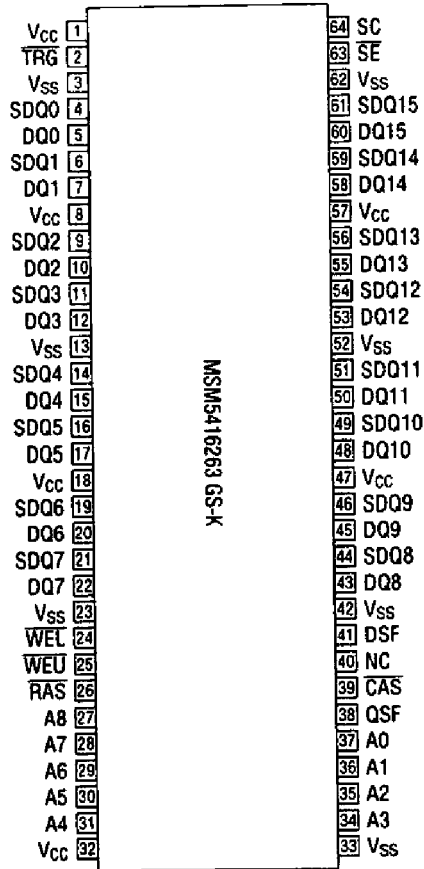
### FEATURES

- Single power supply: 5V ± 10%
- Full TTL compatibility
- Multiport organization
  - RAM : 256K word × 16bits
  - SAM : 512 word × 16bits
- Extended page mode
- Write per bit
- Persistent write per bit
- Byte write
- Masked flash write
- Masked block write (4 × 4 × 4)
- $\overline{\text{RAS}}$  only refresh
- $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh
- Hidden refresh
- Serial read/write
- 512 tap location
- Programmable stops
- Bidirectional data transfer
- Split transfer
- Masked write transfer
- Refresh: 512 cycles/8ms
- Package: 525mil 64pin SSOP (SSOP64-P-525-K)

### PRODUCT FAMILY

Family	Access Time		Cycle Time		Power Dissipation	
	RAM	SAM	RAM	SAM	Operating	Standby
MSM5416263-50	50ns	17ns	110ns	20ns	160mA	9mA
MSM5416263-60	60ns	18ns	120ns	22ns	150mA	9mA
MSM5416263-70	70ns	20ns	140ns	22ns	140mA	9mA

ION (TOP VIEW)



64-PIN SSOP

Function	Pin Name	Function
Address Input	SC	Serial Clock
RAM Inputs/Outputs	SE	SAM Port Enable
SAM Inputs/Outputs	DSF	Special Function Input
Row Address Strobe	QSF	Special Function Output
Column Address Strobe	Vcc	Power Supply (5V)
Write Enable Lower	Vss	Ground (0V)
Write Enable Upper	NC	No Connection
Transfer/Output Enable		



DC Characteristics 2

(V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 0 to 70°C)

ITEM (RAM)	SAM	Symbol	-50	-60	-70	Unit	Note	
			Max.	Max.	Max.			
Operating Current ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ Cycling, $t_{\text{RC}} = t_{\text{RC min.}}$ )	Standby	I <sub>CC1</sub>	125	115	105	mA	3, 4	
	Active	I <sub>CC1A</sub>	160	150	140		17	
Standby Current ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}} = V_{\text{IH}}$ )	Standby	I <sub>CC2</sub>	9	9	9			
	Active	I <sub>CC2A</sub>	55	50	50		3, 4	
RAS Only Refresh ( $\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} = V_{\text{IH}}$ , $t_{\text{RC}} = t_{\text{RC min.}}$ )	Standby	I <sub>CC3</sub>	125	115	105			3, 4
	Active	I <sub>CC3A</sub>	160	150	140			17
Page Mode Current ( $\overline{\text{RAS}} = V_{\text{IL}}$ , $\overline{\text{CAS}}$ Cycling, $t_{\text{PC}} = t_{\text{PC min.}}$ )	Standby	I <sub>CC4</sub>	95	85	75			3, 4
	Active	I <sub>CC4A</sub>	160	150	140			18
CAS Before $\overline{\text{RAS}}$ Refresh Current ( $\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ , $t_{\text{RC}} = t_{\text{RC min.}}$ )	Standby	I <sub>CC5</sub>	125	115	105			3, 4
	Active	I <sub>CC5A</sub>	160	150	140			3, 4
Data Transfer Current ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ Cycling, $t_{\text{RC}} = t_{\text{RC min.}}$ )	Standby	I <sub>CC6</sub>	125	115	105			3, 4
	Active	I <sub>CC6A</sub>	160	150	140			17
Flash Write Current ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ Cycling, $t_{\text{RC}} = t_{\text{RC min.}}$ )	Standby	I <sub>CC7</sub>	125	115	105			3, 4
	Active	I <sub>CC7A</sub>	160	150	140			3, 4
Block Write Current ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ Cycling, $t_{\text{RC}} = t_{\text{RC min.}}$ )	Standby	I <sub>CC8</sub>	125	115	105			3, 4
	Active	I <sub>CC8A</sub>	160	150	140			3, 4

**ELECTRICAL CHARACTERISTICS****Absolute Maximum Ratings**

(Note: 1)

Parameter	Symbol	Condition	Rating	Unit
Input Output Voltage	$V_T$	$T_a = 25^\circ\text{C}$	-1.0 to 7.0	V
Output Current	$I_{OS}$	$T_a = 25^\circ\text{C}$	50	mA
Power Dissipation	$P_D$	$T_a = 25^\circ\text{C}$	1	W
Operating Temperature	$T_{opr}$	—	0 to 70	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	—	-55 to 150	$^\circ\text{C}$

**Recommended Operating Conditions**

(Ta = 0 to 70°C) (Note: 2)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
Input High Voltage	$V_{IH}$	2.4	—	6.5	V
Input Low Voltage	$V_{IL}$	-1.0	—	0.8	V

**Capacitance**(V<sub>CC</sub> = 5V ± 10%, f = 1MHz, T<sub>a</sub> = 25°C)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance	$C_i$	—	8	pF
Input/Output Capacitance	$C_{io}$	—	9	pF
Output Capacitance	$C_o(QSF)$	—	9	pF

Note: This parameter is periodically sampled and is not 100% tested

**DC Characteristics 1**

Parameter	Symbol	Condition	Min.	Max.	Unit
Output 'H' Level Voltage	$V_{OH}$	$I_{OH} = -1\text{mA}$	2.4	—	V
Output 'L' Level Voltage	$V_{OL}$	$I_{OL} = 2.1\text{mA}$	—	0.4	
Input Leakage Current	$I_{LI}$	$0 \leq V_{IN} \leq V_{CC}$ All other pins not under test = 0V	-10	10	$\mu\text{A}$
Output Leakage Current	$I_{LO}$	$0 \leq V_{OUT} \leq 5.5\text{V}$ Output Disable	-10	10	

## AC Characteristics (1/3)

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	$t_{RC}$	110	—	120	—	140	—	ns	
Read Modify Write Cycle	$t_{RMW}$	145	—	170	—	185	—	ns	
Fast Page Mode Cycle Time	$t_{PC}$	35	—	40	—	45	—	ns	
Fast Page Mode Read Modify Write Cycle Time	$t_{PRMW}$	80	—	85	—	90	—	ns	
Access Time from RAS	$t_{RAC}$	—	50	—	60	—	70	ns	8, 14
Access Time from Column Address	$t_{AAC}$	—	25	—	30	—	35	ns	8, 14
Access Time from CAS	$t_{CAC}$	—	15	—	18	—	20	ns	8, 15
Access Time from CAS Precharge	$t_{CPA}$	—	30	—	35	—	40	ns	8, 15
Output Buffer Turn-off Delay	$t_{OFF}$	0	12	0	15	0	17	ns	10
Transition Time (Rise and Fall)	$t_T$	3	35	3	35	3	35	ns	7
RAS Precharge Time	$t_{RP}$	40	—	50	—	60	—	ns	
RAS Pulse Width	$t_{RAS}$	50	10K	60	10K	70	10K	ns	
RAS Pulse Width (Fast Page Mode Only)	$t_{RASP}$	50	100K	60	100K	70	100K	ns	
RAS Hold Time	$t_{RSH}$	15	—	15	—	20	—	ns	
CAS Hold Time	$t_{CSH}$	50	—	60	—	70	—	ns	
CAS Pulse Width	$t_{CAS}$	12	10K	15	10K	20	10K	ns	
RAS to CAS Delay Time	$t_{RCD}$	18	35	20	42	20	50	ns	14
RAS to Column Address Delay Time	$t_{RAD}$	13	25	15	30	15	35	ns	14
Column Address to RAS Lead Time	$t_{RAL}$	25	—	30	—	35	—	ns	
CAS to RAS Precharge Time	$t_{CRP}$	5	—	5	—	10	—	ns	
CAS Precharge Time (Fast Page Mode)	$t_{CP}$	8	—	10	—	10	—	ns	
Row Address Set-up Time	$t_{ASR}$	0	—	0	—	0	—	ns	
Row Address Hold Time	$t_{RAH}$	8	—	10	—	10	—	ns	
Column Address Set-up Time	$t_{ASC}$	0	—	0	—	0	—	ns	
Column Address Hold Time	$t_{CAH}$	10	—	10	—	10	—	ns	
Column Address Hold Time Referenced to RAS	$t_{AR}$	40	—	50	—	55	—	ns	
Read Command Set-up Time	$t_{RCS}$	0	—	0	—	0	—	ns	
Read Command Hold Time	$t_{RCH}$	0	—	0	—	0	—	ns	11
Read Command Hold Time Referenced to RAS	$t_{RRH}$	0	—	0	—	0	—	ns	11
CAS 'H' to RAS 'H' Lead Time	$t_{CRL}$	0	—	0	—	0	—	ns	
RAS 'H' to CAS 'H' Lead Time	$t_{RCL}$	0	—	0	—	0	—	ns	
Data Output Hold After CAS Low	$t_{COH}$	5	—	5	—	5	—	ns	19
Write Command Set-up Time	$t_{WCS}$	0	—	0	—	0	—	ns	13
Write Command Hold Time	$t_{WCH}$	8	—	10	—	12	—	ns	
Write Command Hold Time Referenced to RAS	$t_{WCR}$	40	—	50	—	55	—	ns	
Write Command Pulse Width	$t_{WP}$	8	—	10	—	12	—	ns	
Write Command to RAS Lead Time	$t_{RWL}$	12	—	15	—	20	—	ns	
Write Command to CAS Lead Time	$t_{CWL}$	12	—	15	—	20	—	ns	

## AC Characteristics (2/3)

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Data Set-up Time	t <sub>DS</sub>	0	—	0	—	0	—	ns	12
Data Hold Time	t <sub>DH</sub>	10	—	10	—	12	—	ns	12
Data Hold Time Referenced to $\overline{\text{RAS}}$	t <sub>DHR</sub>	40	—	50	—	55	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>RWD</sub>	70	—	80	—	90	—	ns	13
Column Address to $\overline{\text{WE}}$ Delay Time	t <sub>AWD</sub>	45	—	50	—	55	—	ns	13
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>CWD</sub>	30	—	35	—	40	—	ns	13
Data to $\overline{\text{CAS}}$ Delay Time	t <sub>DZC</sub>	0	—	0	—	0	—	ns	
Data to TRG Delay Time	t <sub>DZO</sub>	0	—	0	—	0	—	ns	
Access Time from TRG	t <sub>OEA</sub>	—	15	—	18	—	20	ns	
Output Buffer Turn-off Delay from TRG	t <sub>OEZ</sub>	0	12	0	15	0	17	ns	
TRG Command Hold Time	t <sub>OEH</sub>	8	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ Hold Time Referenced to TRG	t <sub>ROH</sub>	10	—	10	—	15	—	ns	
$\overline{\text{CAS}}$ Set-up Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycle	t <sub>CSR</sub>	8	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycle	t <sub>CHR</sub>	8	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t <sub>RPC</sub>	0	—	0	—	0	—	ns	
Refresh Period	t <sub>REF</sub>	—	8	—	8	—	8	ms	
$\overline{\text{WE}}$ Set-up Time	t <sub>WSR</sub>	0	—	0	—	0	—	ns	
$\overline{\text{WE}}$ Hold Time	t <sub>RWH</sub>	10	—	10	—	10	—	ns	
DSF Set-up Time Referenced to $\overline{\text{RAS}}$	t <sub>FSR</sub>	0	—	0	—	0	—	ns	
DSF Hold Time Referenced to $\overline{\text{RAS}}$ (1)	t <sub>RFH</sub>	10	—	10	—	10	—	ns	
DSF Hold Time Referenced to $\overline{\text{RAS}}$ (2)	t <sub>FHR</sub>	40	—	50	—	55	—	ns	
DSF Set-up Time Referenced to $\overline{\text{CAS}}$	t <sub>FSC</sub>	0	—	0	—	0	—	ns	
DSF Hold Time Referenced to $\overline{\text{CAS}}$	t <sub>CFH</sub>	10	—	10	—	10	—	ns	
Write Per Bit Mask Data Set-up Time	t <sub>MS</sub>	0	—	0	—	0	—	ns	
Write Per Bit Mask Data Hold Time	t <sub>MH</sub>	10	—	10	—	10	—	ns	
TRG High Set-up Time	t <sub>THS</sub>	0	—	0	—	0	—	ns	
TRG High Hold Time	t <sub>THH</sub>	10	—	10	—	10	—	ns	
TRG Low Set-up Time	t <sub>TLS</sub>	0	—	0	—	0	—	ns	
TRG Low Hold Time	t <sub>TLH</sub>	10	10K	10	10K	10	10K	ns	
TRG Low Hold Time Referenced to $\overline{\text{RAS}}$	t <sub>RTH</sub>	40	10K	50	10K	60	10K	ns	
TRG Low Hold Time Referenced to Column Address	t <sub>ATH</sub>	20	—	20	—	25	—	ns	
TRG Low Hold Time Referenced to $\overline{\text{CAS}}$	t <sub>CTH</sub>	15	—	15	—	20	—	ns	
TRG to $\overline{\text{RAS}}$ Precharge Time	t <sub>TRP</sub>	40	—	50	—	60	—	ns	
TRG Precharge Time	t <sub>TP</sub>	15	—	20	—	20	—	ns	
$\overline{\text{RAS}}$ to First SC Delay Time (Read Transfer)	t <sub>RSD</sub>	50	—	60	—	70	—	ns	
Column Address to First SC Delay Time	t <sub>ASD</sub>	35	—	40	—	45	—	ns	
$\overline{\text{CAS}}$ to First SC Delay Time (Read Transfer)	t <sub>CSD</sub>	20	—	20	—	20	—	ns	
Last SC to TRG Lead Time	t <sub>TSL</sub>	5	—	5	—	5	—	ns	

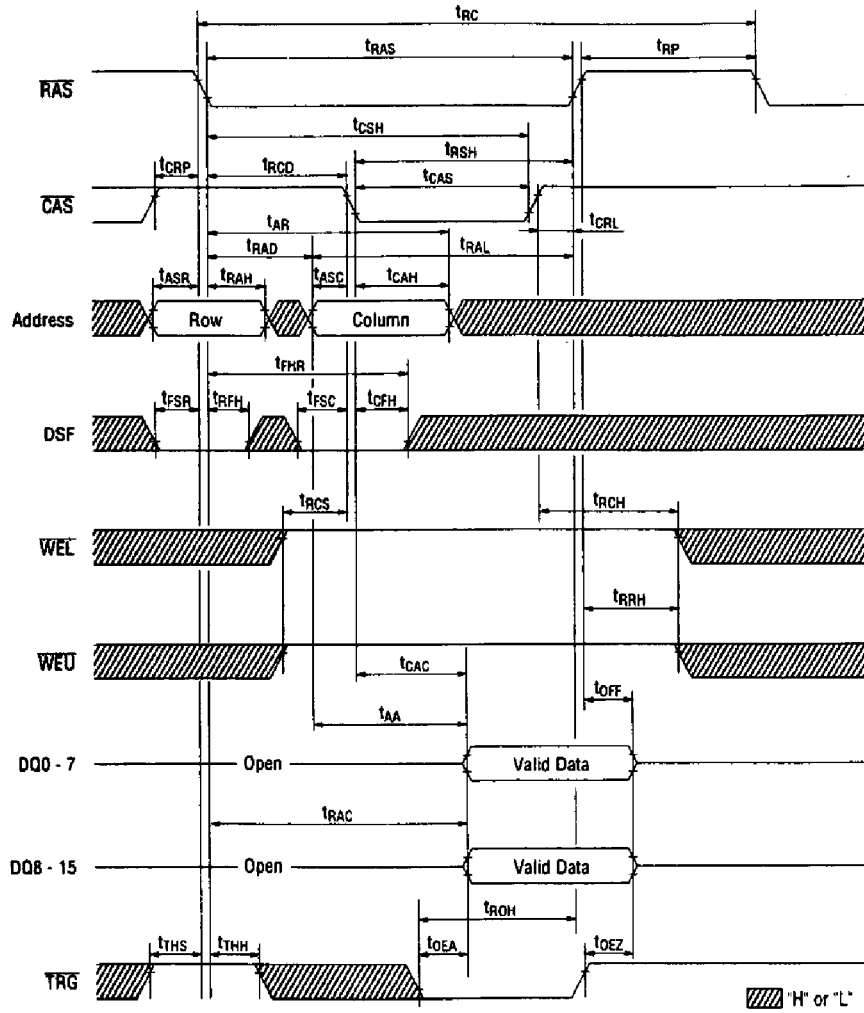
## AC Characteristics (3/3)

Parameter	Symbol	-50		-60		-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
TRG to First SC Delay Time (Read Transfer)	t <sub>TRD</sub>	15	—	15	—	15	—	ns	
Last SC to RAS Set-up Time (Serial Input)	t <sub>SRS</sub>	20	—	20	—	25	—	ns	
Serial Output Buffer Turn-off Delay from RAS	t <sub>SDZ</sub>	10	30	10	30	10	40	ns	10
SC Cycle Time	t <sub>SCC</sub>	20	—	22	—	22	—	ns	
SC Pulse Width (SC High Time)	t <sub>SC</sub>	5	—	5	—	5	—	ns	
SC Precharge Time (SC Low Time)	t <sub>SCP</sub>	5	—	5	—	5	—	ns	
Access Time from SC	t <sub>SCA</sub>	—	17	—	18	—	20	ns	9
Serial Output Hold Time from SC	t <sub>SOH</sub>	5	—	5	—	5	—	ns	19
Access Time from SE	t <sub>SEA</sub>	—	17	—	18	—	20	ns	9
SE Pulse Width	t <sub>SE</sub>	10	—	10	—	10	—	ns	
SE Precharge Time	t <sub>SEP</sub>	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from SE	t <sub>SEZ</sub>	0	14	0	15	0	17	ns	10
Split Transfer Set-up Time	t <sub>STS</sub>	25	—	25	—	25	—	ns	
Split Transfer Hold Time	t <sub>STH</sub>	25	—	25	—	25	—	ns	
SC-QSF Delay Time	t <sub>SOD</sub>	—	25	—	25	—	25	ns	
TRG-QSF Delay Time	t <sub>TQD</sub>	—	25	—	25	—	25	ns	
CAS-QSF Delay Time	t <sub>CQD</sub>	—	30	—	30	—	35	ns	
RAS-QSF Delay Time	t <sub>RQD</sub>	—	70	—	70	—	75	ns	
RAS to Serial Input Delay Time	t <sub>SDD</sub>	30	—	30	—	40	—	ns	
Serial Input Set-up Time	t <sub>SDS</sub>	0	—	0	—	0	—	ns	
Serial Input Hold Time	t <sub>SDH</sub>	8	—	10	—	10	—	ns	
Serial Input to SE Delay Time	t <sub>SZE</sub>	0	—	0	—	0	—	ns	
Serial Input to First SC Delay Time	t <sub>SZS</sub>	0	—	0	—	0	—	ns	
Serial Write Enable Set-up Time	t <sub>SWS</sub>	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t <sub>SWH</sub>	8	—	10	—	10	—	ns	
Serial Write Disable Set-up Time	t <sub>SWIS</sub>	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t <sub>SWIH</sub>	8	—	10	—	10	—	ns	

- Notes:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
  2. All voltage are referenced to  $V_{SS}$ .
  3. These parameters depend on cycle rate.
  4. These parameters depend on output loading. Specified values are obtained with the output open.
  5. An initial pause of 200 $\mu$ s is required after power up followed by any 8  $\overline{RAS}$  cycles ( $\overline{TRG} = \text{"high"}$ ) and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CAS}$  before  $\overline{RAS}$  cycles instead of 8 RAS cycles are required.
  6. AC measurements assume  $t_f = 5$ ns.
  7.  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
  8. RAM port outputs are measured with a load equivalent to 1 TTL load and 50pF. DOUT reference levels:  $V_{OH}/V_{OL} = 2.0V/0.8V$ .
  9. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF. DOUT reference levels:  $V_{OH}/V_{OL} = 2.0V/0.8V$ .
  10.  $t_{OFF}$  (Max.),  $t_{OEZ}$  (Max.),  $t_{SDZ}$  (Max.) and  $t_{SEZ}$  (Max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels. This parameter is sampled and not 100% tested.
  11. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycles.
  12. These parameters are referenced to  $\overline{CAS}$  leading edge of early write cycles and to  $\overline{WE}$  leading edge in  $\overline{TRG}$  controlled write cycles and read modify write cycles.
  13.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only.  
If  $t_{WCS} \geq t_{WCS}$  (Min.), the cycle is an early write cycles and the data out pin will remain open circuit throughout the entire cycles; If  $t_{RWD} \geq t_{RWD}$  (Min.),  $t_{CWD} \geq t_{CWD}$  (Min.) and  $t_{AWD} \geq t_{AWD}$  (Min.) the cycle is a read modify write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
  14. Operation within the  $t_{RCD}$  (Max.) limit insures that  $t_{RAC}$  (Max.) can be met.  $t_{RCD}$  (Max.) is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (Max.) limit, then access time is controlled by  $t_{CAC}$ .
  15. Operation within the  $t_{RAD}$  (Max.) limit insures that  $t_{RAC}$  (Max.) can be met.  $t_{RAD}$  (Max.) is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (Max.) limit, then access time is controlled by  $t_{AA}$ .
  16. Input levels at the AC testing are 3.0V/0V.
  17. Address (A0 - A8) may be changed two times or less while  $\overline{RAS} = V_{IL}$ .
  18. Address (A0 - A8) may be changed once or less while  $\overline{CAS} = V_{IH}$  and  $\overline{RAS} = V_{IL}$ .
  19. This is guaranteed by design. ( $t_{SOH}/t_{COH} = t_{SCA}/t_{CAC}$  - output transition time)  
This parameter is not 100% tested.

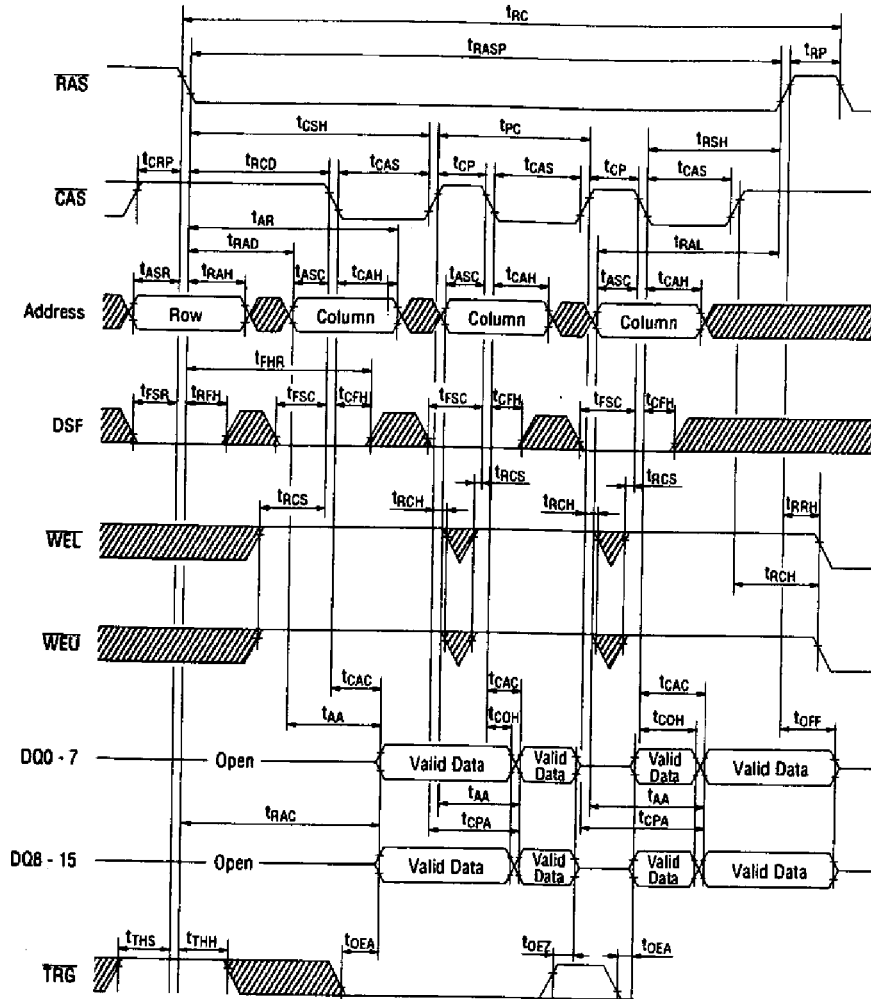
**TIMING WAVEFORM**

**Read Cycle (Outputs Controlled by RAS)**





Extended Page Mode Read Cycle



▨ "H" or "L"

Write Cycle Function Table

Code	RAS Falling Edge			CAS Falling Edge		Function
	A	C	D	B	E	
	DSF	WEL/U	DQ	DSF	DQ	
RWM	0	0	Write Mask	0	Valid Data	Masked Write (New/Old)
BWM	0	0	Write Mask	1	Column Mask	Masked Block Write (New/Old)
FWM	1	0	Write Mask	X	X	Masked Flash Write (New/Old)
RW	0	1	X	0	Valid Data	Normal Write
BW	0	1	X	1	Column Mask	Block Write
LMR	1	1	X	0	Write Mask Data	Load Mask Register
LCR	1	1	X	1	Color Data	Load Color Register

MODE	RAS Falling Edge			
	WEL	WEU	DQ0 - 7	DQ8 - 15
NEW MASK	0	0	Mask	Mask
	0	1	Mask	Mask
	1	0	Mask	Mask
PERSISTENT MASK	0	0	—	—
	0	1	—	—
	1	0	—	—
NO MASK	1	1	—	—

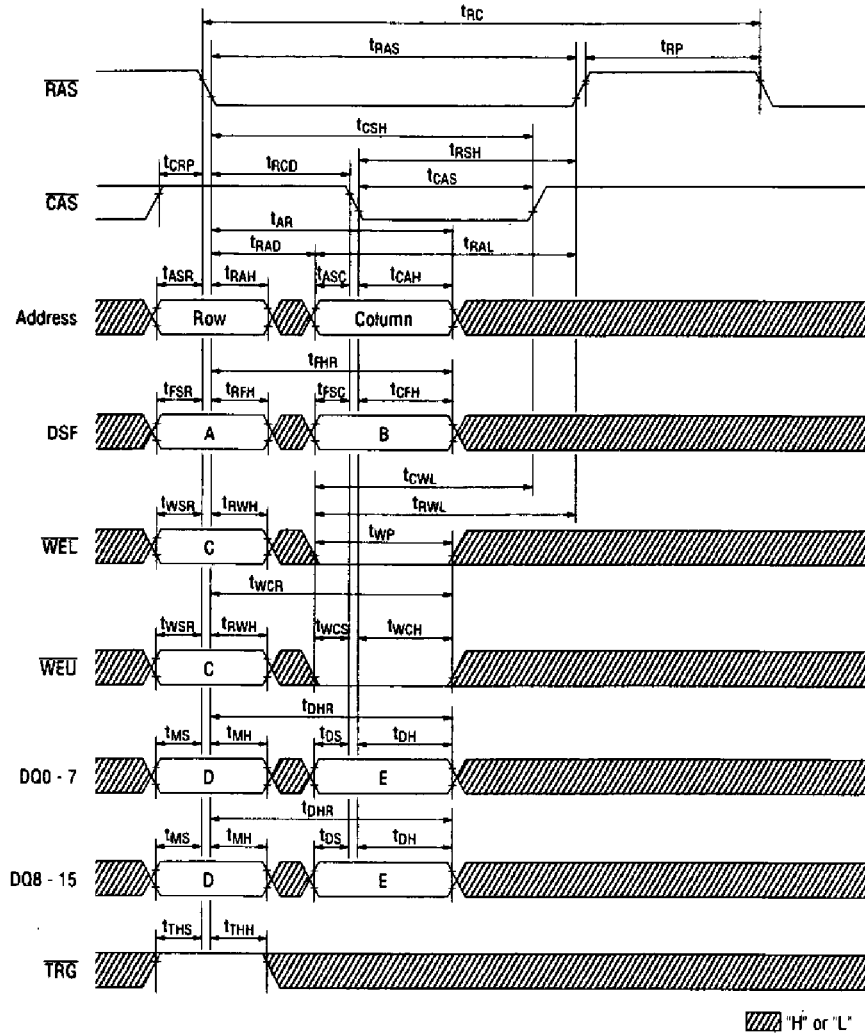
IO MASK DATA: Low = Mask, High = No Mask

IO WRITE MASK DATA: Low = Mask, High = No Mask

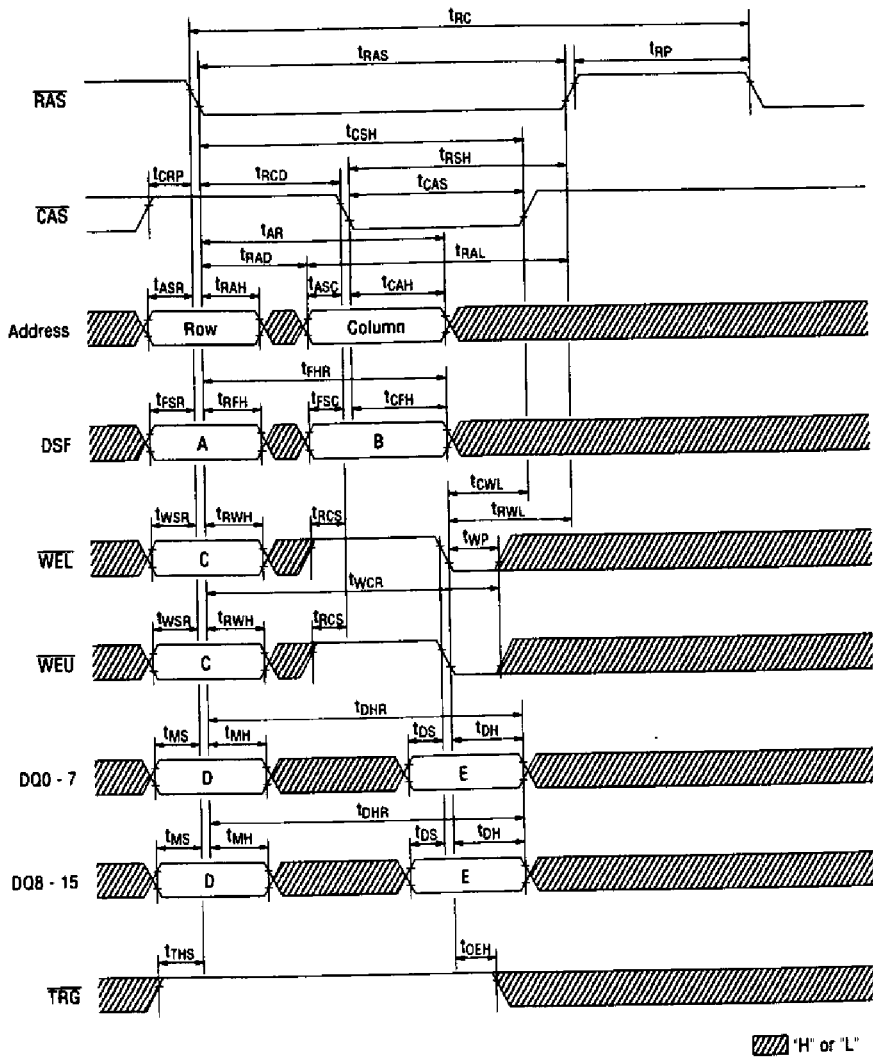
Column Mask Data

DQ0 - 15	Column Mask Data	
DQ0	Column0 (A0=0, A1=0)	Low: Mask High: No Mask
DQ1	Column1 (A0=1, A1=0)	
DQ2	Column2 (A0=0, A1=1)	
DQ3	Column3 (A0=1, A1=1)	Low: Mask High: No Mask
DQ4	Column0 (A0=0, A1=0)	
DQ5	Column1 (A0=1, A1=0)	
DQ6	Column2 (A0=0, A1=1)	Low: Mask High: No Mask
DQ7	Column3 (A0=1, A1=1)	
DQ8	Column0 (A0=0, A1=0)	
DQ9	Column1 (A0=1, A1=0)	Low: Mask High: No Mask
DQ10	Column2 (A0=0, A1=1)	
DQ11	Column3 (A0=1, A1=1)	
DQ12	Column0 (A0=0, A1=0)	Low: Mask High: No Mask
DQ13	Column1 (A0=1, A1=0)	
DQ14	Column2 (A0=0, A1=1)	
DQ15	Column3 (A0=1, A1=1)	

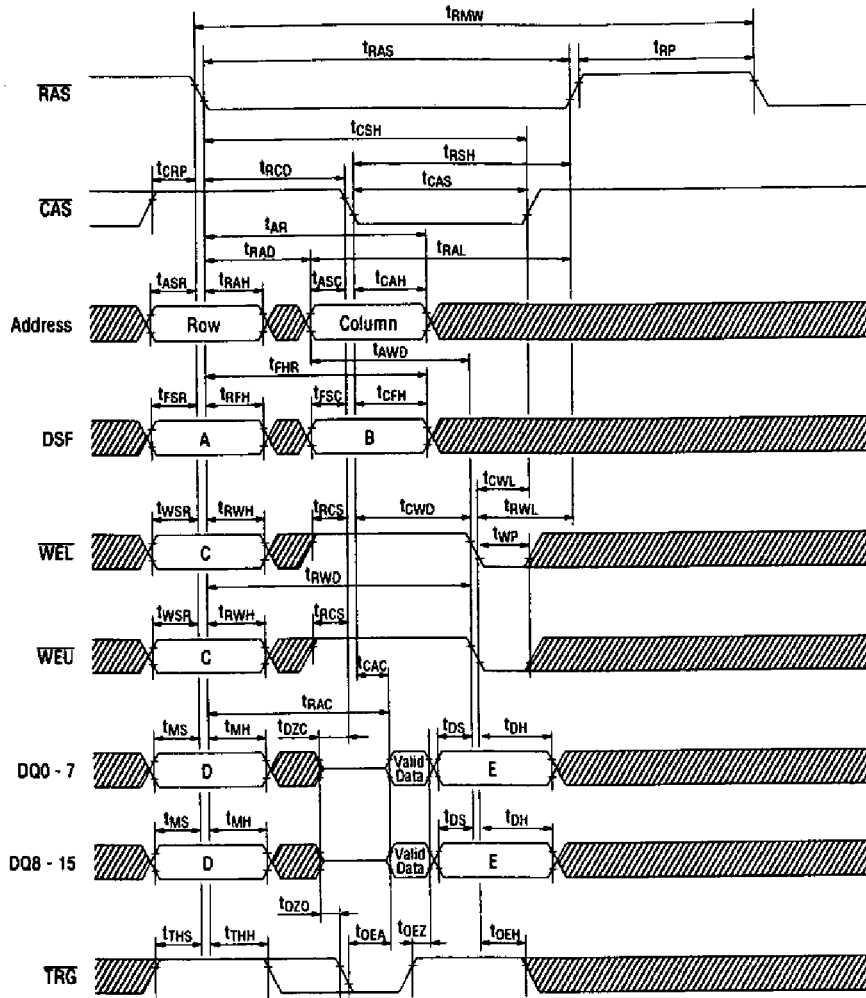
Early Write Cycle



Late Write Cycle

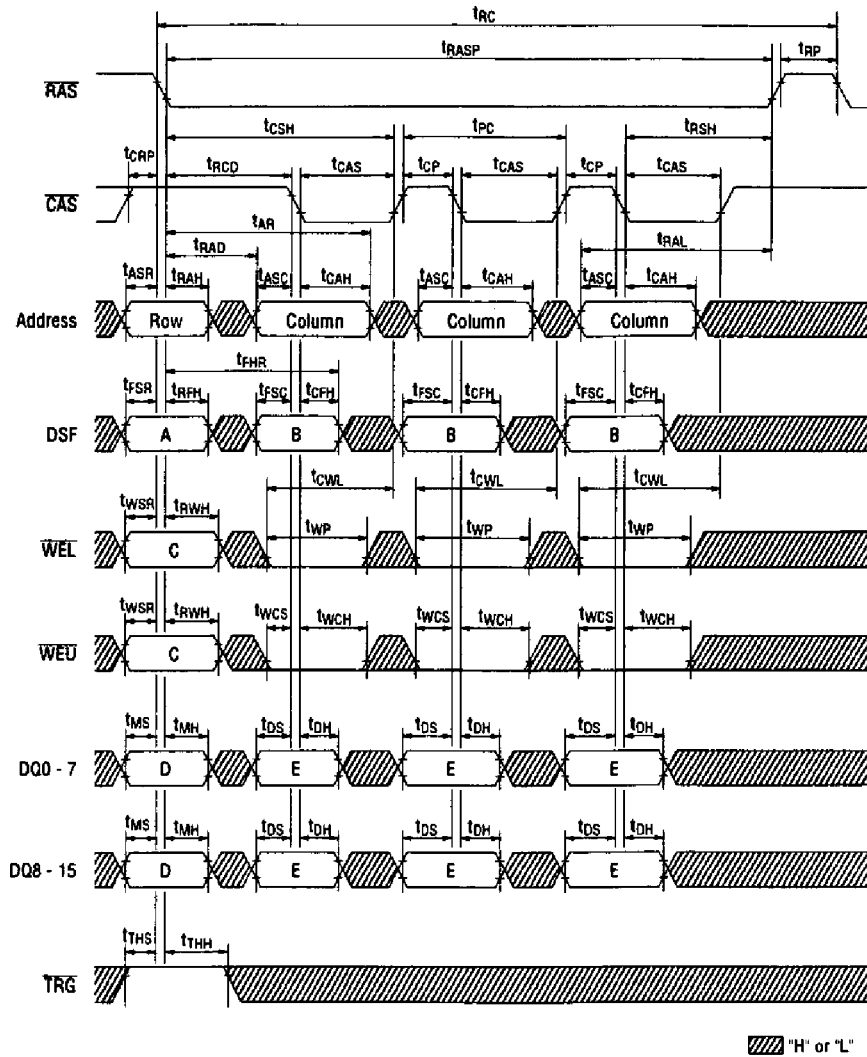


Read Modify Write Cycle



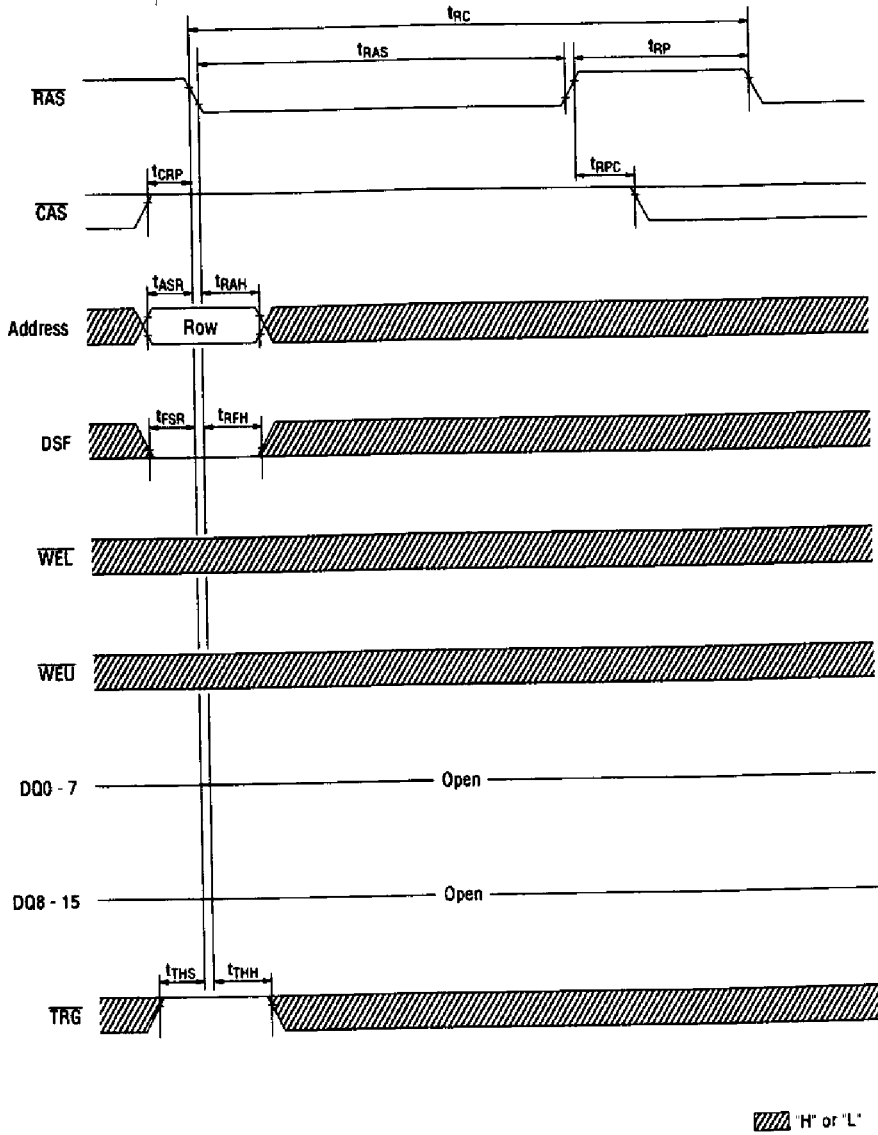
▨ "H" or "L"

Fast Page Mode Early Write Cycle

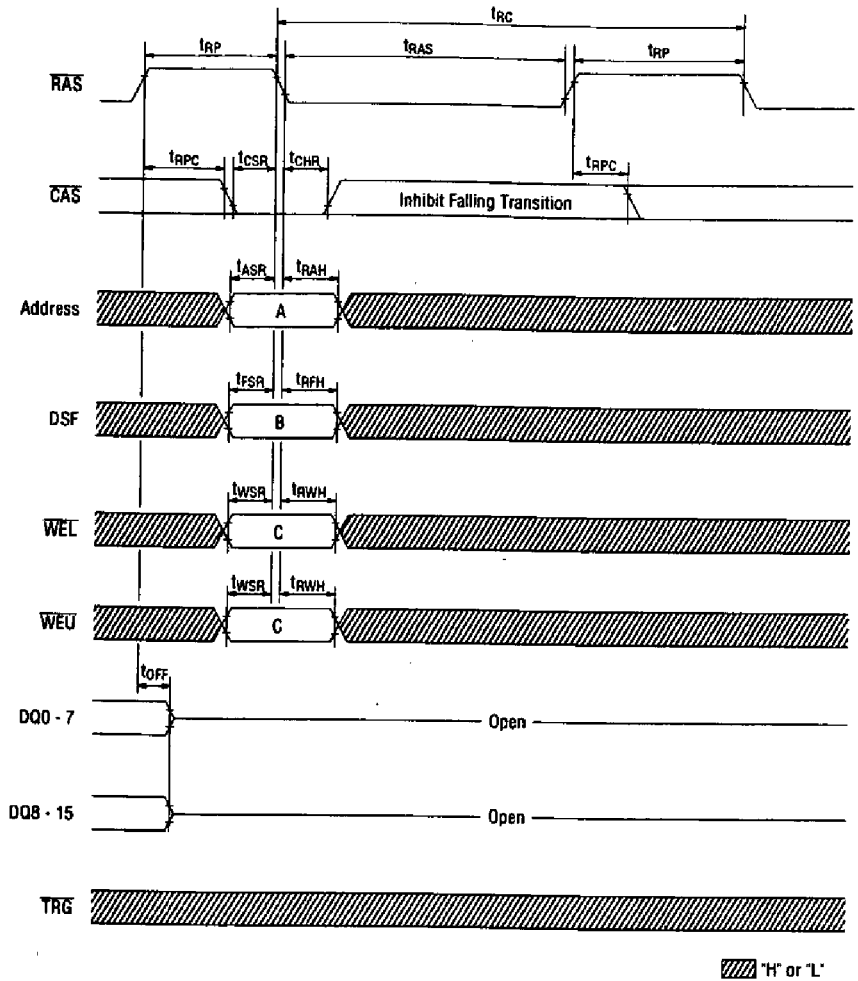




RAS Only Refresh Cycle



**CAS Before RAS Refresh Cycle**

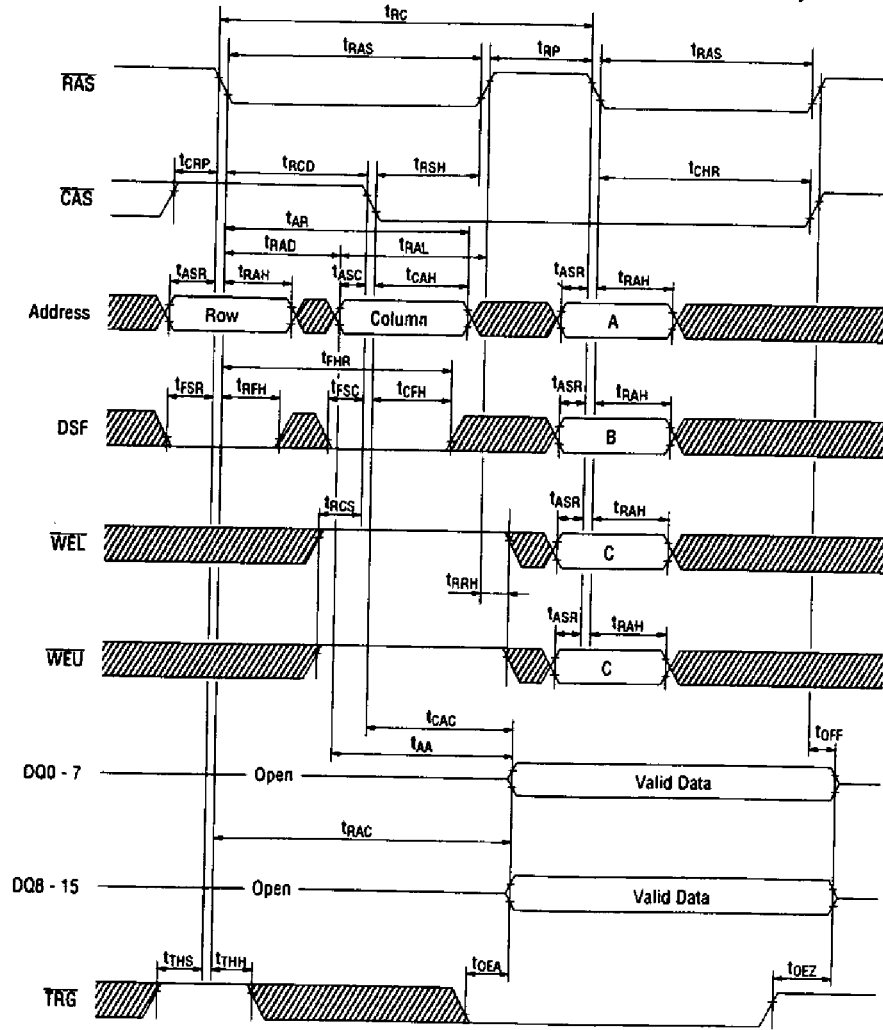


**Note:** The type of CBR operations are determined by the logic states of "A", "B" and "C".

**CBR Cycle Function Table**

Code	RAS Falling Edge			Function
	A	B	C	
CBRR	X	0	1	CBR Refresh (Reset All Options)
CBRS	STOP Address	1	0	CBR Refresh (Set STOP Address)

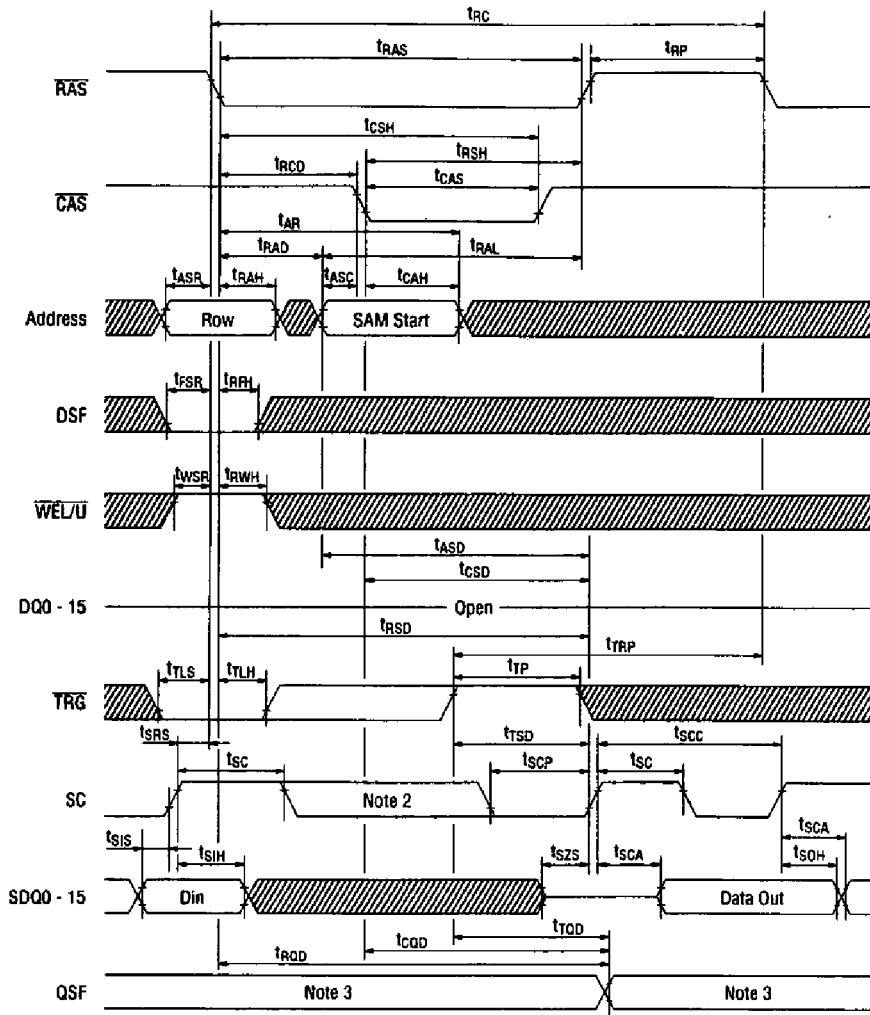
Hidden Refresh Cycle



▨ "H" or "L"

**Note:** The type of CBR operations are determined by the logic states of "A", "B" and "C".

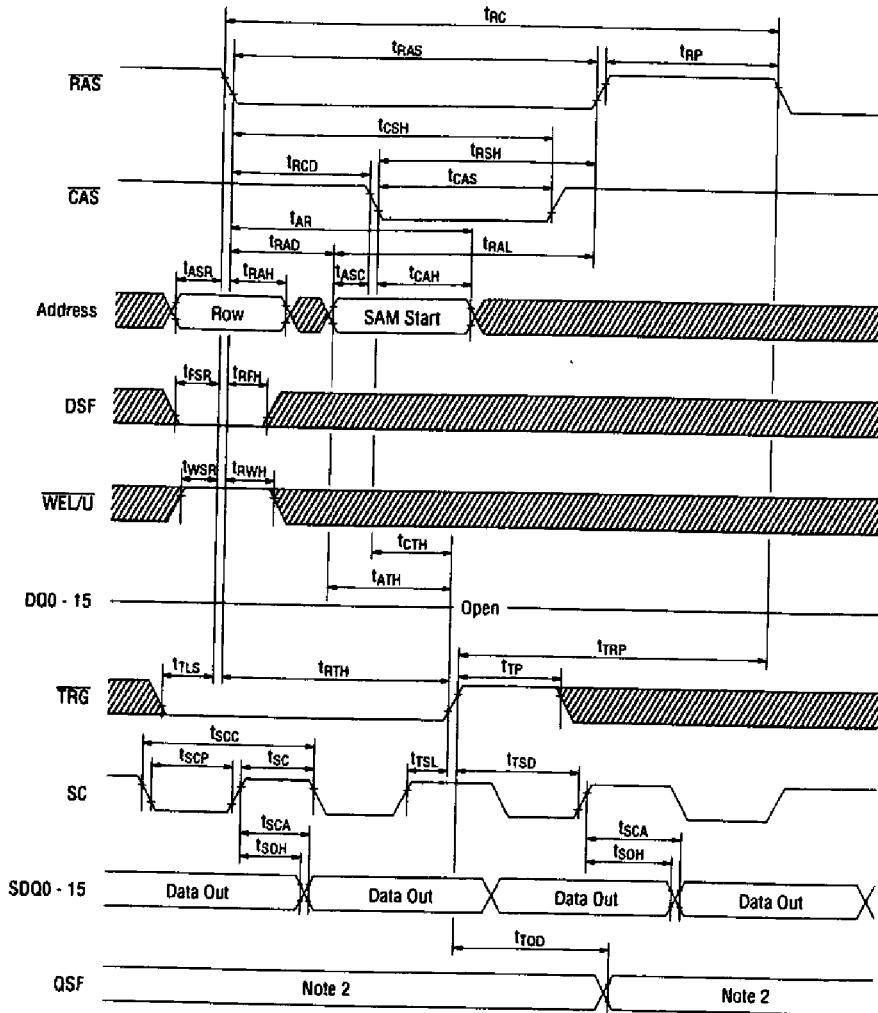
Read Transfer 1



▨ 'H' or 'L'

- Note 1:  $\overline{SE} = 'L'$
- Note 2: There must be no rising transitions
- Note 3: QSF = 'L'-- Lower SAM (0 - 255) is active  
QSF = 'H'-- Upper SAM (256 - 511) is active

Read Transfer 2 (Real Time Read Transfer)

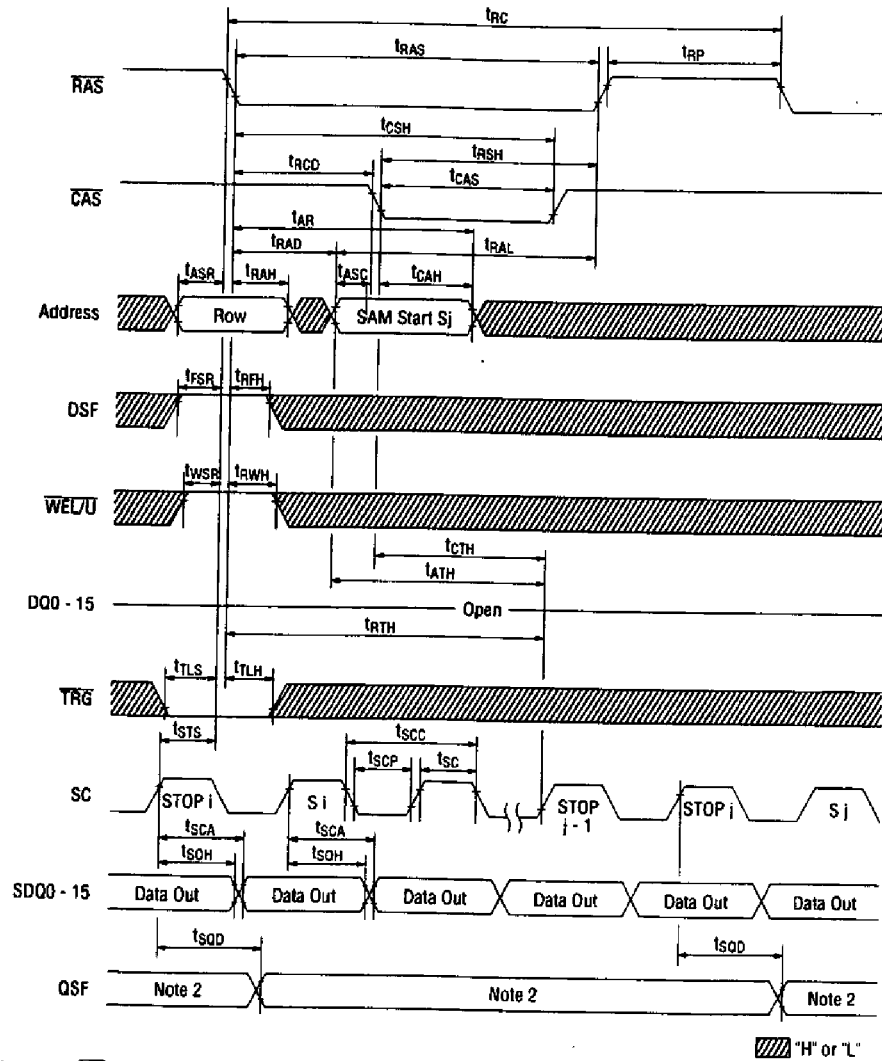


Note 1:  $\overline{SE} = "L"$

Note 2: QSF = "L"-- Lower SAM (0 - 255) is active  
 QSF = "H"-- Upper SAM (256 - 511) is active

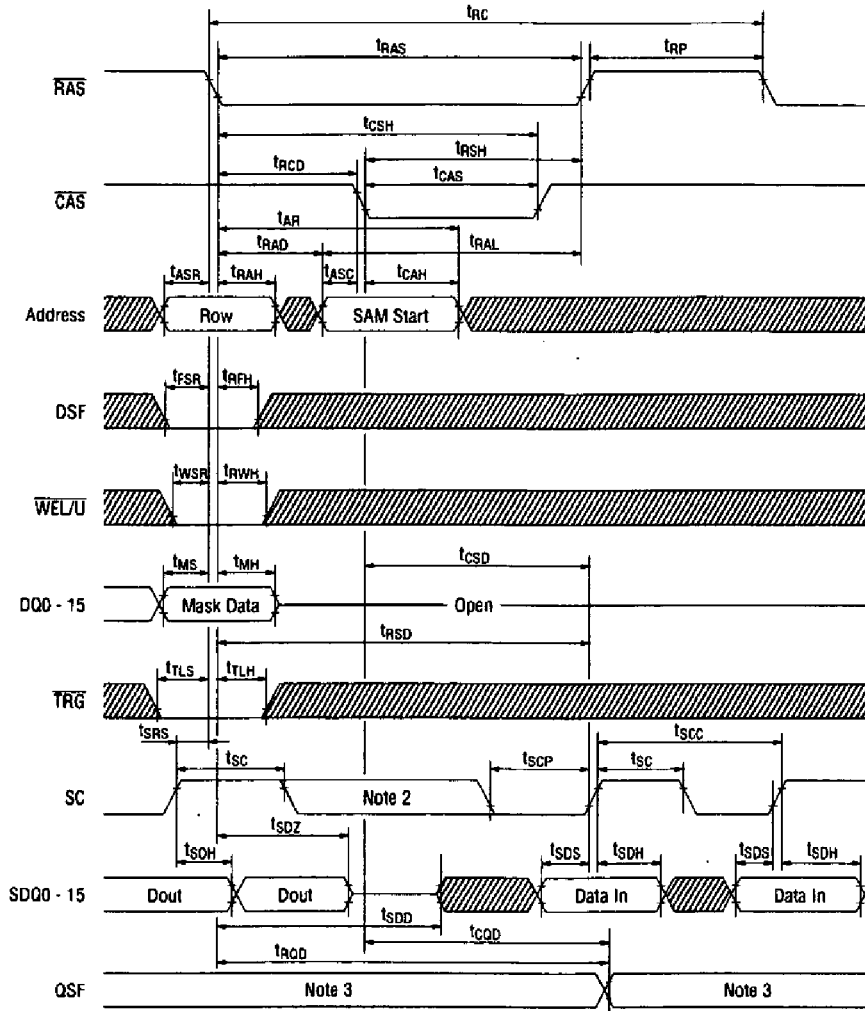
▨ "H" or "L"

Split Read Transfer



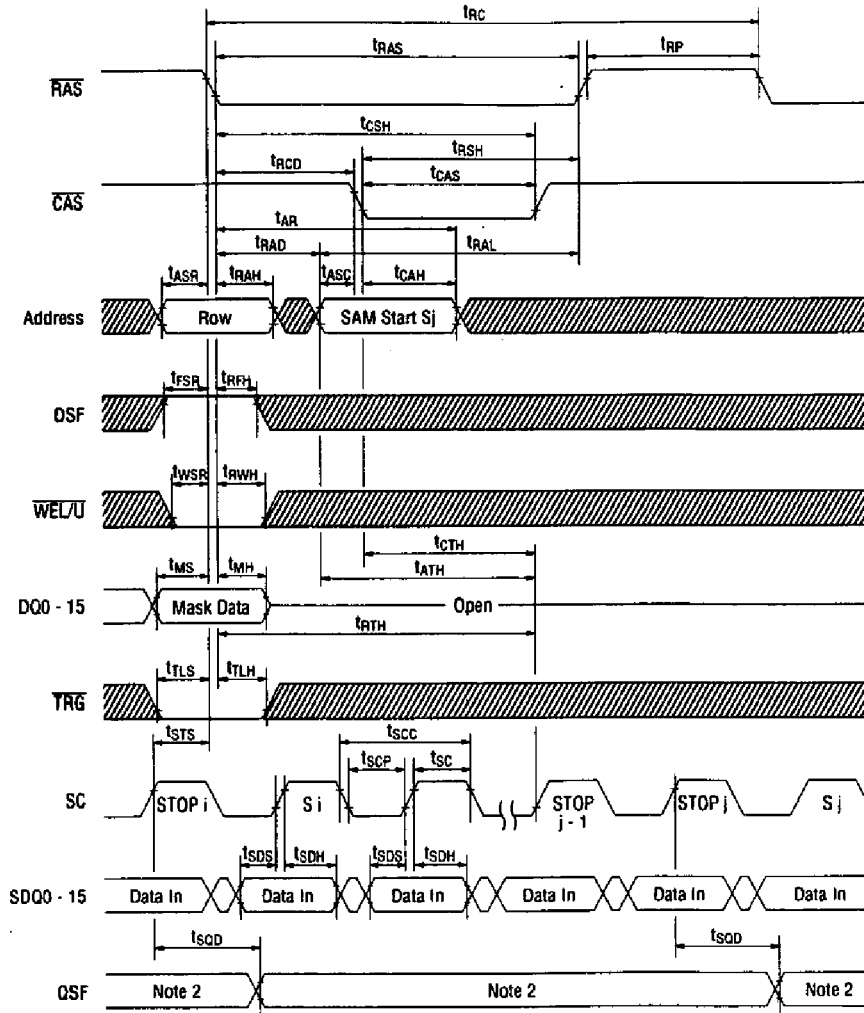
- Note 1:**  $\overline{SE} = "L"$
- Note 2:** QSF = "L"-- Lower SAM (0 - 255) is active  
QSF = "H"-- Upper SAM (256 - 511) is active
- Note 3:**  $S_i$  is the SAM start address in before SRT
- Note 4:** STOP  $i$  and STOP  $j$  are programmable stop address

**Masked Write Transfer**



- Note 1:**  $\overline{SE} = "L"$
- Note 2:** There must be no rising transitions
- Note 3:** QSF = "L"-- Lower SAM (0 - 255) is active  
QSF = "H"-- Upper SAM (256 - 511) is active

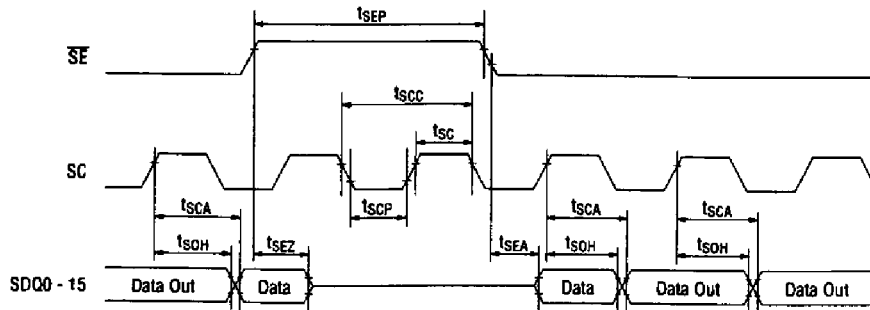
**Masked Split Write Transfer**



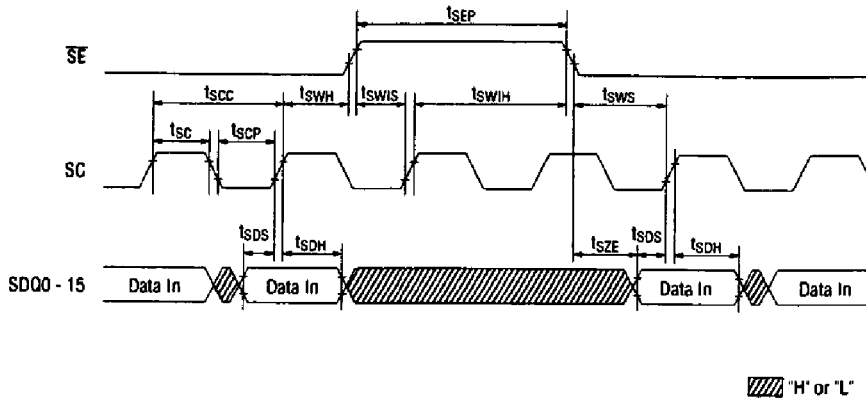
▨ 'H' or 'L'

- Note 1:**  $\overline{SE} = "L"$
- Note 2:** QSF = "L"-- Lower SAM (0 - 255) is active  
QSF = "H"-- Upper SAM (256 - 511) is active
- Note 3:**  $S_i$  is the SAM start address in before SWT
- Note 4:** STOP  $i$  and STOP  $j$  are programmable stop address

Serial Read Cycle



Serial Write Cycle



## PIN FUNCTION

### Address Input: A0 - A8

The 18 address bits decodes 16-bit of the 4,194,304 locations in the MSM5416263 memory array. The address bits are multiplexed to 9 address input pins (A0 - A8) as standard DRAM. 9 row address bits are latched at the falling edge of  $\overline{\text{RAS}}$ . The following 9 column address bits are latched at the falling edge of  $\overline{\text{CAS}}$ .

### Row Address Strobe: $\overline{\text{RAS}}$

$\overline{\text{RAS}}$  is a basic RAM control signal. The RAM port is in standby mode when the  $\overline{\text{RAS}}$  level is "high". As the standard DRAM's  $\overline{\text{RAS}}$  signal function,  $\overline{\text{RAS}}$  is the control input that latches the row address bits and a random access cycle begin at the falling edge of  $\overline{\text{RAS}}$ .

In addition to the conventional  $\overline{\text{RAS}}$  signal function, the level of the input signals,  $\overline{\text{CAS}}$ ,  $\overline{\text{TRG}}$ ,  $\overline{\text{WEL}}$ ,  $\overline{\text{WEU}}$  and DSF at the falling edge of  $\overline{\text{RAS}}$ , determines the MSM5416263 operation modes.

### Column Address Strobe: $\overline{\text{CAS}}$

As the standard DRAM's  $\overline{\text{CAS}}$  signal function,  $\overline{\text{CAS}}$  is the control input signal that latches the column address input and the state of the special function input DSF to select, in conjunction with the  $\overline{\text{RAS}}$  control, either read/write operations or the special block write feature on the RAM port when the DSF is held "low" at the falling edge of  $\overline{\text{RAS}}$ .

$\overline{\text{CAS}}$  also acts as a RAM port output enable signal.

### Data Transfer, Output Enable: $\overline{\text{TRG}}$

$\overline{\text{TRG}}$  is also a control input signal having multifunction. As the standard DRAM's  $\overline{\text{OE}}$  signal function,  $\overline{\text{TRG}}$  is used as an output enable control when  $\overline{\text{TRG}}$  is "high" at the falling edge of  $\overline{\text{RAS}}$ . In addition to the conventional  $\overline{\text{OE}}$  signal function, a data transfer operation is started between the RAM port and the SAM port when  $\overline{\text{TRG}}$  is "low" at the falling edge of  $\overline{\text{RAS}}$ .

### Write Per Bit, Write Enable: $\overline{\text{WEL}}$ and $\overline{\text{WEU}}$

$\overline{\text{WEL}}$ ,  $\overline{\text{WEU}}$  are control input signals having multifunction. As the standard DRAM's  $\overline{\text{WE}}$  signal function, these are used to write data into the memory on the RAM port when  $\overline{\text{WEL}}$  and  $\overline{\text{WEU}}$  are both "high" at the falling edge of  $\overline{\text{RAS}}$ .

In addition to the conventional  $\overline{\text{WE}}$  signal function, the  $\overline{\text{WEL}}$ ,  $\overline{\text{WEU}}$  determine the write-per-bit function when either  $\overline{\text{WEL}}$  or  $\overline{\text{WEU}}$  is "low" at the falling edge of  $\overline{\text{RAS}}$ , during RAM port operations.

The  $\overline{\text{WEL}}$  and  $\overline{\text{WEU}}$  also determine the direction of data transfer between the RAM and SAM. When both  $\overline{\text{WEL}}$  and  $\overline{\text{WEU}}$  are "high" at the falling edge of  $\overline{\text{RAS}}$ , the data is transferred from RAM to SAM (read transfer). When either  $\overline{\text{WEL}}$  or  $\overline{\text{WEU}}$  is "low" at the falling edge of  $\overline{\text{RAS}}$ , the data is transferred SAM to RAM (write transfer).

**Write Mask Data, Data Input and Output: DQ0 - DQ15**

In conventional write-per bit mode, DQ pins function as mask data at the falling edge of  $\overline{RAS}$ . Data are written only to high DQ pins. Data on low DQ pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM. In persistent write-per-bit mode, DQ pins are don't care at the falling edge of  $\overline{RAS}$ . The mask data are determined in the mask register load cycle.

**Serial Clock: SC**

SC is a main serial cycle control input signal. All operations of SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read cycle, the output data becomes valid on the SDQ pins after the maximum specified serial access time  $t_{SCA}$  from the rising edge of SC. In a serial write cycle, data on SDQ pins at the rising edge of SC are fetched into the SAM register.

**Serial Enable:  $\overline{SE}$** 

The  $\overline{SE}$  is a serial access enable control and serial read/write control signal. In a serial read cycle,  $\overline{SE}$  is used as an output control. In a serial write cycle,  $\overline{SE}$  is used as a write enable control. When  $\overline{SE}$  is "high", serial access is disable, however, the serial address pointer location is still incremented when SC is clocked even when  $\overline{SE}$  is "high".

**Special Function Input: DSF**

The DSF is latched at the falling edge of  $\overline{RAS}$  and  $\overline{CAS}$  and allows for the selection of several RAM port and transfer operating modes. In addition to the conventional multiport DRAM, the special function consisting of flash write, block write, load/read color register and split read/write transfer can be invoked.

**Special Function Output: QSF**

QSF is an output signal which, during split register mode, indicates which half of the split SAM is being accessed. QSF "low" indicates that the lower split SAM (0 - 255) is being accessed. QSF "high" indicates that the upper SAM (256 - 511) is being accessed.

**Serial Input/Output: SDQ0 - SDQ15**

Serial input/output mode is determined by the most recent read, write or pseudo write transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a write or pseudo write transfer cycle is performed, the SAM port is switched from output mode to input mode.

## OPERATION MODE

The Table-1 shows the function truth table for a listing of all available RAM port and transfer operation of MSM5416263.

The RAM port and data transfer operating are determined by the state of  $\overline{\text{CAS}}$ , TRG,  $\overline{\text{WE}}$ , and DSF at the falling edge of  $\overline{\text{RAS}}$  and by the state of DSF at the falling edge of  $\overline{\text{CAS}}$ .

Table-1. Function Truth Table

Code	$\overline{\text{RAS}}\downarrow$				$\overline{\text{CAS}}\downarrow$	Address			W/O		Write Mask	Pers. W.M.	Register		Function
	$\overline{\text{CAS}}$	TRG	$\overline{\text{WE}}$	DSF	DSF	$\overline{\text{RAS}}\downarrow$	$\overline{\text{CAS}}\downarrow$	$\overline{\text{RAS}}\downarrow$	$\overline{\text{CAS}}\downarrow$ ( $\overline{\text{WE}}\downarrow$ )	WM			Color		
CBRR	0	*	1	0	—	*	*	*	*	—	Reset	Reset	—	CBR Refresh with Register Reset	
CBRS	0	*	0	1	—	STOP	*	*	*	—	—	—	—	CBR Refresh with Stop Register Set	
CBRN	0	*	1	1	—	*	*	*	*	—	—	—	—	CBR Refresh (No Reset)	
ROR	1	1	*	0	—	Row	—	*	—	—	—	—	—	RAS Only Refresh	
MWT	1	0	0	0	*	Row	TAP	WM1	*	Yes	No/Yes	Load Use	—	Masked Write Transfer	
MSWT	1	0	0	1	*	Row	TAP	WM1	*	Yes	No/Yes	Load Use	—	Masked Split Write Transfer	
RT	1	0	1	0	*	Row	TAP	*	*	—	—	—	—	Read Transfer	
SRT	1	0	1	1	*	Row	TAP	*	*	—	—	—	—	Split Read Transfer	
RWM	1	1	0	0	0	Row	Column	WM1	Din, Dout	Yes	No/Yes	Load Use	—	Read/Write (New/Old Mask)	
BWM	1	1	0	0	1	Row	Column A3c - 8c	WM1	Column Select	Yes	No/Yes	Load Use	Use	Masked Block Write (New/Old)	
FWM	1	1	0	1	*	Row	*	WM1	—	Yes	No/Yes	Load Use	Use	Masked Flash Write (New/Old)	
RW	1	1	1	0	0	Row	Column	*	Din, Dout	No	No	—	—	Read/Write (No Mask)	
BW	1	1	1	0	1	Row	Column A3c - 8c	*	Column Select	No	No	—	Use	Block Write (No Mask)	
LMR	1	1	1	1	0	Row	*	*	Mask Data	—	Set	Load	—	Load Mask Register (Old Mask Set)	
LCR	1	1	1	1	1	Row	*	*	Color Data	—	—	—	Load	Load Color Register	

- Notes:
1. With CBRS, SAM operations use stop register
  2. After LMR, RWM, BWM, FWM, and MSWT, use old mask which can be reset by

If the DSF is "high" at the falling edge of  $\overline{RAS}$ , special function such as split transfer, flash write, load mask register, load color register, CBRS and CBRN can be invoked.

If the DSF is "low" at the falling edge of  $\overline{RAS}$  and "high" at the falling edge of  $\overline{CAS}$ , the block write feature can be invoked.

### RAM PORT OPERATION

**Extended RAM Read Cycle:**  $\overline{RAS}$  falling edge ---  $\overline{TRG}$ ,  $\overline{CAS} = "H"$ ,  $DSF = "L"$   
 $\overline{CAS}$  falling edge ---  $DSF = "L"$

The MSM5416263 offers an accelerated page mode cycle (EXTENDED PAGE MODE) by eliminating output disable from  $\overline{CAS}$  "high", and it allows  $\overline{CAS}$  precharge time ( $t_{CP}$ ) to occur without the output data going invalid. This new data out operates (Extended data out) as any RAM read or Page Mode Read, except data will be held valid after  $\overline{CAS}$  goes "high", as long as  $\overline{RAS}$  is "low".

**RAM Write Cycle:**  $\overline{RAS}$  falling edge ---  $\overline{TRG}$ ,  $\overline{CAS} = "H"$ ,  $DSF = "L"$   
 $\overline{CAS}$  falling edge ---  $DSF = "L"$

1) Write cycle with no mask:  $\overline{RAS}$  falling edge --  $\overline{WEL} = \overline{WEU} = "H"$

At the falling edge of  $\overline{CAS}$ , either  $\overline{WEL}$  or  $\overline{WEU}$  is set "low" after  $\overline{RAS}$  goes "low", a write cycle is executed. If either  $\overline{WEL}$  or  $\overline{WEU}$  is set "low" before the  $\overline{CAS}$  falling edge, this cycle becomes an early write cycle and all DQ pins become in high impedance.

If only one of  $\overline{WEL}$  and  $\overline{WEU}$  is "low" when  $\overline{CAS}$  goes "low", the write will affect only those corresponding 8 bits, with the latched data.

If both  $\overline{WEL}$  and  $\overline{WEU}$  are set "low" after the  $\overline{CAS}$  falling edge, this cycle becomes a delayed write cycle and all 16 data are latched on the falling edge of  $\overline{WEL}$  or  $\overline{WEU}$ .

Byte write occurs if only one of  $\overline{WEL}$  or  $\overline{WEU}$  falls during the cycle. DQ pins don't become high impedance in this cycle, so data should be entered with  $\overline{TRG}$  in "high".

2) Write cycle with mask:  $\overline{RAS}$  falling edge --  $\overline{WEL}$  or  $\overline{WEU} = "L"$

At the falling edge of  $\overline{RAS}$ , if  $\overline{WEL}$  or  $\overline{WEU}$  is set "low", two modes of mask write can be invoked.  
 #1 In new mask mode, mask data is loaded and used. Whether or not a DQ is written depends on DQ level at the falling edge of  $\overline{RAS}$ . The data is written in "high" level DQs, and the data is masked and retained in "low" level DQs. This mask data is effective during the  $\overline{RAS}$  cycle. In page mode cycle, the mask data is retained during the page access.

#2 If a load mask register cycle (LMR) has been performed, the mask data is not loaded from DQ pins and the mask data stored in mask register persistently are used.

This operation is known as persistent write mask, set by LMR and reset by CBRR.

**Load/Read Color Register:**  $\overline{RAS}$  falling edge ---  $\overline{CAS} = \overline{TRG} = \overline{WEL} = \overline{WEU} = DSF = "H"$   
 $\overline{CAS}$  falling edge ---  $DSF = "H"$

The MSM5416263 is provided with an on-chip 16bits color register for use during the flash write or block write operation. Each bit of the color register corresponds to one of the DRAM I/O blocks.

The data presented on the DQ<sub>i</sub> lines is subsequently latched into the color register at the falling edge of either  $\overline{CAS}$  or  $\overline{WE}$  whichever occurs later.

The read color register cycle is activated by holding  $\overline{WE}$  "high" at the falling edge of  $\overline{CAS}$  and throughout the remainder of the cycle. The data in the color register becomes valid on the  $DQ_i$  lines after the specified access times from  $\overline{RAS}$  and  $\overline{TRG}$  are satisfied. During the load/read color register cycle, the memory cells on the row address latched at the falling edge of  $\overline{RAS}$  are refreshed.

**Load/Read Mask Register:**  $\overline{RAS}$  falling edge ---  $\overline{CAS} = \overline{TRG} = \overline{WEL} = \overline{WEU} = \overline{DSF} = "H"$   
 $\overline{CAS}$  falling edge ---  $\overline{DSF} = "L"$

The MSM5416263 is provided with an on-chip 16bits mask register for use during the mask write cycle, flash write cycle, block write cycle, masked write transfer and masked split write transfer. Each bit of the mask register corresponds to one of the DRAM I/O blocks. The data presented on the  $DQ_i$  lines is subsequently latched into the mask register at the falling edge of either  $\overline{CAS}$  or  $\overline{WE}$  whichever occurs later.

The read mask register cycle is activated by holding  $\overline{WE}$  "high" at the falling edge of  $\overline{CAS}$  and throughout the remainder of the cycle. The data in the mask register becomes valid on the  $DQ_i$  lines after the specified access times from  $\overline{RAS}$  and  $\overline{TRG}$  are satisfied. During the load/read mask register cycle, the memory cells on the row address latched at the falling edge of  $\overline{RAS}$  are refreshed.

**Flash Write:**  $\overline{RAS}$  falling edge ---  $\overline{CAS} = \overline{TRG} = \overline{DSF} = "H"$ ,  $\overline{WEL} = \overline{WEU} = "L"$

Flash write allows for the data in the color register to be written into all the memory locations of a selected row.

Each bit of the color register corresponds to one of the DRAM I/O block and the flash write operation can be selectively controlled on an I/O basis in the same manner as the write per bit operation. The mask data is as same as that of a RAM write cycle.

**Block Write:**  $\overline{RAS}$  falling edge ---  $\overline{CAS} = \overline{TRG} = "H"$ ,  $\overline{DSF} = "L"$   
 $\overline{CAS}$  falling edge ---  $\overline{DSF} = "H"$ ,  $\overline{WEL} = \overline{WEU} = "L"$

Block write allows for the data in the color register to be written into 4 consecutive column address locations starting from a selected column address in a selected row.

The block write operation can be selectively controlled on an I/O basis and a column mask capability is also available. This function is implemented as (4 columns  $\times$  4 IOs) repeated in four quadrants. During a block write cycle, the 2 least significant column address locations (A0C, A1C) are internally controlled and only the 7 most significant column address (A2C - A8C) are latched at the falling edge of  $\overline{CAS}$ .

- 1) No mask block write:  $\overline{WEL}$  and  $\overline{WEU}$  "high" at the falling edge of  $\overline{RAS}$   
 The data on 16 DQ pins are all cleared by data of color register.
- 2) Masked block write:  $\overline{WEL}$  or  $\overline{WEU}$  "low" at the falling edge of  $\overline{RAS}$   
 The mask data is the same as that of a RAM write cycle. (new mask and persistent mask)

## SAM PORT OPERATION

### Single Register Mode

High speed serial read or write operation can be performed through the SAM port independent of the RAM port operation, except during read/write transfer cycles.

The preceding transfer operation determines the direction of data flow through the SAM port. If the preceding transfer is a read transfer, the SAM port is in the output mode. If the preceding transfer is write transfer, the SAM port is in the input mode.

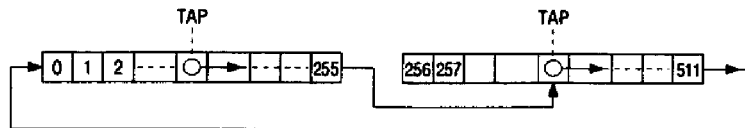
Serial data can be read out of the SAM after a read transfer has been performed. The data is shifted out of the SAM starting at any of the 512 bits locations.

The TAP location corresponds to the column address selected at the falling edge of  $\overline{\text{CAS}}$  during the read or write transfer cycle. The SAM registers are configured as circular data register. The data is shifted out sequentially starting from the selected TAP location to the most significant bit (511) and then wraps around to the least significant bit (0).

### Split Register Mode

In split register mode, data can be shifted into or out of one half of the SAM while a split read or split write transfer is being performed on the other half of the SAM.

Conventional (non split) read, or write transfer cycle must precede any split read or split write transfers. The split read and write transfers will not change the SAM port mode set by preceding conventional transfer operation. In the split register mode, serial data can be shifted in or out of one of the split SAM registers starting from any at the 256 TAP locations, excluding the last address of each split SAM, data is shifted in or out sequentially starting from the selected TAP location to the most significant bit (255 or 511) of the first split SAM and then the SAM pointer moves to the TAP location selected for the second split SAM to shift data in or out sequentially starting from this TAP location to the most significant bit (511 or 255) and finally wraps around to the least significant bit.



## DATA TRANSFER OPERATION

The MSM5416263 features two types of bidirectional data transfer capability between RAM and SAM, as shown in Figure 1 below.

- 1) Conventional (non split) transfer: 512 words by 16 bits of data can be loaded from RAM to SAM (Read transfer) or from SAM to RAM (Write transfer).
- 2) Split transfer: 256 words by 16 bits of data can be loaded from the lower/upper half of the RAM to the lower/upper half of the SAM (Split read transfer) or from the lower/upper half of SAM to the lower/upper half of RAM (Split write transfer).

The conventional transfer and split transfer modes are controlled by the DSF input signal.

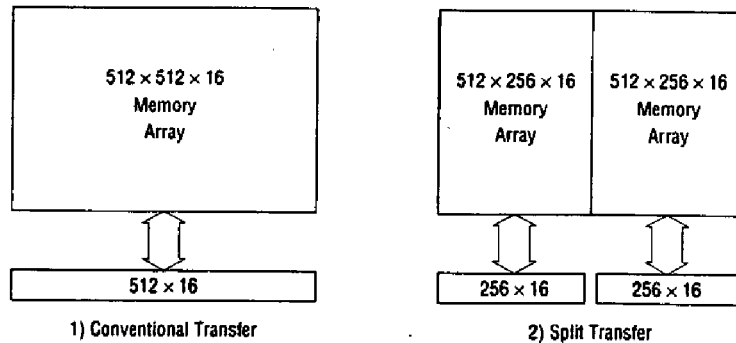


Figure 1.

The MSM5416263 supports 4 types of transfer operation: Read transfer, Split read transfer, Write transfer and Split write transfer as shown in truth table. Data transfer are invoked by holding the  $\overline{\text{TRG}}$  signal "low" at the falling edge of  $\overline{\text{RAS}}$ . The type of transfer operation is determined by the state of  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$  and  $\text{DSF}$  latched at the falling edge of  $\overline{\text{RAS}}$ . During conventional transfer operations, the SAM port is switched from input to output mode (Read transfer) or output to input mode (Write transfer) whereas it remains unchanged during split transfer operation (Split read transfer or Split write transfer).

**Read Transfer:**  $\overline{\text{RAS}}$  falling edge ---  $\overline{\text{CAS}} = \overline{\text{WEL}} = \overline{\text{WEU}} = \text{"H"}$ ,  $\overline{\text{TRG}} = \text{DSF} = \text{"L"}$

Read transfer consists of loading a selected row of data from the RAM into the SAM register. A read transfer is invoked by holding  $\overline{\text{CAS}}$  "high",  $\overline{\text{TRG}}$  "low",  $\overline{\text{WEL}}$  and  $\overline{\text{WEU}}$  "high" and  $\text{DSF}$  "low" at the falling edge of  $\overline{\text{RAS}}$ . The row address selected at the falling edge of  $\overline{\text{RAS}}$  determines the RAM row to be transferred into the SAM. The transfer cycle is completed at the rising edge of  $\overline{\text{TRG}}$ . When the transfer is completed, the SAM port is set into the output mode. In a read/real time read transfer cycle, the transfer of a new row of data is completed at the rising edge of  $\overline{\text{TRG}}$  and this data becomes valid on the SDQ lines after the specified access time  $t_{\text{SCA}}$  from the rising edge of the subsequent SC cycles. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of  $\overline{\text{CAS}}$ . In a read transfer cycle (which is preceded by a write transfer cycle), SC clock must be held at a constant  $V_{\text{IL}}$  or  $V_{\text{IH}}$  after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay  $t_{\text{SDP}}$  from the rising edge of  $\overline{\text{TRG}}$ .

In a real time read transfer cycle (which is preceded by another read transfer cycle), the previous row data appears on the SDQ lines until the  $\overline{\text{TRG}}$  signal goes "high" and the serial access time  $t_{\text{SCA}}$  for the following serial clock is satisfied. This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed without any timing loss. To make this continuous data flow possible, the rising edge of  $\overline{\text{TRG}}$  must be synchronized with  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$  and the subsequent rising edge of SC ( $t_{\text{RTH}}$ ,  $t_{\text{CTH}}$ , and  $t_{\text{TSL}}/t_{\text{TSD}}$  must be satisfied).

**Masked Write Transfer:  $\overline{\text{RAS}}$  falling edge ---  $\overline{\text{CAS}} = \text{"H"}$ ,  $\overline{\text{TRG}} = \text{DSF} = \text{"L"}$   
 $\overline{\text{WEL}}$  or  $\overline{\text{WEU}} = \text{"L"}$**

Write transfer cycle consist of loading the content of the SAM register into a selected row of the RAM. This write transfer is the same as a mask write operation in RAM, so new and persistent (old) mask mode can be supported. (Masked write transfer)

If the SAM data to be transferred must first be loaded through the SAM, a Masked write transfer operation (all DQ pins "low" at falling edge of  $\overline{\text{RAS}}$ ) must precede the write transfer cycles. A masked write transfer is invoked by holding  $\overline{\text{CAS}}$  "high",  $\overline{\text{TRG}}$  "low",  $\overline{\text{WEL}}$  or  $\overline{\text{WEU}}$  "low" and DSF "low" at the falling edge of  $\overline{\text{RAS}}$ . The row address selected at the falling edge of  $\overline{\text{RAS}}$  determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of  $\overline{\text{CAS}}$  determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SDQ lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.

When consecutive write transfer operation are performed, new data must not be written into the serial register until the  $\overline{\text{RAS}}$  cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant  $V_{\text{IL}}$  or  $V_{\text{IH}}$  during the  $\overline{\text{RAS}}$  cycle. A rising edge of the SC clock is only allowed after the specified delay  $t_{\text{CSD}}$  from the falling edge of the  $\overline{\text{CAS}}$ , at which time a new row of data can be written in the serial register.

Data transferred to SAM by read transfer cycle or split read transfer cycle can be written to other address of RAM by write transfer cycle. However, the address to write data must be the same as that of the read transfer cycle (row address AX8).

#### Split Data Transfer and QSF

The MSM5416263 features a bidirectional split data transfer capability between the RAM and SAM. During split data transfer operation, the serial register is split into two halves which can be controlled independently. Split read or split write transfer operation can be performed to or from one half of the serial register while serial data can be shifted into or out of the other half of the serial register. The most significant column address location (A8C) is controlled internally to determines which half of the serial register will be reloaded from the RAM. QSF is an output in which indicates which half of the serial register is in an active state. QSF changes state when the last SC clock is applied to active split SAM.

**Split Read Transfer:**  $\overline{RAS}$  falling edge ---  $\overline{CAS} = \overline{WEL} = \overline{WEU} = DSF = "H", \overline{TRG} = "L"$

The MSM5416263 supports two types of split register operation.

#1 Normal split register operation

#2 Boundary split register operation using programmable SAM stops described later.

Normal split read transfer consists of loading 256 words by 16bits of data from a selected row of the split RAM into the corresponding non-active split SAM register. Serial data can be shifted out from the other half of the split SAM register simultaneously. During split read transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus eliminating timing restrictions as in the case of real time read transfers. A split read transfer can be performed after a delay of  $t_{ST5}$ , from the change of state of the QSF output, is satisfied. Conventional (non-split) read transfer operation must precede split read transfer cycles.

**Masked Split Write Transfer:**  $\overline{RAS}$  falling edge ---  $\overline{CAS} = DSF = "H", \overline{TRG} = "L"$   
 $\overline{WEL}$  or  $\overline{WEU} = "L"$

Split write transfer consists of loading 256 words by 16bits of data from the non-active split SAM register into a selected row of the corresponding split RAM. Serial data can be shifted into the other half of the split SAM register simultaneously. During split write transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus allowing for real time transfer. This operation is the same as a mask write operation in RAM, so new and persistent mode can be supported.

A split write transfer can be performed after a delay of  $t_{ST5}$ , from the change of state of the QSF output, is satisfied.

A masked write transfer operation must precede split write transfer, the purpose is to switch the SAM port from output mode to input mode and to set the initial TAP location prior to split write transfer operations.

#### Programmable SAM Stops in Split Transfer Cycle

The MSM5416263 has the boundary split register operation using programmable stops. If a CBRS cycle has been performed, split transfer cycle performs the boundary operation.

Figure 2 shows an example of boundary split register (4 stop points). The stop points defines a SAM location at which the access will change from one half of the SAM to the other half (at the TAP address).

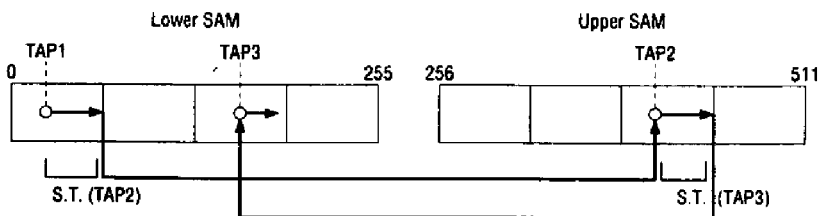


Figure 2. Example of Boundary Split Register

**SAM Stop Set Cycle (CBRS):**  $\overline{RAS}$  falling edge ---  $\overline{CAS} = "L"$ ,  $\overline{WEL} = \overline{WEU} = "L"$ ,  $DSF = "H"$

SAM Stop location data (boundaries) are latched from address inputs at the falling edge of  $\overline{RAS}$ . To determine the boundary, A4 - A7 can be used and don't care A0 - A3, and A8. Once CBRS is executed, the programmable SAM stop operation continues until CBRR.

**SAM Stop Boundary Table**

Number of Stop Points	Address				Size of Partition
	A4	A5	A6	A7	
1	1	1	1	1	256
2	1	1	1	0	128
4	1	1	0	X	64
8	1	0	X	X	32
16	0	X	X	X	16

**Register Reset Cycle (CBRR):**  $\overline{RAS}$  falling edge ---  $\overline{CAS} = "L"$ ,  $\overline{WEL} = \overline{WEU} = "H"$ ,  $DSF = "L"$

A CBRR can reset the programmable SAM stop operation and persistent mask write operation. The CBRR will take effect immediately; it doesn't require a split transfer cycle.

#### POWER UP

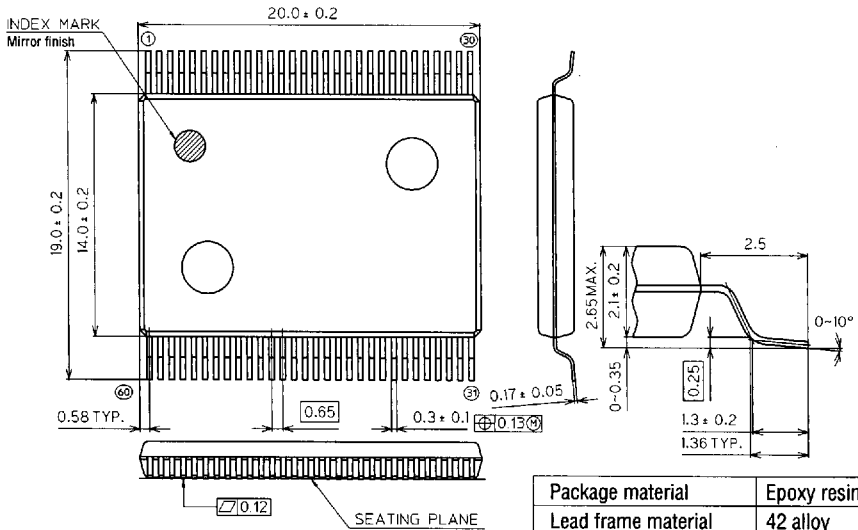
Power must be applied to the  $\overline{RAS}$  and  $\overline{TRG}$  input signals to pull them "high" before or at the same time as the  $V_{CC}$  supply is turned on. After power-up, a pause of 200 $\mu$ s minimum is required with  $\overline{RAS}$  and  $\overline{TRG}$  held "high". After the pause, a minimum of 8  $\overline{RAS}$  and 8 SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the  $\overline{TRG}$  signal must be held "high". If the internal refresh counter is used, a minimum 8  $\overline{CAS}$  before  $\overline{RAS}$  cycles are required instead of 8  $\overline{RAS}$  cycles.

## 2. PACKAGE OUTLINES AND DIMENSIONS

### (1) PLASTIC SOP (cont.)

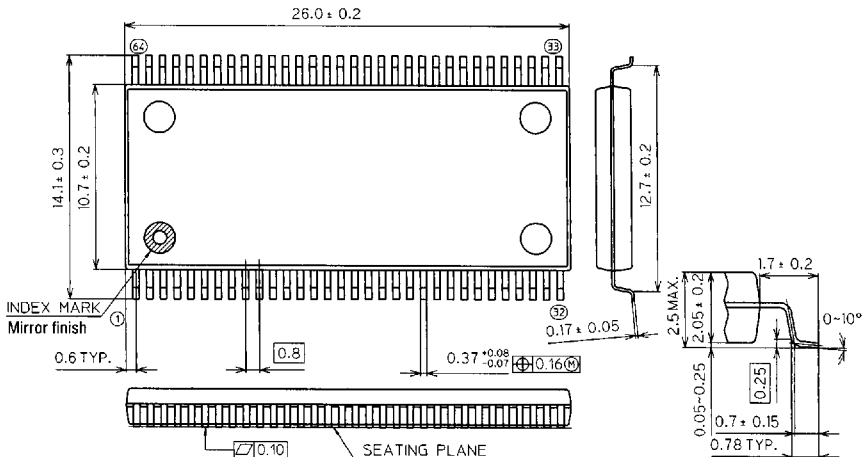
(Unit: mm)

SSOP60-P-700-0.65-L



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 $\mu$ m or more
Package weight (g)	1.21 TYP.

SSOP64-P-525-0.80-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 $\mu$ m or more
Package weight (g)	1.34 TYP.