

To our customers,

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## Old Company Name in Catalogs and Other Documents

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On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

**Phase-out/Discontinued**

## DUAL Pch HIGH-SIDE SWITCH FOR USB

### DESCRIPTION

The μPD16875 is a power switch IC with an overcurrent limiter that is used for the power bus of a Universal Serial Bus (USB). This product has two Pch power MOSFET circuits, each of which has a low-on resistance (100 mΩ TYP.), in its switching block. This product is a low-current-consumption version of the μPD16855B that boasts an operating current consumption of as low as 100 μA (MAX.).

In addition, the IC is also equipped with an overcurrent detector that is essential for a host/hub controller conforming to the USB Standard, so that the IC can report an overcurrent to the controller. Moreover, a thermal shutdown circuit and an undervoltage lockout circuit are also provided as the protection circuits of the IC.

This product has two channels of power switches, control input pins, and flag output pins to simultaneously control two USB ports with a single IC.

### FEATURES

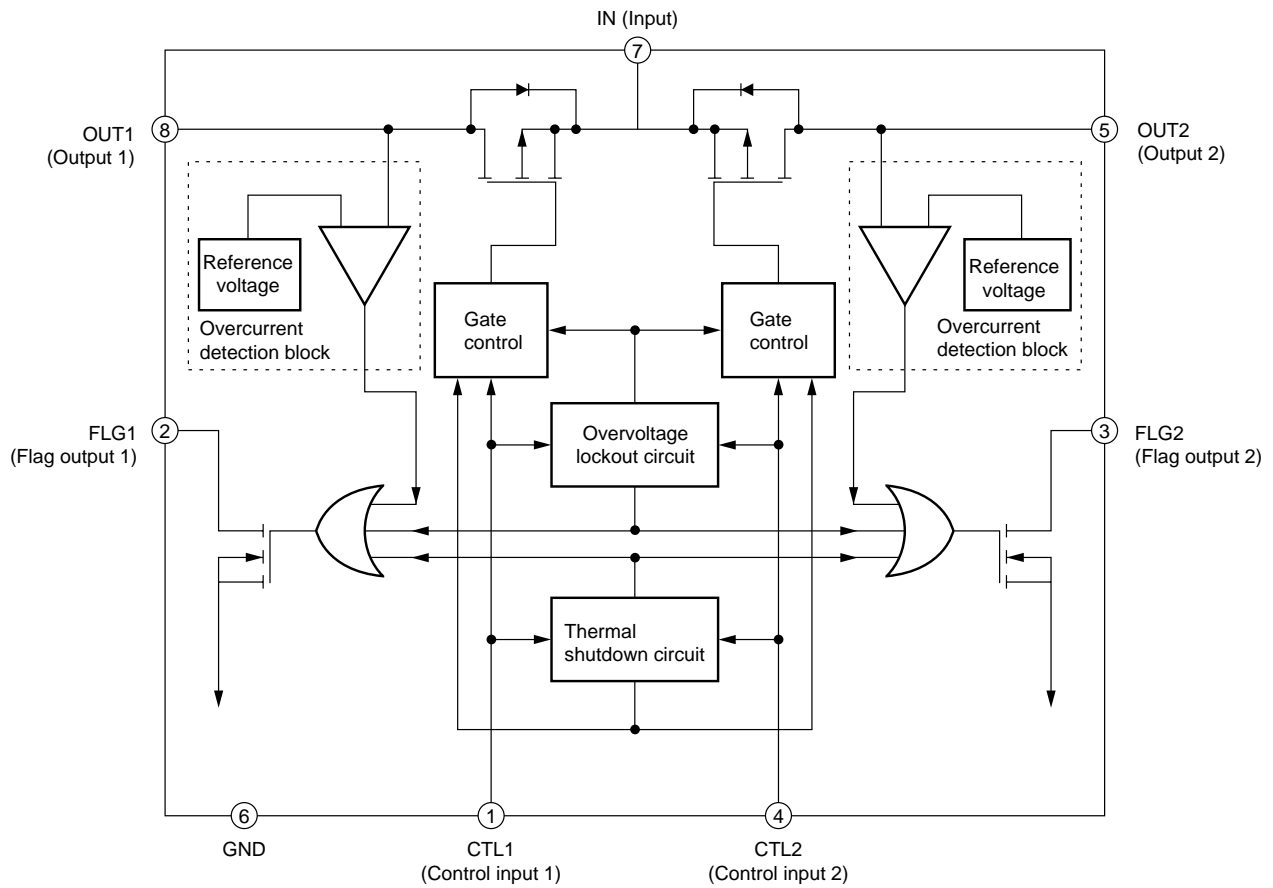
- Two P-ch power MOSFET circuits
- Overcurrent detector that outputs active-low control signal from detection report pin
- Overcurrent limiter to prevent system voltage drop
- Thermal shutdown circuit
- Undervoltage lockout circuit
- Each of two circuits can be turned on and off independently of the others by a control pin.
- 8-pin SOP package

### ORDERING INFORMATION

Part Number	Package
μPD16875G	8-pin SOP (5.72 mm (225))

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.  
 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

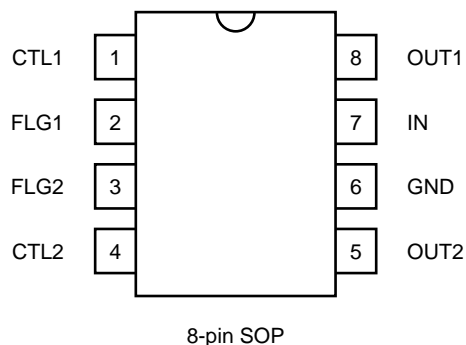
**BLOCK DIAGRAM**



**NOTES ON CORRECT USE**

- No internal resistor is connected to input pins CTL1 (pin 1) and CTL2 (pin 4). When using the  $\mu$ PD16875, therefore, be sure to set the voltage level of these input pins to "H" or "L".

**PIN CONFIGURATION (Top View)**



**PIN DESCRIPTION**

Pin No.	Pin Name	Pin Function
1/4	CTL1/CTL2	Control input: Active-low, TTL input
2/3	FLG1/FLG2	Detection flag (output): Active-low, Nch open-drain
6	GND	Ground
7	IN	Power input: Source of MOSFET for output. Power supply to internal circuitry of IC
8/5	OUT1/OUT2	Switch output: Drain of MOSFET for output. Usually, connected to load.

**TRUTH TABLE (H: High level, L: Low level, ON: Output on, OFF: Output off, X: H or L)**

CTL1 (In)	FLG1 (Out)	OUT1 (Out)	CTL2 (In)	FLG2 (Out)	OUT2 (Out)	Operation mode
L	H	ON	L	H	ON	Normal operation
L	H	ON	H	H	OFF	Only OUT1 is on.
H	H	OFF	L	H	ON	Only OUT2 is on.
H	H	OFF	H	H	OFF	Standby mode
L	L	ON	L	H	ON	Overcurrent detection only for OUT1
L	H	ON	L	L	ON	Overcurrent detection only for OUT2
X	L	OFF	X	L	OFF	Thermal shutdown circuit operation
X	L	OFF	X	L	OFF	Undervoltage lockout circuit operation

**ABSOLUTE MAXIMUM RATINGS (Unless otherwise specified, T<sub>A</sub> = 25°C)**

Parameter	Symbol	Conditions	Ratings	Unit
Input voltage	V <sub>IN</sub>		-0.3 to +6	V
Flag voltage	V <sub>FLG</sub>		-0.3 to +6	V
Flag current	I <sub>FLG</sub>		50	mA
Output voltage	V <sub>OUT</sub>		V <sub>IN</sub> +0.3	V
Output current	I <sub>OUT</sub>	DC	+0.5 (V <sub>IN</sub> = V <sub>CTL</sub> = 5 V) -0.1 (V <sub>IN</sub> = 0 V, V <sub>OUT</sub> = 5 V)	A
		Pulse width ≤ Single 100 μs pulse	+3	
Control input	V <sub>CTL</sub>		-0.3 to +6	V
Total power dissipation	P <sub>D</sub>		300	mW
Operating temperature range	T <sub>A</sub>		-40 to +85	°C
Junction temperature <sup>Note</sup>	T <sub>CH MAX</sub>		+150	°C
Storage temperature	T <sub>stg</sub>		-55 to +150	°C

**Note** This product has an internal thermal shutdown circuit (operating temperature: 150°C or higher TYP.)

**RECOMMENDED OPERATING RANGE (Unless otherwise specified, T<sub>A</sub> = 25°C)**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Input voltage	V <sub>IN</sub>	+4		+5.5	V
Operating temperature range	T <sub>A</sub>	0		+70	°C

**ELECTRICAL SPECIFICATIONS**

**DC Characteristics (Unless otherwise specified, V<sub>IN</sub> = +5 V, T<sub>A</sub> = +25°C)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Current consumption	I <sub>DD</sub>	V <sub>CTL</sub> = V <sub>IN</sub> (Both 1 pin & 4 pin), OUT: Open		1	5	μA
		V <sub>CTL</sub> = 0 V, OUT: open			100	μA
Input voltage, low	V <sub>IL</sub>	CTL pin			1.0	V
Input voltage, high	V <sub>IH</sub>	CTL pin	2.0			V
Control input current	I <sub>CTL</sub>	V <sub>CTL</sub> = 0 V		0.01	1	μA
		V <sub>CTL</sub> = V <sub>IN</sub>		0.01	1	μA
Output MOSFET on-resistance	R <sub>ON</sub>	T <sub>A</sub> = 0 to +70°C, I <sub>OUT</sub> = 500 mA		100	140	mΩ
Output leakage current	I <sub>O LEAK</sub>				10	μA
Overcurrent detector threshold	I <sub>TH</sub>	T <sub>A</sub> = 0 to +70°C	0.6	0.9	1.25	A
Flag output resistance	R <sub>ON F</sub>	I <sub>L</sub> = 10 mA		10	25	Ω
Flag leakage current	I <sub>O LEAK F</sub>	V <sub>FLAG</sub> = 5 V		0.01	1	μA
Undervoltage lockout circuit operating voltage	V <sub>UVLO</sub>	V <sub>IN</sub> : When rising	2.2	2.5	2.8	V
		V <sub>IN</sub> : When falling	2.0	2.3	2.6	V
		Hysteresis width	0.05		0.25	V

**ELECTRICAL SPECIFICATIONS**

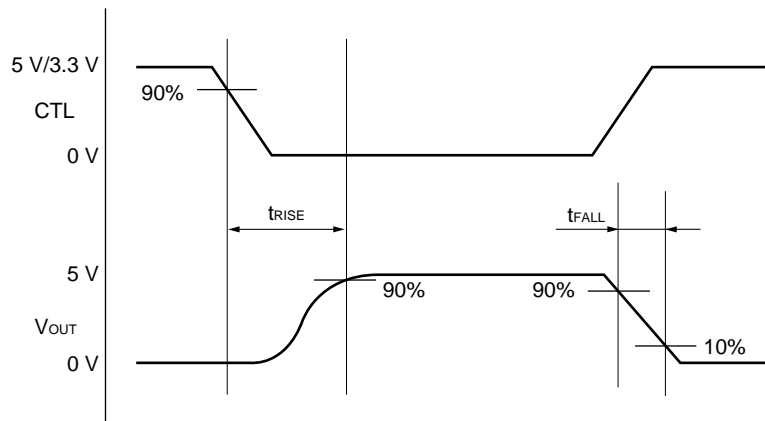
**AC Characteristics (Unless otherwise specified,  $V_{IN} = +5\text{ V}$ ,  $T_A = +25^\circ\text{C}$ )**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output transition rise time (ON)	$t_{RISE}$	$R_L = 10\ \Omega$ per output	2.5	5	8	ms
Output transition fall time (OFF)	$t_{FALL}$	$R_L = 10\ \Omega$ per output			10	$\mu\text{s}$
Overcurrent detection delay time	$t_{OVER}$			20		$\mu\text{s}$
Overcurrent detection output rise time	$t_{SRISE}$	$R_L = 10\ \Omega$ per output	2.5	5	8	ms
Minimum CTL high time	$t_{CTL}$	CTL : L→H→L	20			$\mu\text{s}$

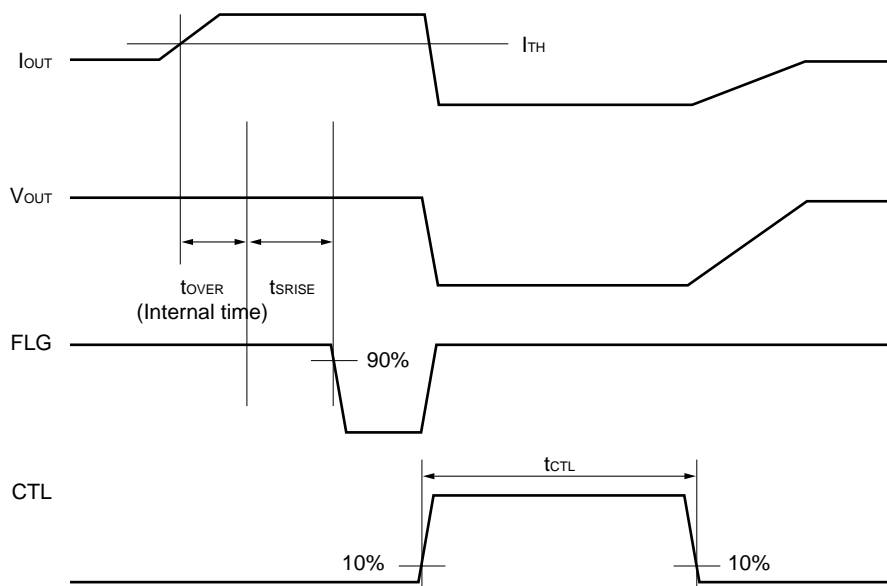
**POINTS OF MEASUREMENT**

**Output Transition Rise Time (ON)/Output Transition Fall Time (OFF)**

CTL pin: H→L/L→H



**Overcurrent Detection Delay Time/Minimum CTL High Time**



**FUNCTIONAL DESCRIPTION REFERENCE TABLE**

Function	Characteristics	Reference Value (TYP.)		Refer to:
Overcurrent detection	Overcurrent detection Threshold	0.9A		p.7 1. Overcurrent detection
	Overcurrent detection delay time	20μs		p.7 1. Overcurrent detection p.10 On Detection of Overcurrent
	Slow-start repeat time	5 ms		p.10 On Detection of Overcurrent
Under voltage lockout circuit (UVLO)	UVLO operating voltage	V <sub>DD</sub> L→H	2.5 V	p.7 2. Under Voltage Lockout Circuit (UVLO)
		V <sub>DD</sub> H→L	2.3 V	
Operation when power is turned on/off	Output rise time	t <sub>RISE</sub>	5 ms	p.8 3. Behavior When Power Is Turned ON/OFF
	Output fall time	t <sub>FALL</sub>	1 μs	
Thermal shutdown circuit	Thermal shutdown circuit operating temperature	150°C or higher		p.11 When Thermal Shutdown Circuit Operates

**DESCRIPTION OF FUNCTIONS**

**1. Overcurrent Detection**

This IC detects an overcurrent in a range of 0.6 to 1.25 A (0.9 A TYP.) (the USB Standard defines that an overcurrent is 0.5 A MAX.). When the IC detects an overcurrent, the FLG pin goes low (active) and reports the result of detection to the control IC. At this time, the switch is kept ON and the current limiter is activated. In this way, an overcurrent status that lasts for a long time can be prevented.

By deasserted the CTL pin inactive by the control IC, the switch is turned OFF and the FLG pin goes back high. Therefore, the CTL signal must be deasserted inactive as soon as the controller IC has detected that the FLG pin has gone low, to avoid overheating this IC. Once the switch has been turned OFF, it turns back ON again only when the CTL signal is asserted active while the FLG pin is high.

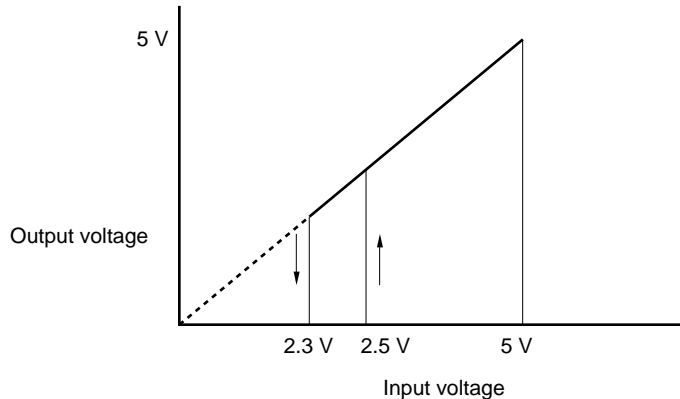
To prevent an inrush current being detected by mistake, a deadband time (overcurrent detection delay time) is set to elapse before the overcurrent detector is activated. The duration of this deadband time is 20 μs TYP.

While the overcurrent limiter is activated, the power consumption of the device may abruptly increase. As a result, the junction temperature may also rise. Make sure that the CTL signal is deasserted inactive and that the switch is turned OFF before the absolute maximum rating is exceeded.

**2. Undervoltage Lockout Circuit (UVLO)**

This circuit prevents malfunctioning of the switch due to fluctuation in supply voltage. When power is turned on (2.5 V or less TYP.) or off (2.3 V or less TYP.), the OUT and FLG pins have the following status:

- OUT: OFF
- FLG: "L" (= 0 V)



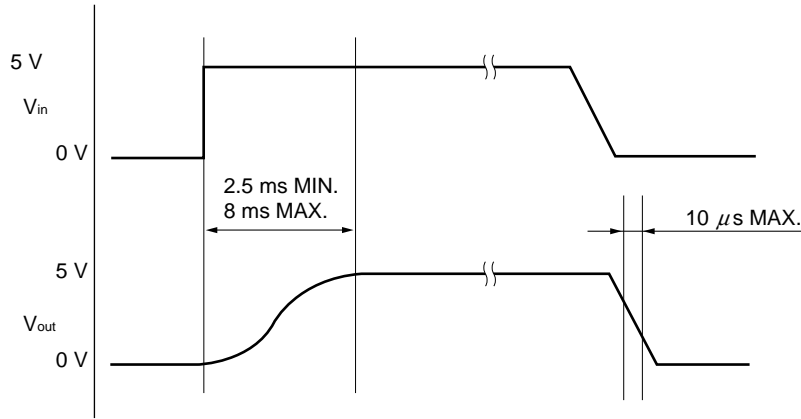
The above figure does not show the actual waveform. For the related characteristic waveform, refer to Major Characteristic Curves.

### 3. Behavior When Power Is Turned ON/OFF

This IC performs a soft-start operation on power application. This is to prevent an overcurrent from flowing through the IC on power application while the high-capacity capacitor connected to the output pin is charged.

Power ON: Soft start (2.5 to 8 ms)

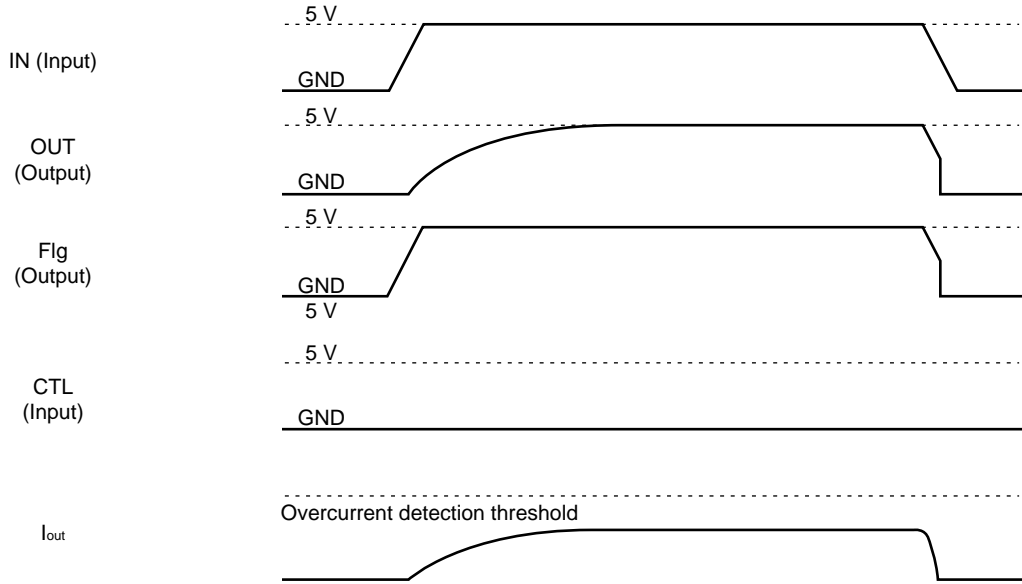
Power OFF: No control (10  $\mu$ s MAX.)



The above figure does not show the actual waveform. For the related characteristic waveform, refer to Major Characteristic Curves.

**OPERATION SEQUENCE**

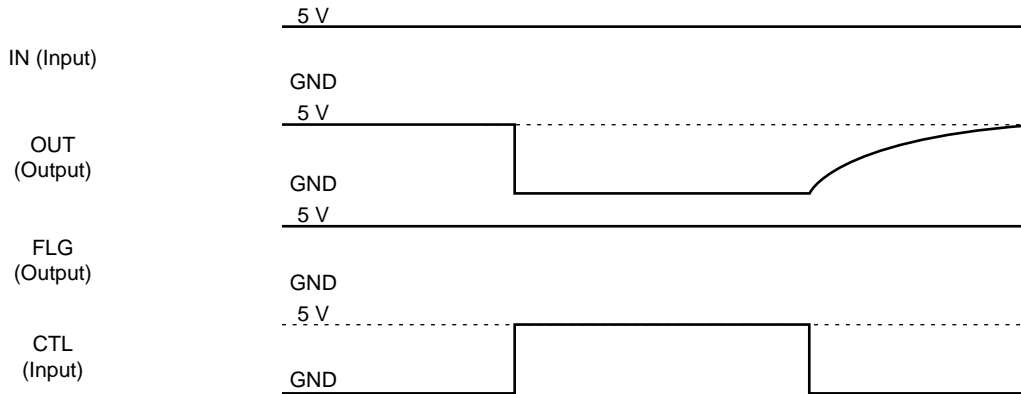
**Power ON/OFF**



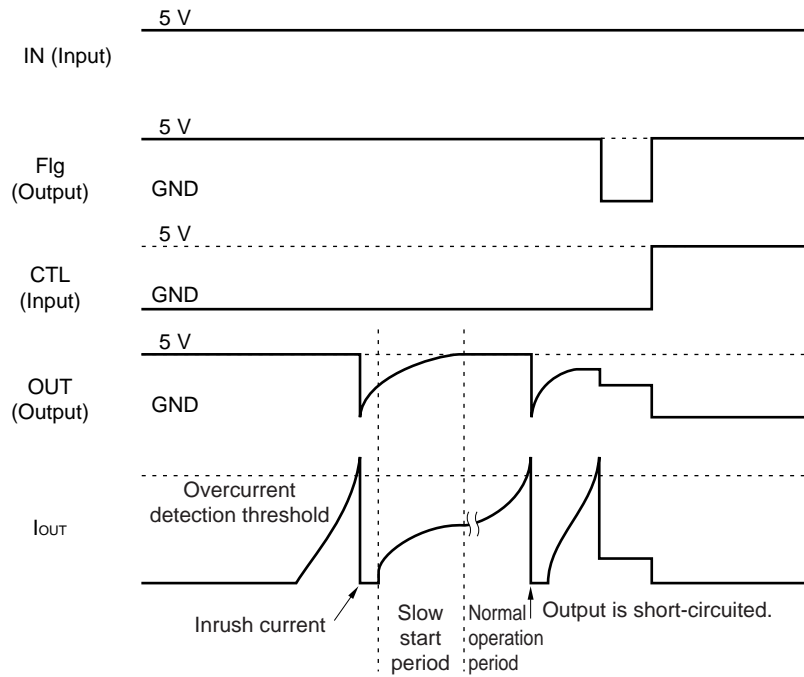
If the CTL signal is asserted active after power has been turned ON, OUT executes the soft-start operation (output transition time: 8 ms MAX.). In addition, FLG output is fixed to “L” if the supply voltage is lower than the operating voltage of the undervoltage lockout circuit (UVLO) on power application.

If all the CTL pins are inactive when power is supplied, the IC enters the standby status (IDD = 5 μA MAX.).

**When Control Signals Are Input**



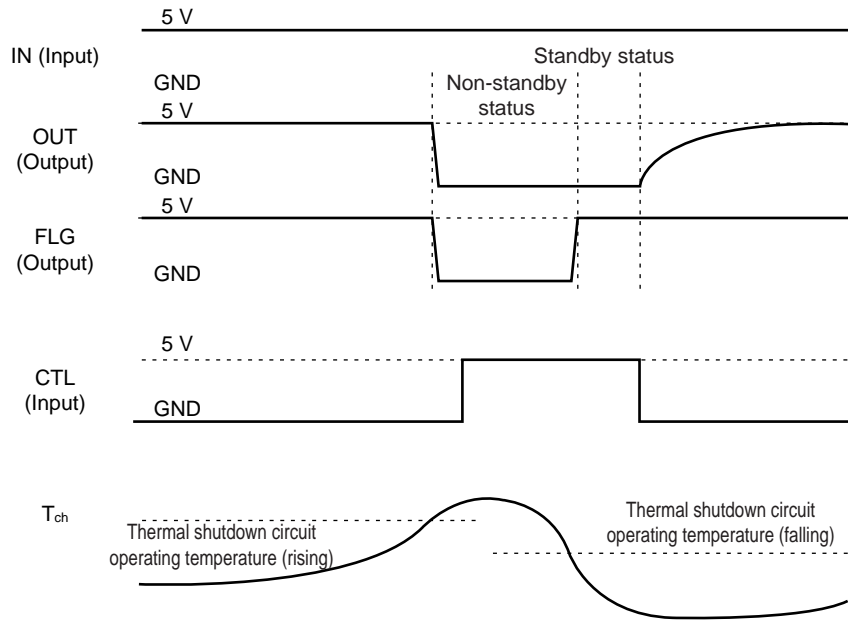
**On Detection of Overcurrent**



If an overcurrent is detected after the overcurrent detection delay time of 20 μs, the IC executes a slow-start operation (output rise time: 5 ms TYP.) again.

If an overcurrent is detected while the IC is executing the slow-start operation again, it is assumed that the output is short-circuited and the FLG pin goes low. When the CTL signal is deasserted inactive, OUT is turned OFF and FLG goes high. If the CTL signal is asserted active, OUT is turned back ON unless the undervoltage lockout circuit or thermal shutdown circuit is activated.

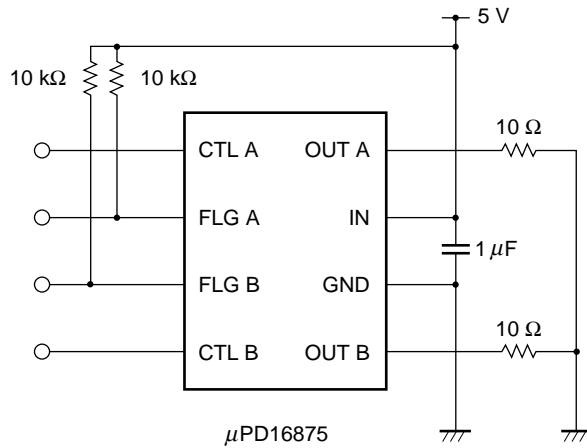
**When Thermal Shutdown Circuit Operates**



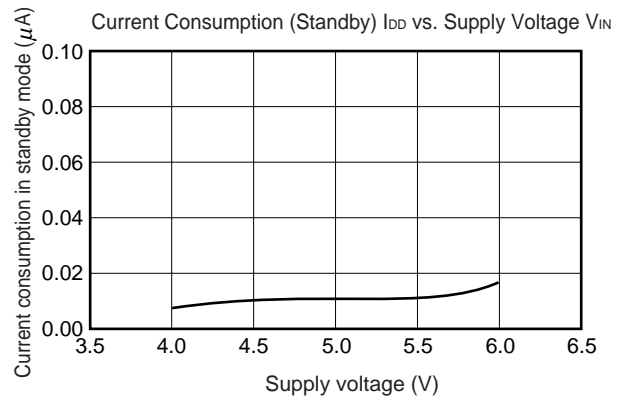
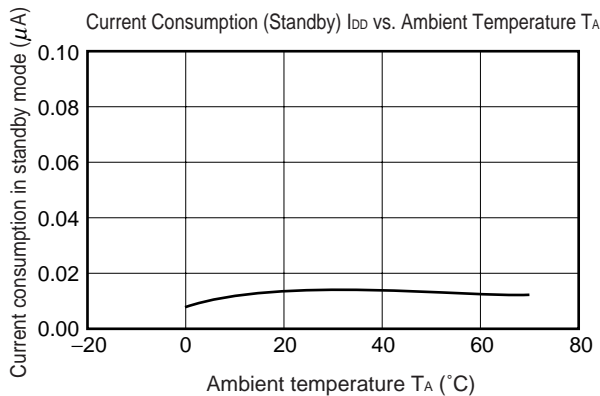
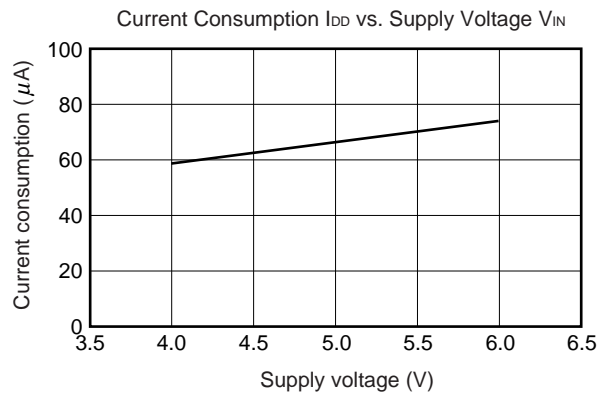
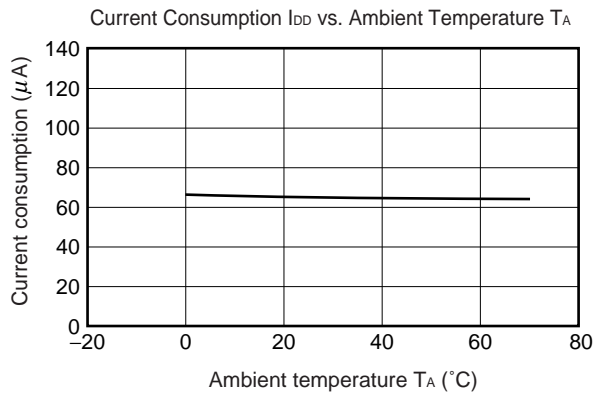
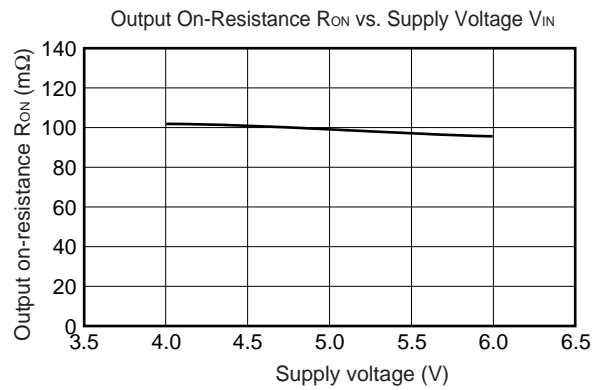
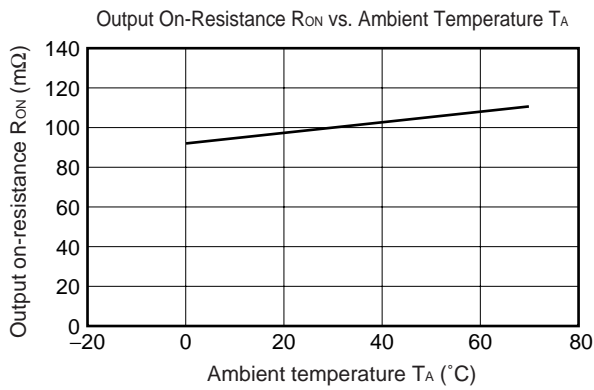
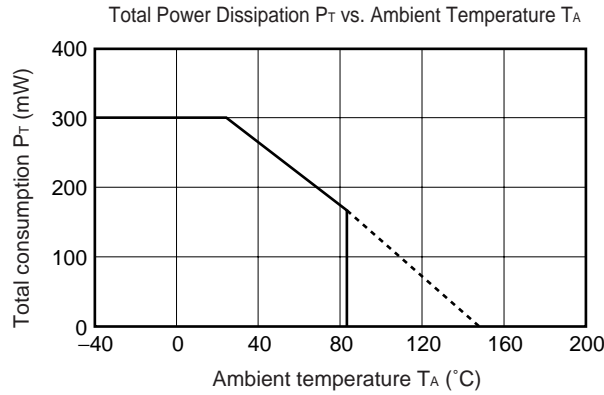
While the thermal shutdown circuit is activated, the output pins are in the OFF status. However, the IC does not enter the standby status even if all the CTL pins are deasserted inactive at the same time.

The thermal shutdown circuit is not activated even if the junction temperature exceeds 150°C TYP. while the IC is in the standby mode (when CTL1 and CTL2 pins are inactive).

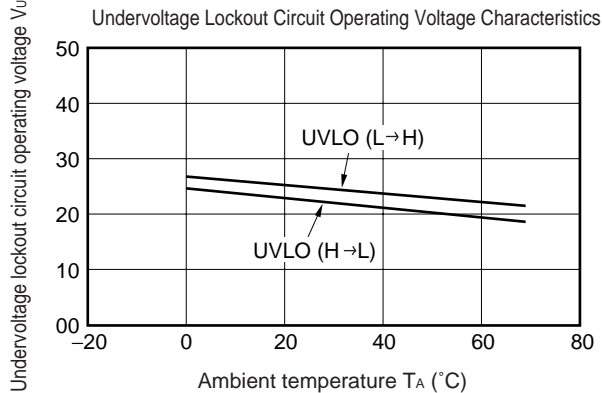
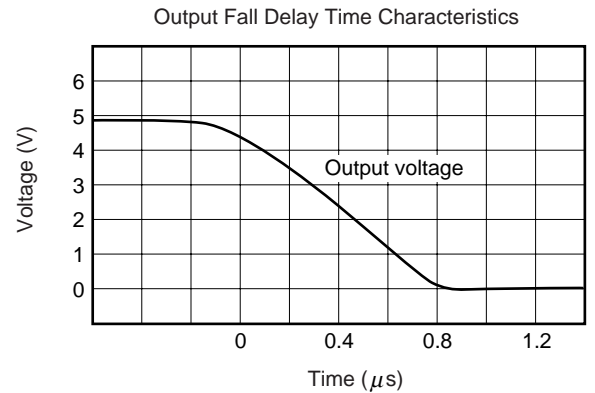
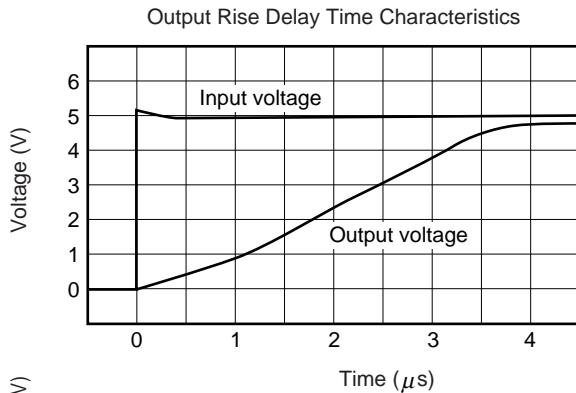
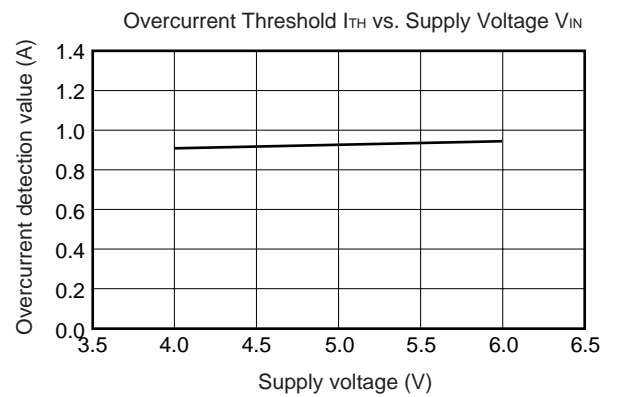
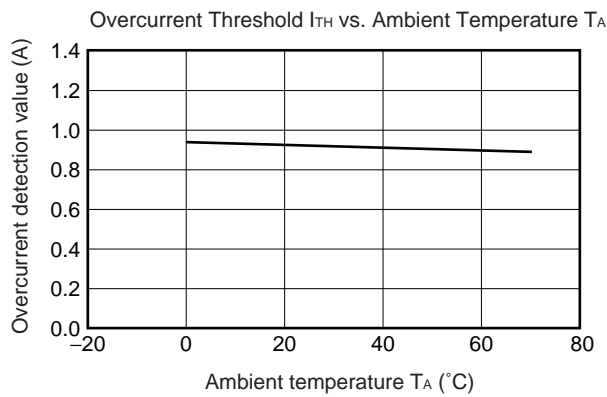
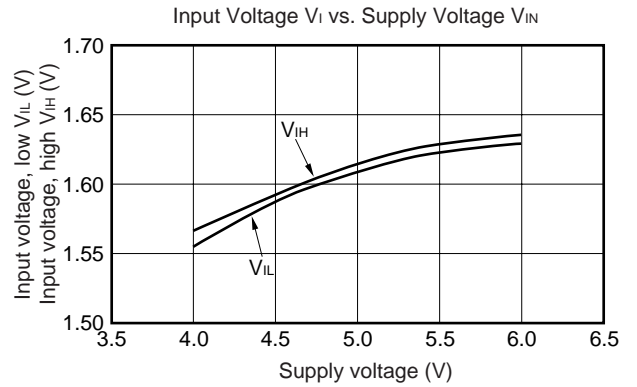
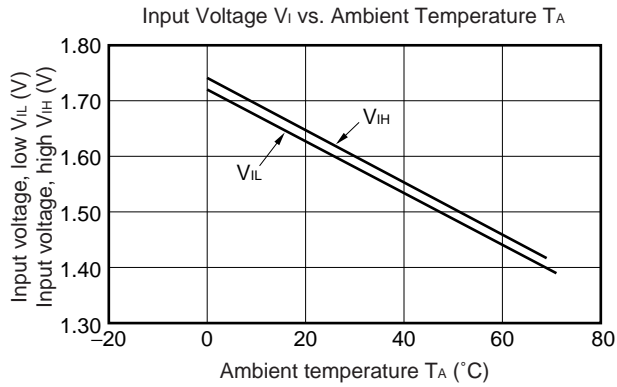
**TEST CIRCUIT**



**MAJOR CHARACTERISTIC CURVES (Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 5\text{ V}$ )**

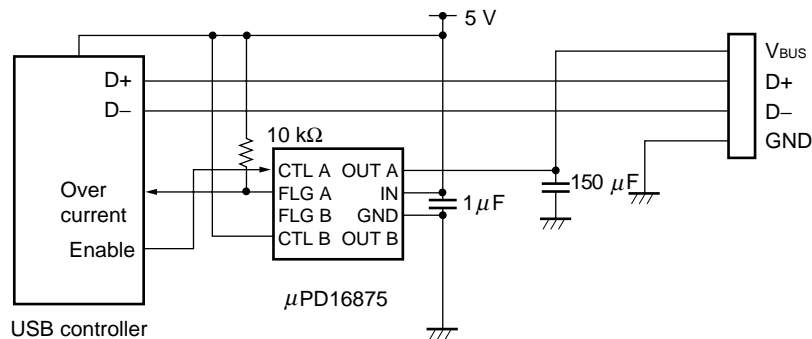


MAJOR CHARACTERISTIC CURVES (Unless otherwise specified,  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 5\text{ V}$ )



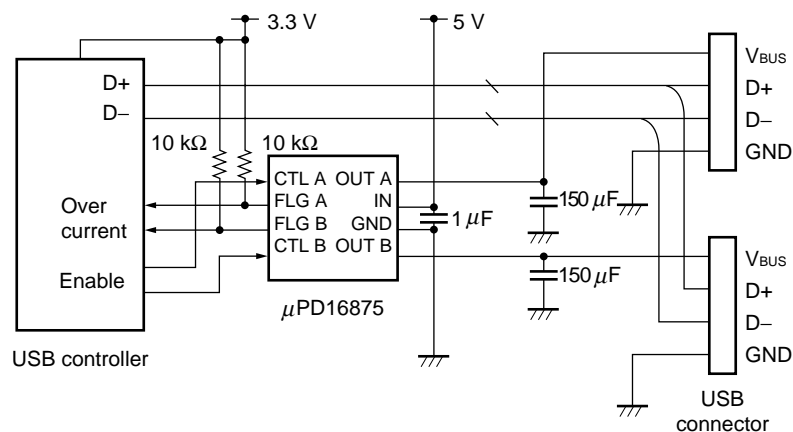
APPLICATION CIRCUIT

Application Circuit 1



USB output port: 1 port  
Controllable by USB controller (CTL input: Active low)

Application Circuit 2

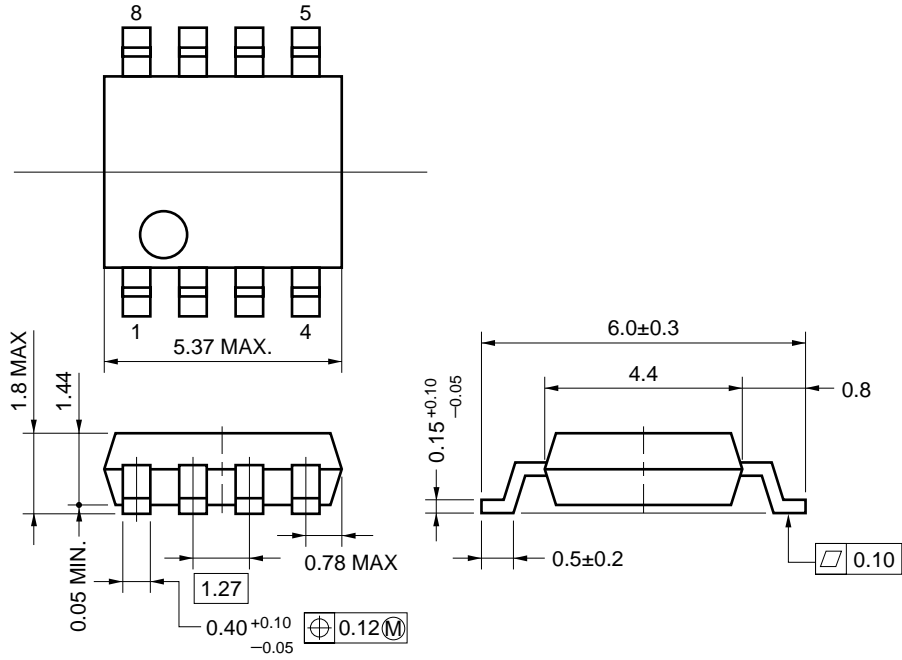


USB output port: 2 ports  
Controllable by USB controller (CTL input: Active low)

The application circuits and their parameters are for references only and are not intended for use in actual designin's.

PACKAGE DRAWING

8-Pin Plastic SOP (5.72 mm (225)) (Unit: mm)



**RECOMMENDED SOLDERING CONDITIONS**

The μPD16875 should be soldered and mounted under the following recommended conditions.  
 For soldering methods and conditions other than those recommended, contact your NEC sales representative.

**Surface Mount Type**

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

**μPD16875G**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: two times, Exposure limit: Not limited <sup>Note</sup>	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: two times, Exposure limit: Not limited <sup>Note</sup>	VP15-00-2
Wave soldering	Solder bath temperature: 260°C Max., Time: 10 sec. Max., Count: once, Exposure limit: not limited <sup>Note</sup>	WS60-00-1
Partial heating	Pin temperature: 300°C Max., Time: 3 sec. Max., Exposure limit: not limited <sup>Note</sup>	—

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

**Cautions** Do not use different soldering methods together (except for partial heating).

**REFERENCE**

Quality Grades on NEC semiconductor Devices	C11531E
Semiconductor Device Mounting Technology Manual	C10535E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Semiconductor Selection Guide	X10679X

[MEMO]

## NOTES FOR CMOS DEVICES

**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

## Regional Information

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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