

December 1996

## Fast CMOS 3.3V 8-Bit Latched Transceiver

### Features

- Advanced 0.6 micron CMOS Technology
- Compatible with LCX™ Families of Products
- Supports 5V Tolerant Mixed Signal Mode Operation
  - Input Can Be 3V or 5V
  - Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Active Bus-Hold Circuitry
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
- Low Ground Bounce Outputs
- Hysteresis on All Inputs

### Ordering Information

| PART NUMBER   | TEMP. RANGE (°C) | PACKAGE    | PKG. NO. |
|---------------|------------------|------------|----------|
| CD74LPT543AM  | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74LPT543AQM | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74LPT543CM  | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74LPT543CQM | -40 to 85        | 24 Ld QSOP | M24.15-P |
| CD74LPT543M   | -40 to 85        | 24 Ld SOIC | M24.3-P  |
| CD74LPT543QM  | -40 to 85        | 24 Ld QSOP | M24.15-P |

NOTE: QSOP is commonly known as SSOP.

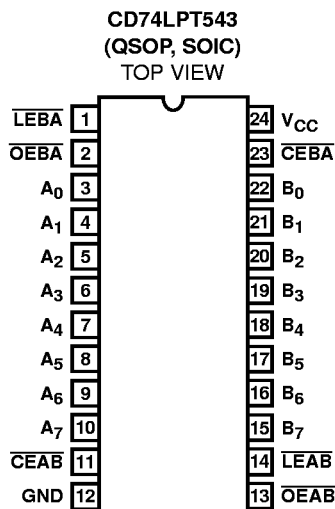
When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

### Description

The CD74LPT543 is an 8-bit wide non-inverting transceiver designed with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ( $\overline{CEAB}$ ) input must be LOW in order to enter data from  $A_0$ - $A_7$  or to take data from  $B_0$ - $B_7$ , as indicated in the Truth Table. With  $\overline{CEAB}$  LOW, a LOW signal makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the  $\overline{LEAB}$  signal puts the A latches in the storage mode and their outputs no longer change the A inputs. With  $\overline{CEAB}$  and  $\overline{OEAB}$  both LOW, the three-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{OEBA}$  inputs. Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

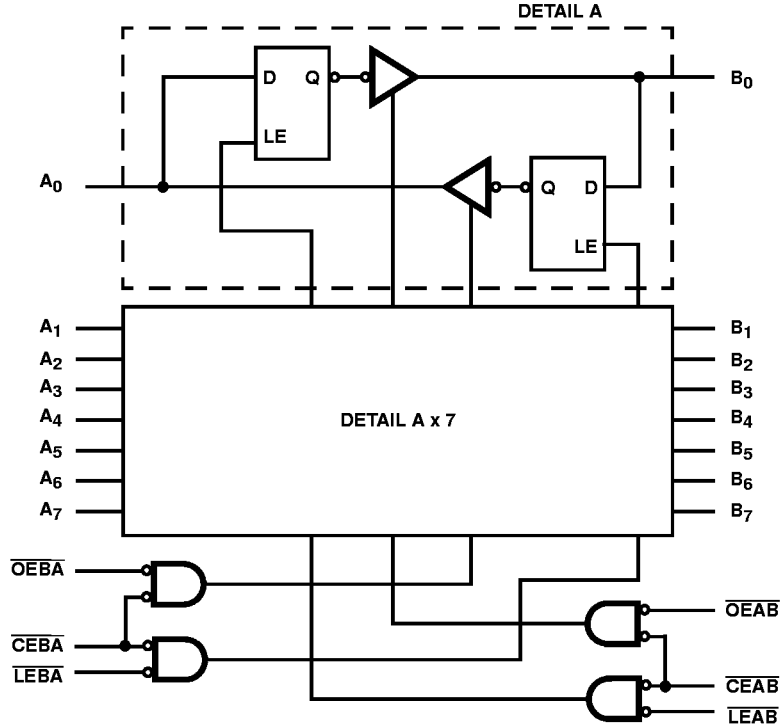
The CD74LPT543 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

### Pinout



# CD74LPT543

## Functional Block Diagram



TRUTH TABLE (NOTES 1, 3)

| INPUTS            |                   |                   | LATCH STATUS | OUTPUT BUFFERS             |
|-------------------|-------------------|-------------------|--------------|----------------------------|
| $\overline{CEAB}$ | $\overline{LEAB}$ | $\overline{OEAB}$ | A-TO-B       | $B_0 - B_7$                |
| H                 | X                 | X                 | Storing      | High Z                     |
| X                 | H                 | X                 | Storing      | X                          |
| X                 | X                 | H                 | X            | High Z                     |
| L                 | L                 | L                 | Transparent  | Current A Inputs           |
| L                 | H                 | L                 | Storing      | Previous A Inputs (Note 2) |

NOTES:

1. A-to-B data flow is shown. B-to-A flow control is the same except using  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{OEBA}$ .
2. Before  $\overline{LEAB}$  LOW-to-HIGH Transition
3. H = High Voltage Level  
L = Low Voltage Level  
X = Don't Care or Irrelevant  
Z = High Impedance

## Pin Descriptions

| PIN NAME          | DESCRIPTION                                      |
|-------------------|--|
| $\overline{OEAB}$ | A-to-B Output Enable Input (Active LOW)          |
| $\overline{OEBA}$ | B-to-A Output Enable Input (Active LOW)          |
| $\overline{CEAB}$ | A-to-B Enable Input (Active LOW)                 |
| $\overline{CEBA}$ | B-to-A Enable Input (Active LOW)                 |
| $\overline{LEAB}$ | A-to-B Latch Enable Input (Active LOW)           |
| $\overline{LEBA}$ | B-to-A Latch Enable Input (Active LOW)           |
| $A_0 - A_7$       | A-to-B Data Inputs or B-to-A Three-State Outputs |
| $B_0 - B_7$       | B-to-A Data Inputs or B-to-A Three-State Outputs |
| GND               | Ground   |
| $V_{CC}$          | Power  |



## CD74LPT543

### Electrical Specifications (Continued)

| PARAMETER  | SYMBOL          | (NOTE 5)<br>TEST CONDITIONS   | MIN   | (NOTE 6)<br>TYP | MAX       | UNITS            |                    |
|--|-----------------|---|---|-----------------|-----------|------------------|--------------------|
| Short Circuit Current (Note 8)                         | $I_{OS}$        | $V_{CC} = \text{Max (Note 7)}, V_{OUT} = \text{GND}$  | -60   | -85             | -240      | mA               |                    |
| Power Down Disable                                     | $I_{OFF}$       | $V_{CC} = 0V, V_{IN} \text{ or } V_{OUT} \leq 4.5V$   | -   | -               | $\pm 100$ | $\mu A$          |                    |
| Input Hysteresis                                       | $V_H$           |   | -   | 150             | -         | mV               |                    |
| <b>CAPACITANCE</b> $T_A = 25^\circ C, f = 1\text{MHz}$ |                 |   |   |                 |           |                  |                    |
| Input Capacitance (Note 10)                            | $C_{IN}$        | $V_{IN} = 0V$   | -   | 4.5             | 6         | pF               |                    |
| Output Capacitance (Note 10)                           | $C_{OUT}$       | $V_{OUT} = 0V$  | -   | 5.5             | 8         | pF               |                    |
| <b>POWER SUPPLY SPECIFICATIONS</b>                     |                 |   |   |                 |           |                  |                    |
| Quiescent Power Supply Current                         | $I_{CC}$        | $V_{CC} = \text{Max}$   | $V_{IN} = \text{GND}$<br>or $V_{CC}$              | -               | 0.1       | 10               | $\mu A$            |
| Quiescent Power Supply Current TTL Inputs HIGH         | $\Delta I_{CC}$ | $V_{CC} = \text{Max}$   | $V_{IN} = V_{CC} - 0.6V$<br>(Note 11)             | -               | 2.0       | 30               | $\mu A$            |
| Dynamic Power Supply (Note 12)                         | $I_{CCD}$       | $V_{CC} = \text{Max}, \text{Outputs Open}$<br>$\overline{CEAB}$ and $\overline{OEAB} = \text{GND}$<br>$\overline{CEBA} = V_{CC}$<br>One Bit Toggling<br>50% Duty Cycle                                | $V_{IN} = V_{CC}$<br>$V_{IN} = \text{GND}$        | -               | 50        | 75               | $\mu A/\text{MHz}$ |
| Total Power Supply Current (Note 14)                   | $I_C$           | $V_{CC} = \text{Max}, \text{Outputs Open}$<br>$f_l = 10\text{MHz}, 50\% \text{ Duty Cycle}$<br>$\overline{CEAB}$ and $\overline{OEAB} = \text{GND}$<br>$\overline{CEBA} = V_{CC}$<br>One Bit Toggling | $V_{IN} = V_{CC} - 0.6V$<br>$V_{IN} = \text{GND}$ | -               | 0.6       | 2.3              | mA                 |
|  |                 | $V_{CC} = \text{Max}, \text{Outputs Open}$<br>$f_l = 2.5\text{MHz}, 50\% \text{ Duty Cycle}$<br>$\overline{CEAB}$ and $\overline{OEAB} = \text{GND}$<br>$\overline{CEBA} = V_{CC}$<br>8 Bits Toggling | $V_{IN} = V_{CC} - 0.6V$<br>$V_{IN} = \text{GND}$ | -               | 2.1       | 4.7<br>(Note 13) | mA                 |

## CD74LPT543

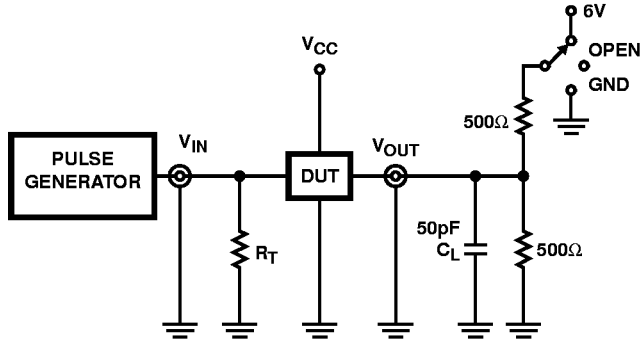
### Switching Specifications Over Operating Range (NOTE 15)

| PARAMETER   | SYMBOL                                 | (NOTE 16)<br>TEST<br>CONDITIONS                | CD74LPT543       |      | CD74LPT543A      |     | CD74LPT543C      |     | UNITS |
|---|--|--|------------------|------|------------------|-----|------------------|-----|-------|
|   |  |  | (NOTE 17)<br>MIN | MAX  | (NOTE 17)<br>MIN | MAX | (NOTE 17)<br>MIN | MAX |       |
| Propagation Delay<br>Transparent Mode<br>A <sub>N</sub> to B <sub>N</sub> or B <sub>N</sub> to A <sub>N</sub>               | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF<br>R <sub>L</sub> = 500Ω | 2.5              | 8.5  | 2.5              | 6.5 | 2.5              | 5.3 | ns    |
| Propagation Delay<br>LEBA to A <sub>N</sub><br>LEAB to B <sub>N</sub>   | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> |  | 2.5              | 12.5 | 2.5              | 8.0 | 2.5              | 7.0 | ns    |
| Output Enable Time<br>OEBA or OEAB to A <sub>N</sub> or B <sub>N</sub><br>CEBA or CEAB to A <sub>N</sub> or B <sub>N</sub>  | t <sub>PZH</sub> ,<br>t <sub>PZL</sub> |  | 2.0              | 12.0 | 2.0              | 9.0 | 2.0              | 8.0 | ns    |
| Output Disable Time<br>OEBA or OEAB to A <sub>N</sub> or B <sub>N</sub><br>CEBA or CEAB to A <sub>N</sub> or B <sub>N</sub> | t <sub>PHZ</sub> ,<br>t <sub>PLZ</sub> |  | 2.0              | 9.0  | 2.0              | 7.5 | 2.0              | 6.5 | ns    |
| Setup Time HIGH or LOW,<br>A <sub>N</sub> or B <sub>N</sub> to LEAB or LEBA   | t <sub>SU</sub>                        |  | 3.0              | -    | 2.0              | -   | 2.0              | -   | ns    |
| Hold Time HIGH or LOW,<br>A <sub>N</sub> or B <sub>N</sub> to LEAB or LEBA  | t <sub>H</sub>                         |  | 2.0              | -    | 2.0              | -   | 2.0              | -   | ns    |
| LEAB or LEBA Pulse Width<br>LOW   | t <sub>W</sub>                         |  | 5.0              | -    | 5.0              | -   | 5.0              | -   | ns    |

**NOTES:**

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V<sub>CC</sub> = 3.3V, 25°C ambient and maximum loading.
7. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
8. This parameter is guaranteed but not tested.
9. V<sub>OH</sub> = V<sub>CC</sub> - 0.6V at rated current.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input; all other inputs at V<sub>CC</sub> or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
14. I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$   
 I<sub>CC</sub> = Quiescent Current  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 f<sub>I</sub> = Input Frequency  
 N<sub>I</sub> = Number of Inputs at f<sub>I</sub>  
 All currents are in milliamps and all frequencies are in megahertz.
15. Propagation Delays and Enable/Disable times are with V<sub>CC</sub> = 3.3V 0.3V, normal range. For V<sub>CC</sub> = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
16. See test circuit and wave forms.
17. Minimum limits are guaranteed but not tested on Propagation Delays.

Test Circuits and Waveforms



NOTE:

18. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $Z_{OUT} \leq 50\Omega$ ;  $t_f, t_r \leq 2.5\text{ns}$ .

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

| TEST                                  | SWITCH |
|---------------------------------------|--------|
| $t_{PLZ}, t_{PZL}, \text{Open Drain}$ | 6V     |
| $t_{PHZ}, t_{PZH}$                    | GND    |
| $t_{PLH}, t_{PHL}$                    | Open   |

DEFINITIONS:

$C_L$  = Load capacitance, includes jig and probe capacitance.  
 $R_T$  = Termination resistance, should be equal to  $Z_{OUT}$  of the Pulse Generator.

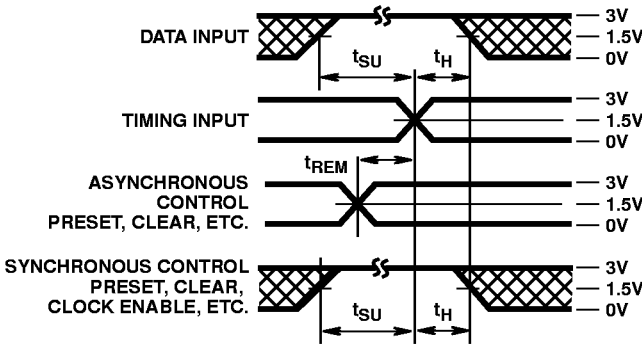


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

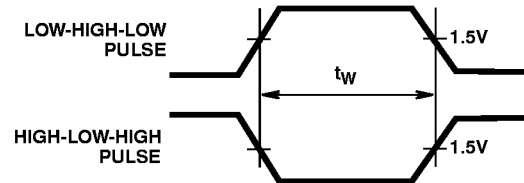


FIGURE 3. PULSE WIDTH

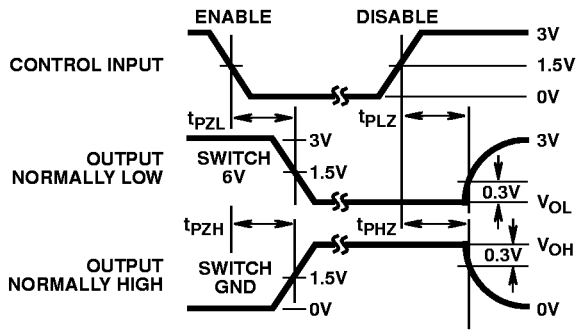


FIGURE 4. ENABLE AND DISABLE TIMING

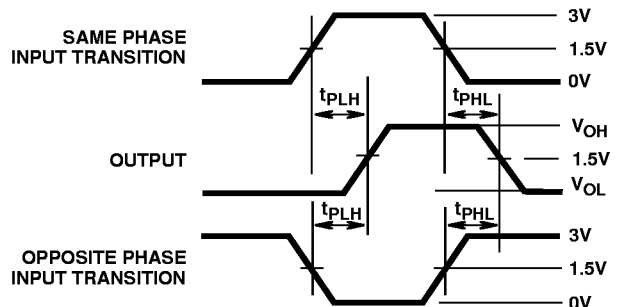


FIGURE 5. PROPAGATION DELAY