Data Sheet
March 1997

microelectronics group

Lucent Technologies
Bell Labs Innovations

T7115A Synchronous Protocol Data Formatter

Features

Serial Port Interface

- 32-channel (full-duplex), multiplexed, serial input/output HDLC processing
- Support for T1/DS1 24-channel and CEPT/E1 32-channel modes
- Automatic flag transmission and detection
- Flag stuffing up to 2,047 flags
- Flag adjustment for synchronous rate adaption
- Full, partial, or no CRC generation and checking
- Zero-bit insertion and deletion
- Abort/idle detection and transmission
- Long-frame detection
- 2 Mbits/s continuous serial data rate
- Transparent mode (no protocol) supports ECMA 102 and ITU-T I.463 RA2 rate adaption standards
- Dynamic channel allocation (or channel concatenation) supports DS0, H0, H11, and H12 channels and other channel rates
- Bit-rate control on each channel
- Channel inversion
- Loopback mode
- DMA CRC for relay mode

Microprocessor Interface

- Compatibility with 16-bit or 32-bit microprocessor systems
- On-chip, 64-channel, DMA memory address generator and buffer manager
- Interrupt queue (up to 4,096 interrupts)
- Nonmultiplexed 16-bit data and 24-bit address (8 Mwords) buses
- Transmit and receive buffers accessible through memory-mapped look-up tables

Description

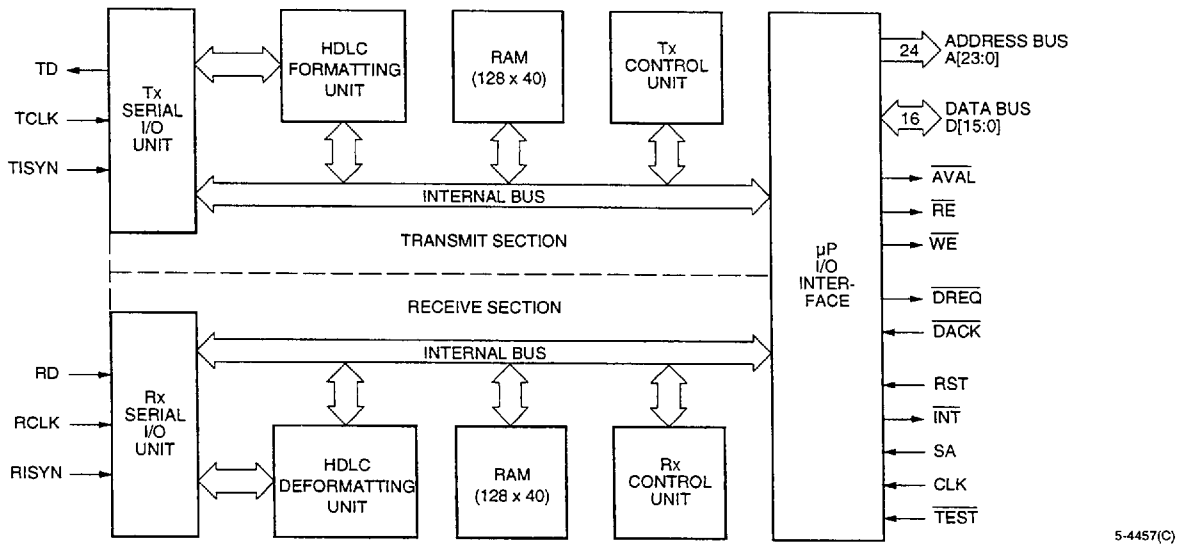


Figure 1. Simplified Block Diagram

Table of Contents

Contents

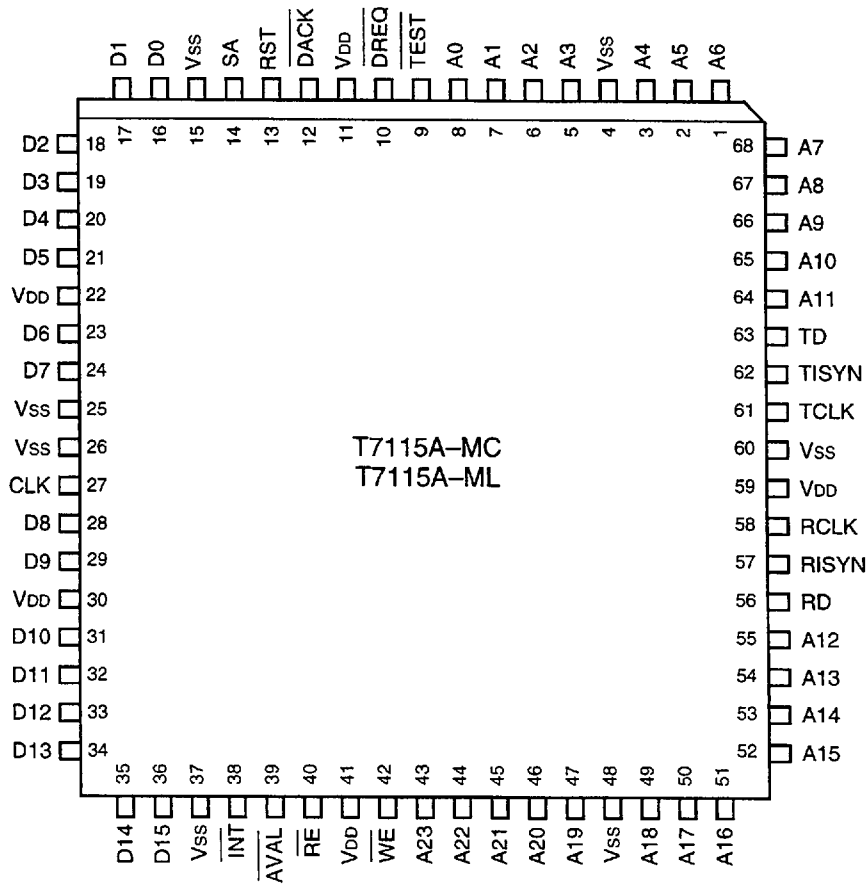
Page

Description (continued)

The Lucent Technologies Microelectronics Group T7115A Synchronous Protocol Data Formatter (SPYDER-T) integrated circuit is an extremely flexible 32-channel HDLC/DMA controller. The device can be used in a variety of data and signaling applications to provide cost-effective DS1/E1 line termination or multiple D-channel termination. All inputs and outputs of the T7115A SPYDER-T are TTL compatible. The device is fabricated by using CMOS technology, requires a single 5 V supply, and is available in a 68-pin, plastic leaded chip carrier.

Pin Information

This section gives the pin numbering information for both a nonindustry-standard (Figure 2A) and an industry-standard pin convention (Figure 2B). The actual physical location of each pin function is the same for both numbering schemes.



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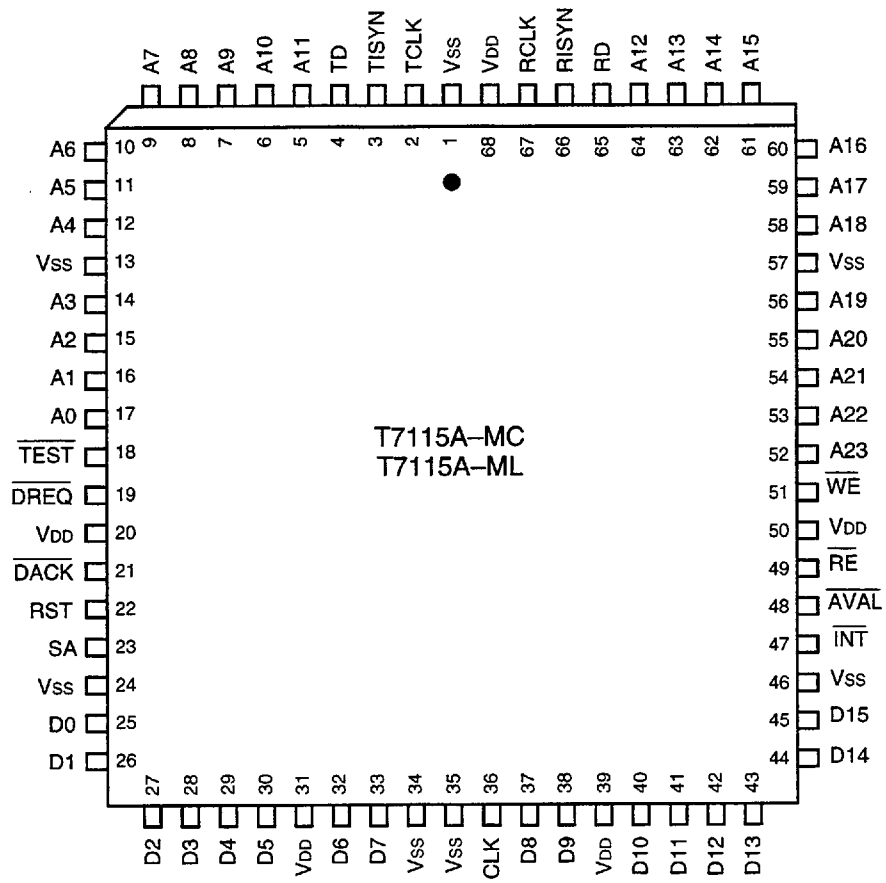
A. Nonindustry-Standard Numbering Convention

Figure 2. Pin Function Diagrams

Pin Information (continued)



B. Industry-Standard Numbering Convention

Figure 2. Pin Function Diagrams (continued)

Pin Information (continued)

Table 1. Pins Grouped by Function (Nonindustry Standard)

Symbol	Pin	Symbol	Pin
A23—A0	43—47, 49—55, 64—68, 1—3, 5—8	RISYN	57
$\overline{\text{AVAL}}$	39	RST	13
CLK	27	SA	14
D15—D0	36—31, 24, 23, 21—16	TCLK	61
$\overline{\text{DACK}}$	12	TD	63
$\overline{\text{DREQ}}$	10	$\overline{\text{TEST}}$	9
$\overline{\text{INT}}$	38	TISYN	62
RCLK	58	$\overline{\text{WE}}$	42
RD	56	V_{DD}	11, 22, 30, 59
$\overline{\text{RE}}$	40	V_{SS}	4, 15, 25, 26, 37, 48, 60

Table 2. Pins Grouped by Function (Industry Standard)

Symbol	Pin	Symbol	Pin
A23—A0	52—56, 58—64, 5—12, 14—17	RISYN	66
$\overline{\text{AVAL}}$	48	RST	22
CLK	36	SA	23
D15—D0	45—40, 33, 32, 30—25	TCLK	2
$\overline{\text{DACK}}$	21	TD	4
$\overline{\text{DREQ}}$	19	$\overline{\text{TEST}}$	18
$\overline{\text{INT}}$	47	TISYN	3
RCLK	67	$\overline{\text{WE}}$	51
RD	65	V_{DD}	20, 31, 39, 68
$\overline{\text{RE}}$	49	V_{SS}	1, 13, 24, 34, 35, 46, 57

Pin Information (continued)

Table 3. Pin Descriptions

Pins		Symbol	Type	Name/Function
Industry Standard	Nonindustry Standard			
10	1	A6	O	**Address Bus Bit 6.**
11	2	A5	O	**Address Bus Bit 5.**
12	3	A4	O	**Address Bus Bit 4.**
13	4	VSS	—	**Ground.**
14	5	A3	O	**Address Bus Bit 3.**
15	6	A2	O	**Address Bus Bit 2.**
16	7	A1	O	**Address Bus Bit 1.**
17	8	A0	O	**Address Bus Bit 0.**
18	9	$\overline{\text{TEST}}$	I	**Test Input (Active-Low).** All pins become 3-stated when this pin is driven low. The SPYDER-T should always be reset immediately after $\overline{\text{TEST}}$ is driven high.
19	10	$\overline{\text{DREQ}}$	O	**DMA Request (Active-Low).** This pin indicates that the SPYDER-T requires the system bus for a data transfer.
20	11	VDD	—	**5 V Supply.**
21	12	$\overline{\text{DACK}}$	I	**DMA Acknowledge (Active-Low).** This pin indicates that the SPYDER-T has been granted the system bus.
22	13	RST	I	**Reset Input.** A minimum input of 2xTCLK (or RCLK) is required. TCLK, RCLK, and CLK must all be active.
23	14	SA	I	**SPYDER Attention Input.** This pin must be pulsed high for a minimum of one clock (CLK) cycle.
24	15	VSS	—	**Ground.**
25	16	D0	I/O	**Data Bus Bit 0.** This is a 3-state, bidirectional I/O pin.
26	17	D1	I/O	**Data Bus Bit 1.** This is a 3-state, bidirectional I/O pin.
27	18	D2	I/O	**Data Bus Bit 2.** This is a 3-state, bidirectional I/O pin.
28	19	D3	I/O	**Data Bus Bit 3.** This is a 3-state, bidirectional I/O pin.
29	20	D4	I/O	**Data Bus Bit 4.** This is a 3-state, bidirectional I/O pin.
30	21	D5	I/O	**Data Bus Bit 5.** This is a 3-state, bidirectional I/O pin.
31	22	VDD	—	**5 V Supply.**
32	23	D6	I/O	**Data Bus Bit 6.** This is a 3-state, bidirectional I/O pin.
33	24	D7	I/O	**Data Bus Bit 7.** This is a 3-state, bidirectional I/O pin.
34	25	VSS	—	**Ground.**
35	26	VSS	—	**Ground.**
36	27	CLK	I	**Clock Input.** This pin requires a minimum input of 12.352 MHz for T1/DS1 mode and a minimum input of 16.384 MHz for CEPT/E1 mode.
37	28	D8	I/O	**Data Bus Bit 8.** This is a 3-state, bidirectional I/O pin.

Pin Information (continued)

Table 3. Pin Descriptions (continued)

Pins		Symbol	Type	Name/Function
Industry Standard	Nonindustry Standard			
38	29	D9	I/O	**Data Bus Bit 9.** This is a 3-state, bidirectional I/O pin.
39	30	V_{DD}	—	**5 V Supply.**
40	31	D10	I/O	**Data Bus Bit 10.** This is a 3-state, bidirectional I/O pin.
41	32	D11	I/O	**Data Bus Bit 11.** This is a 3-state, bidirectional I/O pin.
42	33	D12	I/O	**Data Bus Bit 12.** This is a 3-state, bidirectional I/O pin.
43	34	D13	I/O	**Data Bus Bit 13.** This is a 3-state, bidirectional I/O pin.
44	35	D14	I/O	**Data Bus Bit 14.** This is a 3-state, bidirectional I/O pin.
45	36	D15	I/O	**Data Bus Bit 15.** This is a 3-state, bidirectional I/O pin.
46	37	V_{SS}	—	**Ground.**
47	38	$\overline{INT}$	O	**Interrupt Request Output (Active-Low).**
48	39	$\overline{AVAL}$	O	**Address Valid (Active-Low).** This pin indicates that the address bus (A23—A0) is now valid.
49	40	$\overline{RE}$	O	**Read Enable (Active-Low).** This pin indicates that a read operation is to occur.
50	41	V_{DD}	—	**5 V Supply.**
51	42	$\overline{WE}$	O	**Write Enable (Active-Low).** This pin indicates that a write operation is to occur.
52	43	A23	O	**Address Bus Bit 23.**
53	44	A22	O	**Address Bus Bit 22.**
54	45	A21	O	**Address Bus Bit 21.**
55	46	A20	O	**Address Bus Bit 20.**
56	47	A19	O	**Address Bus Bit 19.**
57	48	V_{SS}	—	**Ground.**
58	49	A18	O	**Address Bus Bit 18.**
59	50	A17	O	**Address Bus Bit 17.**
60	51	A16	O	**Address Bus Bit 16.**
61	52	A15	O	**Address Bus Bit 15.**
62	53	A14	O	**Address Bus Bit 14.**
63	54	A13	O	**Address Bus Bit 13.**
64	55	A12	O	**Address Bus Bit 12.**
65	56	RD	I	**Receive Data Input.**
66	57	RISYN	I	**Receive Interdevice Synchronization.** This pin is sampled on the rising edge of RCLK and identifies the current bit on the serial line (RD) as the first bit of an E1 frame (or framing bit of a T1/DS1 frame).

Pin Information (continued)

Table 3. Pin Descriptions (continued)

Pins		Symbol	Type	Name/Function
Industry Standard	Nonindustry Standard			
67	58	RCLK	I	**Receive Clock.** This pin must be pulsed eight times per time slot for synchronization and external timing regardless of the bit rate.
68	59	V_{DD}	—	**5 V Supply.**
1	60	V_{SS}	—	**Ground.**
2	61	TCLK	I	**Transmit Clock.** This pin must be pulsed eight times per time slot for synchronization and external timing regardless of the bit rate.
3	62	TISYN	I	**Transmit Interdevice Synchronization.** This pin establishes frame alignment and is sampled on the rising edge of TCLK. It identifies the current bit on the serial line (TD) as the last bit of a E1 or T1/DS1 frame.
4	63	TD	O	**Transmit Data Output.**
5	64	A11	O	**Address Bus Bit 11.**
6	65	A10	O	**Address Bus Bit 10.**
7	66	A9	O	**Address Bus Bit 9.**
8	67	A8	O	**Address Bus Bit 8.**
9	68	A7	O	**Address Bus Bit 7.**

Functional Overview

The SPYDER-T device reads data from shared memory, performs low-level formatting functions, and supports up to 32 channels by transmitting the data to a serial concentration highway in a time-division multiplexed manner. Similarly, the SPYDER-T receives serial data from the concentration highway, performs deformatting functions, and, on a channel-by-channel basis, stores the raw data in the shared memory.

The device transmits and receives serial data at the primary rate of 2.048 Mbits/s for the CEPT/E1 32-channel European mode and 1.544 Mbits/s for the T1/DS1 24-channel North American mode. Two or more time slots can be concatenated to create a superchannel. These time slots do not have to be adjacent (see Figures 3 and 4).

The SPYDER-T also provides nonprotocol and transparent DMA functions on all or selected channels. The on-chip DMA controller allows the direct transfer of packet data (up to 8,191 bytes) between the shared memory and the SPYDER-T for up to 32 full-duplex channels without host-processor intervention. The SPYDER-T and the host processor exchange all commands and messages through the shared memory.

Functional Overview (continued)

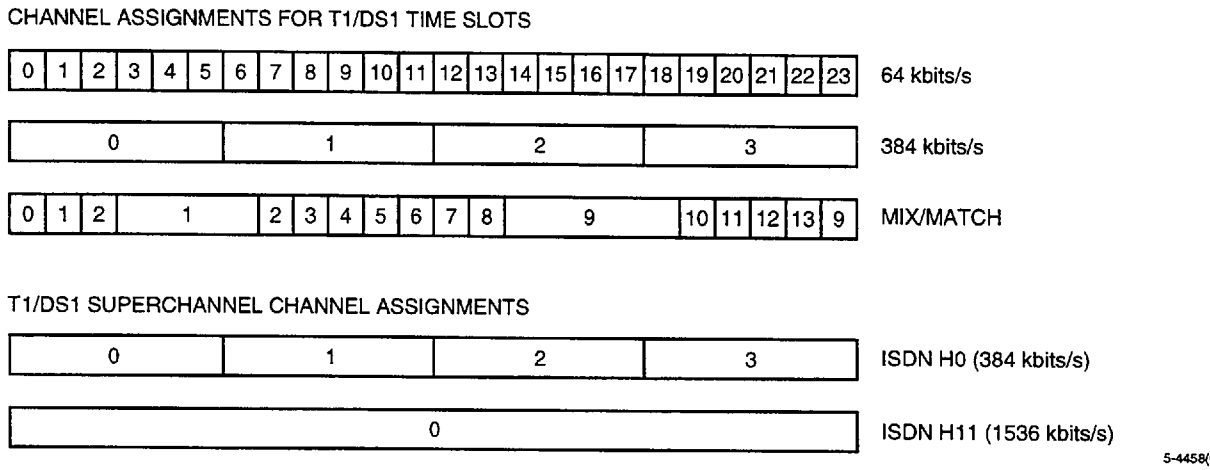


Figure 3. Dynamic Channel Allocation for T1 Time Slots

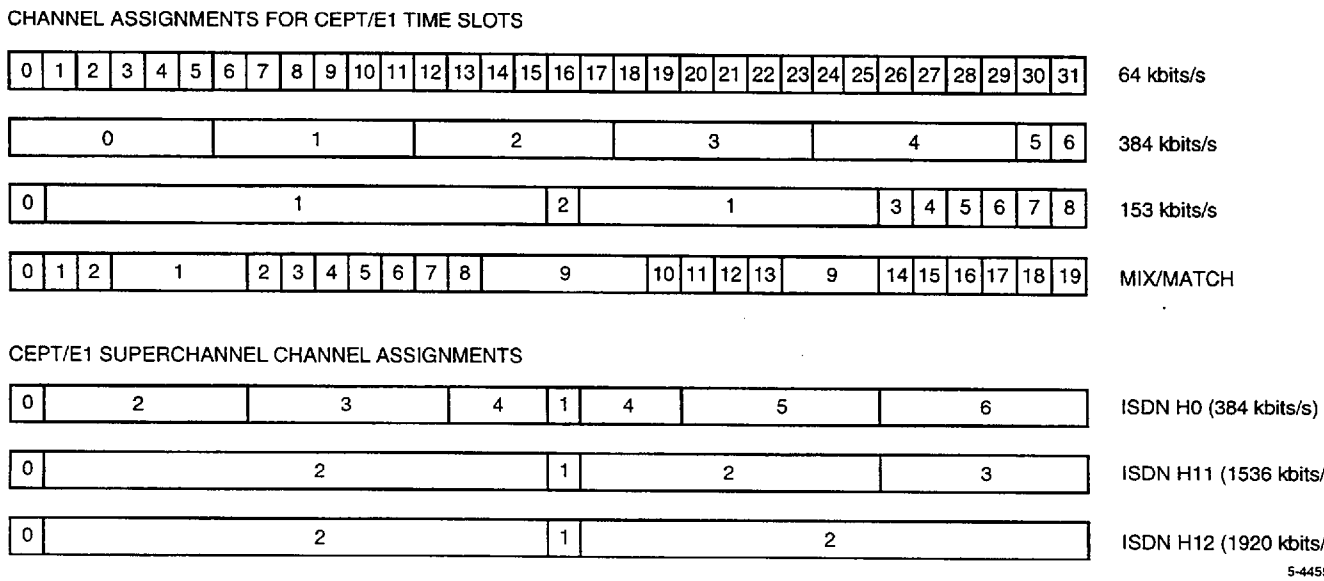


Figure 4. Dynamic Channel Allocation for E1 Time Slots

The HDLC Mode

The SPYDER-T uses the following HDLC format:

Opening Flag	Header Bytes	Information Field	CRC	Closing Flag
01111110	Up to 7 bytes	≥0 bytes*	2 bytes	01111110

* The length of the transmit buffer must be at least 2 bytes in any transmit descriptor. The T7115A discards any receive data with less than 2 bytes in any receive descriptor with no status reported.

The transmitter transmits a flag (opening flag) before the header bytes and transmits another flag (closing flag) after the CRC bytes. The transmitted data (header, information, and CRC bytes) delimited by these two flags is referred to as a frame. The CRC bytes (16 bits) are generated by the SPYDER-T, while the header bytes and information data are fetched from the shared memory. For transparency, zero-bit stuffing is performed on the data between the last bit of the opening flag and the first bit of the closing flag. The CRC received by the SPYDER-T is stored in the receive buffer, with the first bit received in the least significant bit (LSB) position.

The receiver recognizes a frame after receiving one flag byte followed by a nonflag byte. After performing zero-bit unstuffing on the received data, the receiver performs a CRC on both the header bytes and information field (if required). The receiver accumulates 2 bytes of data in on-chip memory and writes them to shared memory. This procedure is repeated until a closing flag is received.

Zero-Bit Insertion and Deletion (Bit Stuffing and Unstuffing)

The SPYDER-T performs zero-bit stuffing and unstuffing on the header bytes, information field, and CRC to maintain transparency. In the transmit unit, if five consecutive 1s appear in the serial data stream being transmitted, a zero bit is automatically inserted (bit stuffing) after the fifth 1. In the receive unit, if five consecutive 1s followed by a 0 are received, the 0 is assumed to have been inserted and is automatically deleted (bit unstuffing).

Flag

The flag character, 01111110 (0x7E), is used for frame synchronization. Flags are also used as time-fill characters between frames. If the receive unit receives only one flag between two frames, the SPYDER-T recognizes it as the closing flag of one frame and also the opening flag of the next frame. The transmit unit can also transmit one flag between frames.

The receive unit also recognizes two or more consecutive flags that share a common zero bit (011111101111110).

The SPYDER-T inserts an opening flag before transmitting the first bit of the header and appends the closing flag after the last bit of CRC. A number of flags (not including the opening and closing flag) equal to the value of the flag count (FCNT) in the transmit descriptor are then transmitted.

Abort

Upon receiving a command from the host, the transmit unit sends an abort character, 01111111 (0x7F), immediately after sending the current byte of data. The CRC bytes are not sent when an abort occurs. The receive unit interrupts the host when an abort is received.

Idle

The idle character, 11111111 (0xFF), can be transmitted between frames as an alternative to the flag character. The number of idle characters transmitted is specified in the FCNT field of the transmit descriptor. However, the opening flag and closing flag are still sent to delimit the frame. When data is being received, an idle condition is detected after 15 consecutive 1s are received.

The Transparent (Non-HDLC) Modes

There are two transparent (non-HDLC) modes available on the SPYDER-T. Transparent mode 0 is totally transparent, while transparent mode 1 performs the second-stage rate adaption, RA2, defined in the ECMA 102 and ITU-T I.463 standards. The transparent modes are selected by the two control bits (HDLC and TMODE) in the channel-control register.

Transparent Mode 0

The SPYDER-T transmits data in a completely transparent manner without performing any bit manipulation or flag insertion (no flags if FCNT = 0).

For the receive channels, the SPYDER-T continuously writes received data into shared memory as specified in the receive descriptor. Since no boundaries exist (no flags or idles) in this mode, the receive unit continuously fills buffers in shared memory without creating frame boundaries. With the RTA bit cleared and the FR bit set in the channel-control register, the receive unit removes the flags defined in the control mask from the data (flags are not written to shared memory). In this mode, the RTA and FR bits cannot be set at the same time; both enable options use the same 8-bit code in the control mask. This code can be used for either bit rate control (RTA set) or flag filtering (FR set), but not for both.

The following is an example of how data is received and stored in transparent mode 0 with RTA set, FR cleared, and 0x0F in the control mask (32 kbits/s).

Note: A pull-down resistor is required at the serial output to ensure that 3-stated conditions are transmitted as 0.

The following is an example of a data stream received at the serial port:

0000zzzz, 0000zzzz, 0010zzzz, 1011zzzz, 0011zzzz, 1111zzzz,

0010zzzz, 1100zzzz, 1110zzzz, 1100zzzz, 0011zzzz, 1111zzzz,

0011zzzz, 0000zzzz, 1111zzzz, 1011zzzz, 1110zzzz, 0000zzzz,

1111zzzz, 1111zzzz, → more serial data

The processed data is stored in shared memory as follows:

D7—D0	D7—D0
RD #1	**RD #2**
00000000	00001100
00000000	00001111
00000100	00001100
00001101	00000000
00001100	00001111
00001111	00001101
00000100	00000111
00000011	00000000
00000111	00001111
00000011	00001111
CNT = 10	CNT = 10

The Transparent (Non-HDLC) Modes

(continued)

Transparent Mode 1

HDLC formatting is not performed in transparent mode 1. The SPYDER-T reads raw data from the transmit buffers and transmits it over the serial port (the concentration highway) without formatting. The SPYDER-T performs the same sequence of buffer management functions that is performed in HDLC mode. The SPYDER-T sends the number of bytes specified in the CNT field of the transmit descriptor and sends the number of fill characters specified in the FCNT field. No flags are transmitted if FCNT is cleared. In this mode, the 8-bit code in the control mask defines the intermediate data rate (8, 16, or 32 kbits/s) and the bit positions in each data byte. Transparent mode 0 should be used for rate adaptation in a range of 48 kbits/s to 56 kbits/s.

In the receive unit, the SPYDER-T performs frame and byte alignment by detecting at least eight consecutive 0s followed by a 1, accumulating 16 bits of data (excluding leading 0s but including the first 1) and storing the 16 bits as a word in the shared memory. An example of transparent mode 1 with RTA set and 0x0F in the control mask (32 kbits/s) is shown below.

The following is an example of a data stream received at the serial port:

0000zzzz, 0000zzzz, 0010zzzz, 1011zzzz, 0011zzzz, 1111zzzz,

0010zzzz, 1100zzzz, 1110zzzz, 1100zzzz, 0011zzzz, 1111zzzz,

0011zzzz, 0000zzzz, 1111zzzz, 1011zzzz, 1110zzzz, 0000zzzz,

1111zzzz, 1111zzzz, 1000zzzz, 0000zzzz, 0011zzzz, 1111zzzz,

1110zzzz, 0000zzzz, 0010zzzz, → more serial data

The processed data is stored in shared memory as follows:

D7—D0 RD #1	D7—D0 RD #2
00110101	11111111
00111111	00000001
11001101	01
00001101	
00111111	
11000011	more
11110111	data
11000001	
01111111	

Memory Interface

The SPYDER-T and the host communicate with one another via a shared memory. All pointers within this shared memory must point to a word boundary (A0 = 0). The components of this memory interface are described in the following sections (see Figures 5 and 6).

SPYDER-T Configuration Pointer

The SPYDER-T configuration pointer (SCP) resides at address 0xFFFFFC and points to the SPYDER-T control block, which provides initialization information for the entire SPYDER-T system. Table 4 shows the bit assignment for the SCP.

Table 4. SPYDER-T Configuration Pointer (SCP)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used								Control Block Address (high 8 bits)							
	Control Block Address (low 16 bits)														

Control Block

The control block (CB) consists of the SPYDER-T attention register, interrupt queue pointer, channel-configuration register, and 32 channel-control blocks. The CB requires a total of 588 bytes of memory. All pointers and registers must reside on word boundaries. The last eight channel-control blocks (64 words) are not used for the T1/DS1 mode.

Memory Interface (continued)

Control Block (continued)

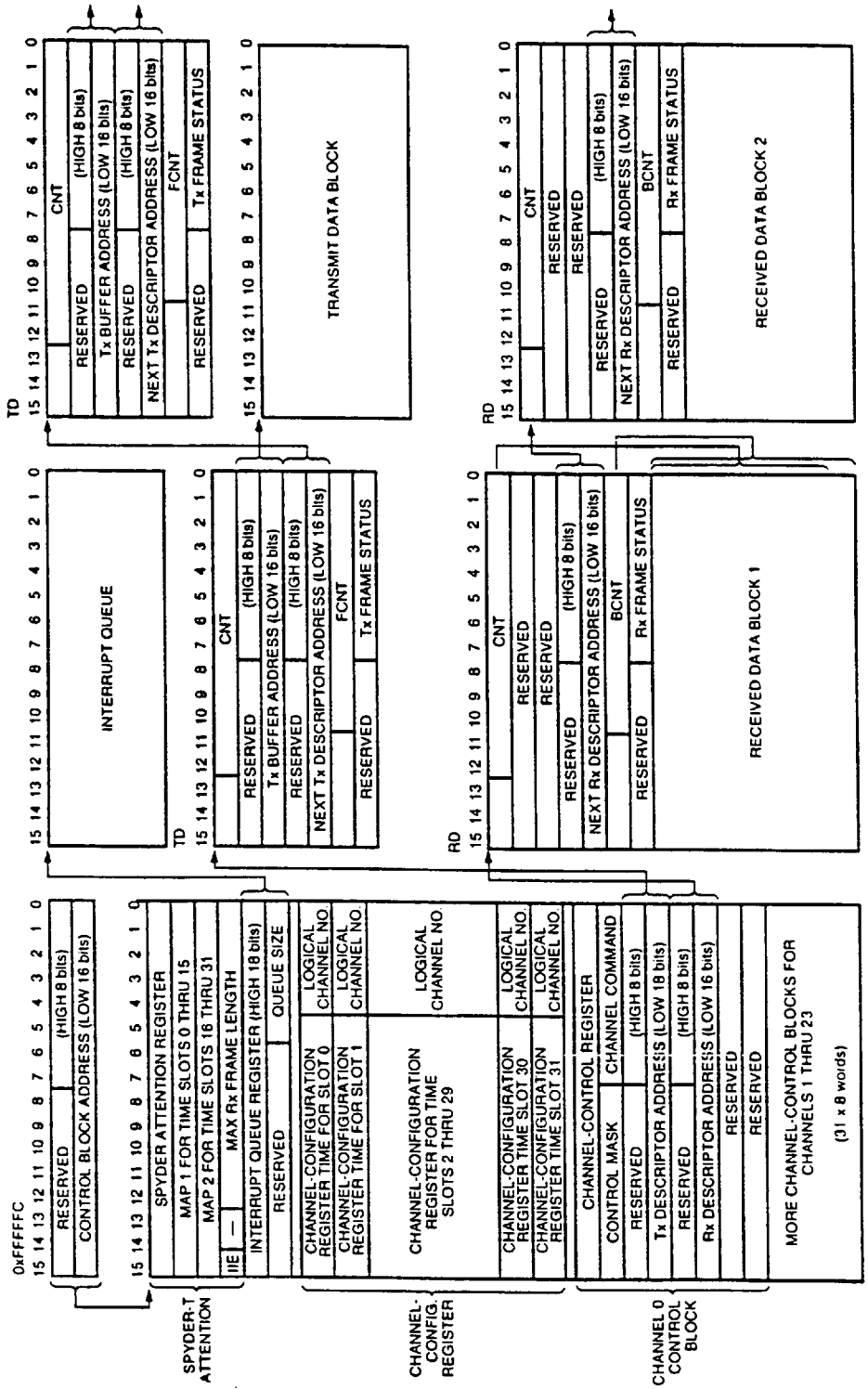


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Figure 5. Memory Maps for the CEPT/E1 32-Channel International Mode

Memory Interface (continued)

Control Block (continued)

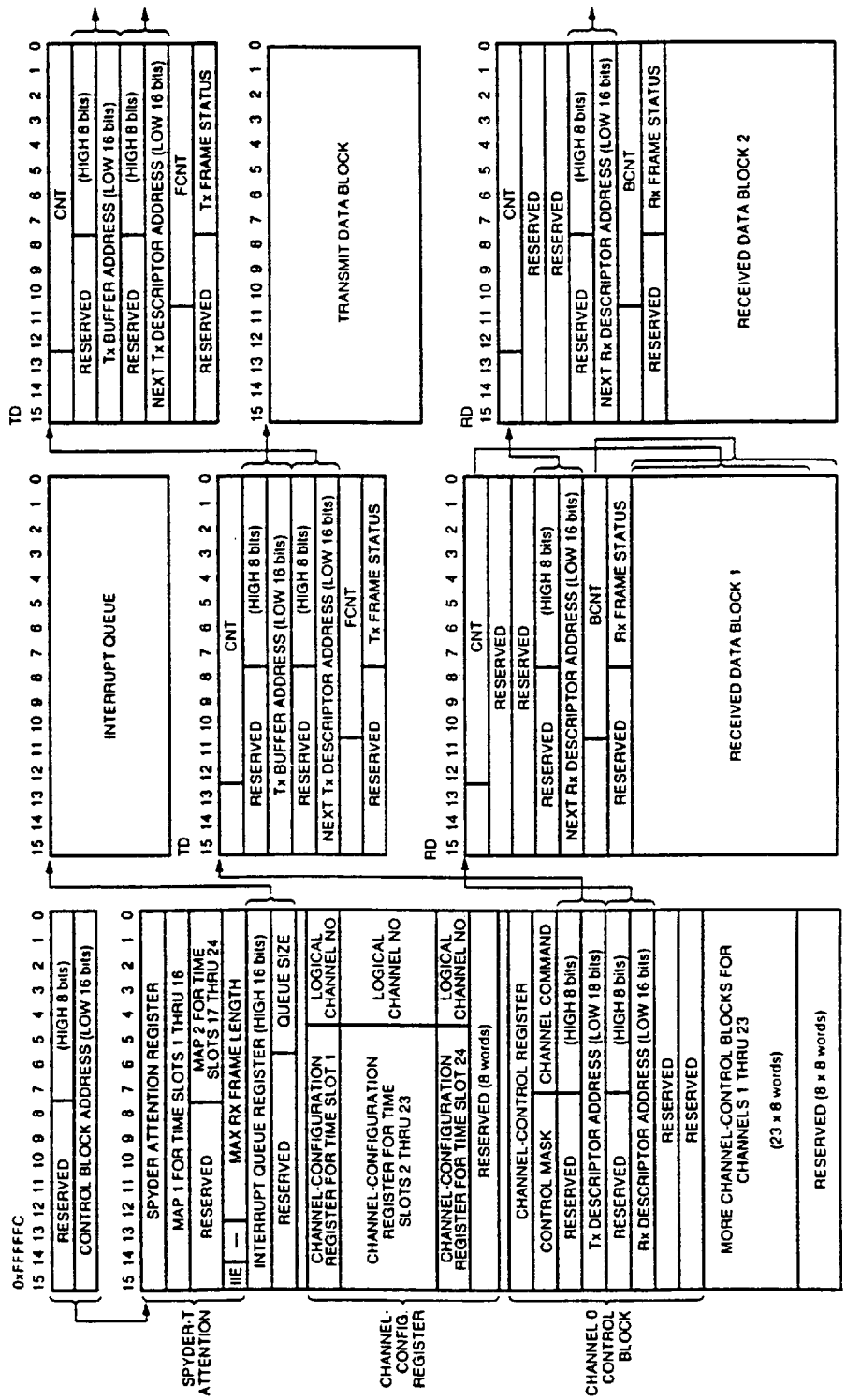


Figure 6. Memory Maps for the T1/DS1 24-Channel North American Mode

Memory Interface (continued)

Control Block (continued)

Table 5. Control Block Memory Structure

Control Block	No. of Bytes
SPYDER-T Attention Register	8
Interrupt Queue Pointer	4
Channel-configuration Register	64
Channel-control Blocks	512

SPYDER-T Attention Register

The first word of the SPYDER-T attention (SA) register must reside at the address specified in the SCP. This 8-byte register is the first in the CB and is read by the SPYDER-T immediately after the host issues an SA request. After servicing the SA request, the SPYDER-T writes the SA register to the host and clears the BOOT, NIQ, and CA bits. The host must not issue a second SA request until these bits are cleared.

Table 6. SPYDER-T Attention Register for CEPT/E1 32-Channel International Mode (MOD = 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOT	NIQ	LOOP	SWB	—			MOD	—		CA	Channel Number				
Map 1 for Time Slots 15—0															
Map 2 for Time Slots 31—16															
IIE	—			Maximum Receive Frame Length											

Table 7. SPYDER-T Attention Register for T1/DS1 24-Channel North American Mode (MOD = 0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BOOT	NIQ	LOOP	SWB	—			MOD	—		CA	Channel Number				
Map 1 for Time Slots 16—0															
Not Used								Map 2 for Time Slots 24—17							
IIE	—			Maximum Receive Frame Length											

Table 8. SPYDER-T Attention Register Bit Descriptions

Symbol	Name/Description
BOOT	**Boot.** If the host sets this bit before issuing an SA request, the SPYDER-T must read the next two words from the register to determine which time slots need attention. After reading the channel-control blocks, the SPYDER-T reinitializes only those time slots whose corresponding bits are set in the memory maps. This procedure allows dynamic channel reconfigurations and eliminates the need to reset the SPYDER-T whenever the host changes the configuration for some of the channels. The SPYDER-T reinitializes all 32 channels if all 32 bits are set (24 channels for the T1/DS1 mode). All time slots being reinitialized should be in idle mode before the BOOT command is issued. The other time slots are not affected.
NIQ	**New Interrupt Queue.** If this bit is set, the SPYDER-T must read the new interrupt queue pointer and start from the first entry in the new queue.

Memory Interface (continued)

SPYDER-T Attention Register (continued)

Figure 8. SPYDER-T Attention Register Bit Descriptions (continued)

Symbol	Name/Description
LOOP	**Loop.** If this bit is set, the SPYDER-T enters the loopback mode. In this mode, the serial data output (TD) is internally connected to the serial data input (RD). The SPYDER-T enters the no-loop mode upon a hardware reset. In the loopback mode, link-side (serial port) timing must be provided to ensure synchronization between the transmit and receive time slots.
SWB	**Swap.** If this bit is set by the host, the upper and lower bytes of each 16-bit data word are swapped when passed between the SPYDER-T and memory. The high-order byte is stored first and the low-order byte second. If the host clears SWB, the low-order byte is stored first and the high-order byte second. This procedure affects only those data bytes stored in the transmit or receive data block.
MOD	**Mode.** If this bit is set, the SPYDER-T operates in the CEPT/E1 32-channel International mode (see Figure 7). If the MOD bit is cleared, the SPYDER-T operates in the T1/DS1 24-channel North American mode.
CA	**Channel Attention.** If this bit is set by the host, the SPYDER-T services only specific channels. The 5 bits following the CA bit represent the SPYDER-T channel number.
—	**Channel-Configuration Maps.** Each bit in these two words (4 bytes) corresponds to a unique time slot among 32 (or 24) time slots. The least significant bit (LSB) represents the first time slot, while the most significant bit (MSB) represents the last time slot. These maps are valid only when the BOOT bit is set.
IIE	**Idle Interrupt Enable.** If this bit is set, the SPYDER-T issues an interrupt IB (idle begin) and IE (idle end) for flag-to-idle and idle-to-flag transitions, respectively. If the Idle Interrupt bit is set, interrupts are reported only for those channels programmed for the HDLC mode (see Tables 18—20).
—	**Maximum Receive Frame Length.** The host uses these bits to specify the maximum number of bytes allowed for the incoming HDLC frame. This maximum number can range from 4 bytes to 8,191 bytes. If the host writes 0 to this field, the SPYDER-T enforces no limit on the length of the receive frame. In this case, the 13-bit internal counter counts to 8,191 once; the MSB of the counter remains set, and the counter continues to cycle between 4,096 and 8,191 until an end-of-frame condition is detected. It is up to the user to keep track of the frame length once it exceeds 8,191. Whatever is written into this field applies to all channels.

The host sets the BOOT, NIQ, or CA bits before issuing an SA request. After servicing the SA request, the SPYDER-T resets these bits as an acknowledgment.

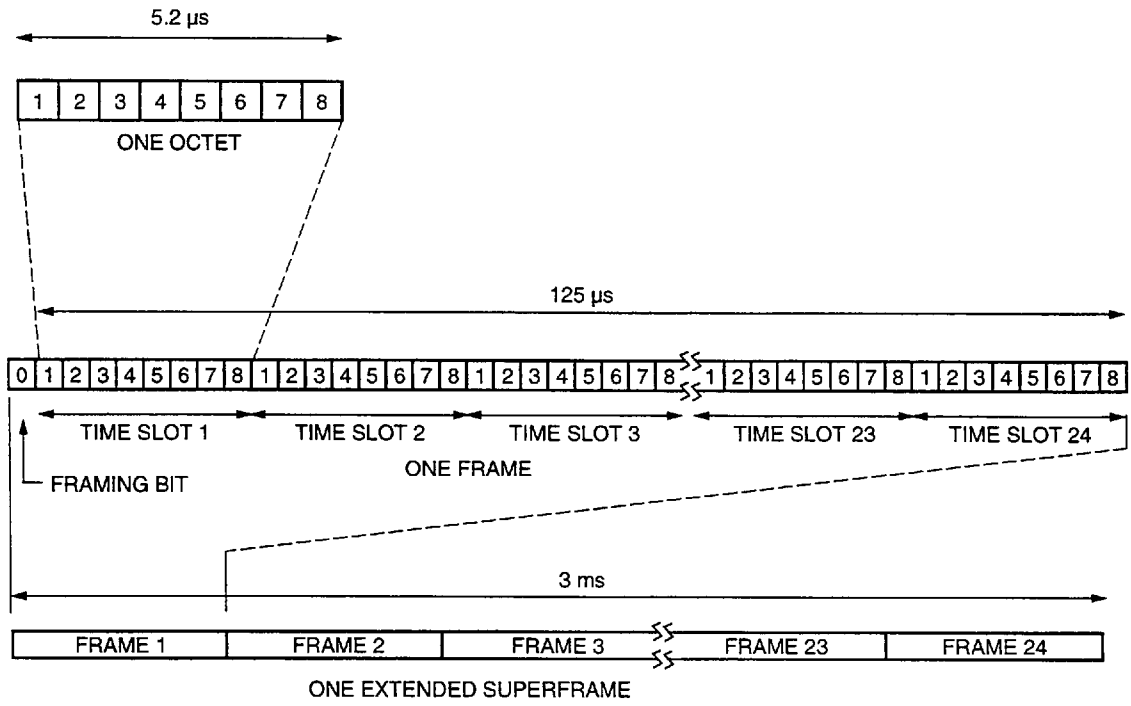
Interrupt Queue Pointer

The 16-bit interrupt queue pointer is stored in the word following the SA register. This pointer makes up the 16 MSBs of a 24-bit address that points to the beginning of the interrupt queue. The eight LSBs of the address are always 0. The interrupt queue address must be an integer multiple of the interrupt queue size (see Table 10).

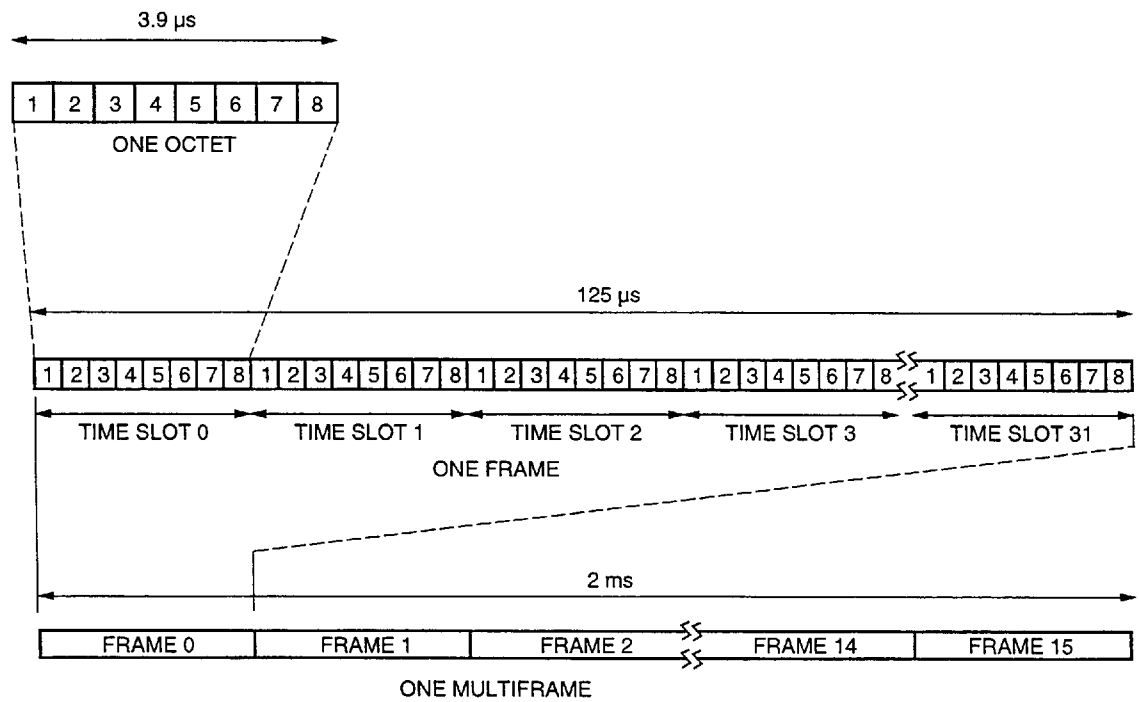
The interrupt queue size is stored in the six LSBs of the word following the interrupt queue pointer. The remaining 10 bits in this word are not used and are assumed to be 0s. The queue consists of a minimum of 128 and a maximum of 4,096 words. Each word in the queue represents an interrupt and contains a channel number and interrupt code (see Table 11). Table 13 shows the bit assignments for the interrupt code.

Memory Interface (continued)

Interrupt Queue Pointer (continued)



A. T1/DS1 24-Channel North American Mode; Bit Rate = 1.544 Mbits/s



B. CEPT/E1 32-Channel International Mode; Bit Rate = 2.048 Mbits/s

Figure 7. Frame Formats for the Primary-Rate Interface

Memory Interface (continued)

Interrupt Queue Pointer (continued)

Table 9. Bit Assignments for the Interrupt Queue Pointer and Size

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Interrupt Queue Address (high 16 bits)															
Not Used										Interrupt Queue Size					

Table 10. Interrupt Queue Size Options

Bit Number						Queue Size
5	4	3	2	1	0	
0	0	0	0	0	1	128 Words (256 bytes)
0	0	0	0	1	0	256
0	0	0	1	0	0	512
0	0	1	0	0	0	1,024
0	1	0	0	0	0	2,048
1	0	0	0	0	0	4,096

Table 11. Bit Assignments for the Interrupt Queue

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTR	—		Channel Number					Interrupt Code							

The interrupt code bits are detailed in Table 13.

Table 12. Interrupt Queue Bit Descriptions

Symbol	Name/Description
INTR	**Interrupt.** If this bit is set, an interrupt has occurred. INTR is provided for host maintenance and polling of the interrupt queue.
—	**Channel Number.** The 5-bit binary number that specifies the SPYDER-T channel number where the interrupt occurred.

When an interrupt occurs, the SPYDER-T sets the INTR bit; writes the Rx/Tx bit (in the interrupt code), channel number, and interrupt code; and then immediately issues an INT pulse. After servicing an interrupt, the host should clear the word associated with the interrupt in the interrupt queue. It is important that the queue be of sufficient size, since the queue is circular and the SPYDER-T never checks whether it is overwriting unserviced interrupts. The SPYDER-T never reads the registers in the interrupt queue. The host is responsible for ensuring that the number of interrupts accumulated does not exceed the queue size or else interrupts are lost.

If the host requires the SPYDER-T to service a new interrupt queue, it must issue an SA request after setting the NIQ bit in the SA register. The SPYDER-T then points to the first word of the new queue.

Memory Interface (continued)

Interrupt Queue Pointer (continued)

Table 13. Bit Assignments for the Interrupt Code

7	6	5	4	3	2	1	0
Rx/Tx	INT	EOL	FINT	Not Used		IB	IE

Table 14. Interrupt Code Bit Descriptions

Symbol	Name/Description
Rx/Tx	**Receive/Transmit Interrupt.** If this bit is set, an interrupt has occurred on a receive channel; if cleared, an interrupt has occurred on a transmit channel.
INT	**Interrupt.** If this bit is set, the SPYDER-T has filled a buffer in which the INT bit in the receive descriptor was set. **Note:** This bit also gets set with a receiver FINT.
EOL	**End of List.** The SPYDER-T reads the EOL bit before reading from or writing to the data buffer assigned by the current descriptor. If the SPYDER-T encounters an EOL bit set in either a transmit or receive descriptor, it generates an EOL interrupt (sets the EOL bit in the interrupt code), and the corresponding buffer is not accessed.
FINT	**Frame Interrupt.** The SPYDER-T sets this bit whenever it finishes receiving or transmitting a frame. This interrupt is nonmaskable in the receive unit but is maskable in the transmit unit.
IB	**Idle Begin.** The SPYDER-T sets this bit when it detects a flag-to-idle transition. Enabled by IIE bit in SPYDER-T attention register.
IE	**Idle End.** The SPYDER-T sets this bit when it detects an idle-to-flag transition. Idle (1) codes between 15 bits and 22 bits long may not be reported. Enabled by IIE bit in SPYDER-T attention register.

Channel-Configuration Register

The channel-configuration register resides in memory below the interrupt queue pointer and occupies 32 consecutive words. The last eight words are not used for the T1/DS1 mode. This register acts as a cross-reference, mapping physical time slots to SPYDER-T channels. This register can also be used to combine several time slots to create superchannels. In addition to the superchannels defined in the ISDN standards, any other superchannel combination can be configured (see Figures 3, 4, and 8).

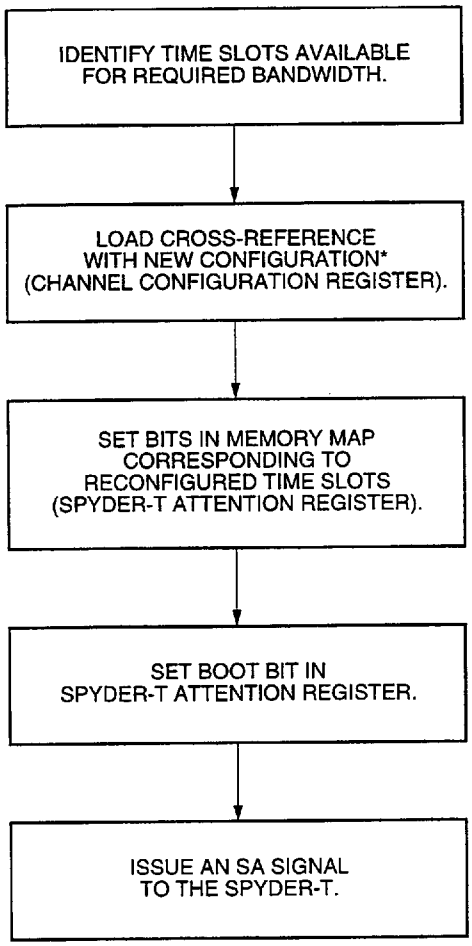
Each word in the 32-word channel-configuration register corresponds to one of the 32 multiplexed time slots. The first word in the register corresponds to the first physical time slot. The five LSBs (D4—D0) in each word determine the SPYDER-T channel number associated with that particular time slot. Superchannels are created by assigning the same channel number to several words (and therefore time slots) in the channel-configuration register.

Table 15. Channel-Configuration Register for CEPT/E1 32-Channel International Mode (MOD = 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Channel Configuration for Time Slot 0															
Channel Configuration for Time Slot 1															
: Channel Configuration for Time Slots 2—29 :															
Channel Configuration for Time Slot 30															
Channel Configuration for Time Slot 31															

Memory Interface (continued)

Channel-Configuration Register (continued)



* Channels not directly involved in the reconfiguration are not interrupted.

Figure 8. Dynamic Channel Allocation—Host Procedure

Memory Interface (continued)

Channel-Configuration Register (continued)

Table 16. Channel-Configuration Register for T1/DS1 24-Channel North American Mode (MOD = 0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Channel Configuration for Time Slot 1															
Channel Configuration for Time Slot 2															
: Channel Configurations for Time Slots 3—23 :															
Channel Configuration for Time Slot 24															
: Not Used (8 words) :															

Table 17. Bit Assignments for the Channel-Configuration Register

Information in the channel-configuration register is read into the on-chip memory upon a hardware reset or after a BOOT command.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used											Channel Number				

The following three examples show various SPYDER-T channel configurations. The numbers in these examples represent the SPYDER-T channel numbers in the channel-configuration register.

Example 1: 32 different channels in the CEPT/E1 mode

←0→←1→←2→←- - - - - - - - - -→←29→←30→←31→←0→

Example 2: Superchannel configuration for four 384 kbyte channels in the T1/DS1 mode

←0→←0→←0→←0→←0→←0→←1→ ←1→←1→←1→←1→←1→←2→←2→
←2→←2→←2→←2→←3→←3→←3→←3→←3→←3→←0→

Example 3: ISDN 23 B+D primary-rate configuration in the T1/DS1 mode

←B0→←B1 ←B2→←- - - - - - - - - -→←B21→ ←B22→←D→←B0→

Channel-Control Block

There are 32 channel-control blocks (CCB), each occupying eight words (16 bytes). Table 18 shows the CCB bit assignments. The CCBs are configured sequentially, starting with SPYDER-T channel 0. The last eight CCBs (64 words) are not used for the T1/DS1 mode.

Table 18. Channel-Control Block

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Channel-control Register															
Control Mask								Channel Command							
Not Used								First Transmit Descriptor Address (high 8 bits)							
First Transmit Descriptor Address (low 16 bits)															
Not Used								First Receive Descriptor Address (high 8 bits)							
First Receive Descriptor Address (low 16 bits)															
Not Used															
Not Used															

Memory Interface (continued)

Channel-Control Block (continued)

The control bits in the channel-control register determine the modes of operation for the channel (HDLC, non-HDLC, rate adaption, channel invert, etc.).

Table 19. Bit Assignments for the Channel-Control Register

15	14	13	12	11	10	9	8—4*	3	2	1	0
HDLC	TMODE	RTA	INV	TxOFF	RxOFF	FR	—	HCRC	HDR2—0		

* Bits D8—D4 are not used.

Table 20. Channel-Control Register Bit Descriptions

Symbol	Name/Description
HDLC	**HDLC Formatting.** If this bit is set, the SPYDER-T performs HDLC formatting functions on this channel. If this bit is cleared, HDLC formatting is not performed (i.e., transparent mode).
TMODE	**Transparent Mode.** If this bit is set, transparent mode 1 is selected. If this bit is cleared, transparent mode 0 is selected. In either case, the HDLC bit must be 0. The SPYDER-T performs no protocols and continues sending and receiving data as instructed in the frame descriptors. When the channel is in the HDLC mode, the TMODE bit must be cleared. (See Table 21.)
RTA	**Rate Control.** If this bit is set, the current channel is rate adapted. The control mask specifies which bits within the associated 8-bit time slot are not used (masked) for transmission. Conversely, it also specifies which bits in the associated time slot are used (unmasked) for transmission. If RTA is cleared, all 8 bits in the associated time slot are used, and the byte in the control mask is used as a fill character.
INV	**Inverted.** If this bit is set, all data transmitted from or received by the SPYDER-T is inverted.
TxOFF	**Transmit Off.** If this bit is set, the serial port output for the current channel is 3-stated.
RxOFF	**Receive Off.** If this bit is set, internal operations for the current receive channel are disabled, and a bus cycle access to the external memory does not occur.
FR	**Flag Adjust.** If this bit is set and the SPYDER-T is operating in HDLC mode, the transmit unit adjusts the FCNT to compensate for the number of bits stuffed in the previous frame. FCNT can be automatically adjusted by up to eight flags in order to compensate for up to 64 bit-stuffing operations. If FR is set and the SPYDER-T is operating in one of the transparent modes, the receive unit removes from the received data any occurrence of the fill character specified in the control mask. The RTA bit must be cleared when the channel is in transparent mode 0 if the FR bit is set.
HCRC	**CRC on Header.** If this bit is set, the CRC is calculated on the header bytes only. This bit is used for receive channels only.
HDR2—0	**Header Byte Count.** This 3-bit binary number specifies how many header bytes the SPYDER-T puts in the frame. If the HCRC bit is set, the CRC is performed only on the header bytes specified by HDR2 0. These bits are used for receive channels only.

Memory Interface (continued)

Channel-Control Block (continued)

The control bits HDLC, TMODE, RTA, and FR in the channel-control register select the mode of operation for each channel.

Table 21. SPYDER-T Mode Selection

Bits				Mode*	Description	Applications
HDLC	TMODE	RTA	FR			
0	0	1	0	Transparent Mode 0	Clear subrate channel selected; flag filtering and adjustment not available.	—
0	0	0	0	Transparent Mode 0	64 kbits/s clear channel; Mode 0: flag filtering and adjustment not available.	DMI Mode 0; DMI BOS
0	0	0	1	Transparent Mode 0	64 kbits/s clear channel; flag filtering selected.	DMI Mode 1†
0	1	1	0	Transparent Mode 1	Rate adaption selected.	ITU-T I.463; ECMA 102 (RA2)
1	0	1	0	HDLC	Subrate HDLC channel; flag adjustment not selected.	Subrate HDLC Channel
1	0	1	1	HDLC	Subrate HDLC channel; flag adjustment selected.	Subrate HDLC Channel
1	0	0	1	HDLC	64 kbits/s HDLC channel; flag adjustment selected.	DMI Mode 2 Sync/Asyn
1	0	0	0	HDLC	64 kbits/s HDLC channel; flag adjustment not selected.	—

* The flag adjustment applies to the HDLC mode transmit channels only.
† The flag filtering based on the control-mask register applies to the transparent mode receive channels only.

The SPYDER-T always writes the CRC bytes in the shared memory after receiving a frame. The CRC bytes for the transmit channels are calculated by the SPYDER-T, and the CRC bytes for the receive channels are the last 2 bytes of the HDLC frame received.

The control mask performs two functions: it controls the bit rate and provides the fill character. The control mask determines the number of bits per channel and the position of these bits in the channel (if RTA is set). If RTA is cleared and FR is set, the control mask is used as the fill character. The fill character is used only in the transparent modes (see Table 21).

If RTA is set, a 0 in the control mask means that the corresponding bit in the serial output stream is 3-stated; a 1 in the control mask means that the corresponding output bit is valid.

This feature allows the SPYDER-T to be set up for many different communication configurations. For instance, four SPYDER-Ts, each with 2 bits set in their control masks, can handle 128 sixteen kbits/s channels. Typical uses of the control mask are shown in the following examples.

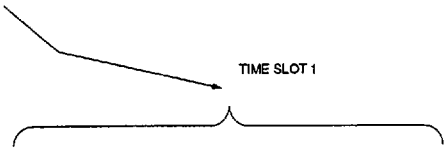
Memory Interface (continued)

Channel-Control Block (continued)

Example 1. The control mask for a 16 kbits/s channel (RTA = 1):

15	14	13	12	11	10	9	8
0	0	0	0	1	1	0	0

←0→←1→←2→←- - - - - - - - - - - - - →←29→←30→←31→←0→



←Ts 0→←Z→←Z→←bit 0→←bit 1→← Z→← Z→← Z→← Z→←Ts 2→

Example 2. The control mask for fill character 0x7F (RTA = 0):

15	14	13	12	11	10	9	8
0	1	1	1	1	1	1	1

The channel command byte allows the host to define a number of commands that the SPYDER-T must execute for that channel. Multiple channel commands cannot be stacked, so they should generally be used for exceptional conditions (e.g., retransmission). Extending the transmit and receive queues can easily be done by moving the set EOL bit.

Table 22. Bit Assignments for the Channel Command Byte

7	6	5	4	3	2	1	0
IDLE	TxABT	RxABT	Not Used		TxHLT	RQD	TQD

Table 23. Channel-Control Block Command Byte and Descriptor Address Bit Descriptions

Symbol	Name/Description
IDLE	**Idle.** If this bit is set, the transmitter sends idle codes after the closing flag of the current frame. If the SPYDER-T is currently transmitting flags, it begins idling immediately after servicing this command. This procedure is used when the host wants the transmitter to idle immediately instead of waiting for the transmitter to read the next transmit descriptor with IDL set. If the SPYDER-T is waiting for TQD to be set, a CA command is not necessary to assert the IDLE.
TxABT	**Transmit Abort.** If this bit is set, the transmitter aborts the current frame and either idles (IDLE is set) or begins sending flags (IDLE is cleared).
RxABT	**Receive Abort.** If this bit is set, the receiver aborts the current frame. After aborting the frame, the SPYDER-T polls the channel command register until RQD is set. The host should not issue another SA request when it sets RQD.
TxHLT	**Transmit Halt.** If this bit is set, the transmit unit completes sending the current frame and then either idles or sends flags until the host sets the TQD. The host should not issue a second SA request for retransmission, since the SPYDER-T polls TQD during channel service.

Memory Interface (continued)

Channel-Control Block (continued)

Table 23. Channel-Control Block Command Byte and Descriptor Address Bit Descriptions (continued)

Symbol	Name/Description
RQD	**Receive Queue Define.** If this bit is set, the receiver reads a new receive descriptor address from the current CCB and then reads the contents of that descriptor. This procedure is performed after the current frame is completed unless RxABT is also set.
TQD	**Transmit Queue Define.** If this bit is set, the transmitter reads the new transmit descriptor address from the current CCB and then reads the contents in that descriptor. The SPYDER-T then begins transmitting a new sequence of frames. This procedure is performed after the current frame is completed unless the TxABT bit is also set. No frames are sent until TQD is set following a reset.
—	**Transmit Descriptor Address.** This 24-bit pointer contains the starting address of the first transmit descriptor. If the TQD bit in the channel command register is set, the SPYDER-T reads this pointer (see Table 18).
—	**Receive Descriptor Address.** This 24-bit pointer contains the starting address of the first receive descriptor. If the RQD bit in the channel command register is set, the SPYDER-T reads this pointer (see Table 18).

Transmit Descriptor for the HDLC Mode

The transmit descriptor (TD) consists of a buffer address, byte count (CNT), fill-flag count (FCNT), control bits, and the address of the next descriptor. After sending the opening flags, the SPYDER-T begins transmitting data from the current transmit buffer (only if EOL is cleared). The buffer's CNT is stored in the SPYDER-T's on-chip memory and is decremented by one after each byte in the buffer is transmitted. The CNT is used exclusively by the SPYDER-T and is not transmitted.

If the EOF bit is cleared when CNT decrements to 0, the SPYDER-T accesses the next TD and continues sending data as a continuous frame. As the SPYDER-T begins transmitting data from the new data buffer, the new TD's CNT is loaded and decremented accordingly. A single large frame may use several TDs to store its data. To simplify the handling of a large frame, the frame's header and information field bytes can be stored separately. In this case, the header bytes are stored in one TD, while the information field bytes are stored in one or more other TDs.

If the EOF bit is set when CNT decrements to 0, the SPYDER-T sends a closing flag and then reads the FCNT in the TD. The SPYDER-T then sends FCNT + 1 flags between frames, updates the status, and reads the transmit descriptor address for the next frame. The functions described above are repeated until the host issues a CA request. If FR is set, FCNT should be chosen so that the adjusted value of FCNT is always greater than 0.

Table 24. Transmit Descriptor for the HDLC Mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EOF	HCRC	EOL	CNT												
Not Used								Transmit Buffer Address (high 8 bits)							
Transmit Buffer Address (low 16 bits)															
Not Used								Next Transmit Descriptor Address (high 8 bits)							
Next Transmit Descriptor Address (low 16 bits)															
FINT	—	IDL	DCRC	—	FCNT										
Not Used								Status							

Memory Interface (continued)

Transmit Descriptor for the HDLC Mode (continued)

Table 25. Transmit Descriptor Bit Descriptions

Symbol	Name/Description
EOF	**End of Frame.** If this bit is set, this indicates that the frame ends after this buffer is transmitted. The SPYDER-T then performs a CRC and transmits the result at the end of the frame (only if DCRC is cleared). If this bit is cleared, the SPYDER-T continues the frame by ignoring the last two words in the current TD and accessing the next TD.
HCRC	**CRC on Header.** If this bit is set, the CRC is calculated on data bytes in the buffer.
EOL	**End of List.** If this bit is set by the host, the current TD is the last in the list for this channel. The SPYDER-T reads this bit before entering the buffer and interrupts the host if it is set. The SPYDER-T polls this bit until this bit is cleared by the host. A continuous string of either flag or idle characters is transmitted by the SPYDER-T until this bit is cleared. When this bit is finally cleared, the SPYDER-T reads the current TD's parameters and begins transmitting data from the current buffer. Consequently, it is not necessary to issue an SA request to restart transmission after the SPYDER-T encounters this bit set. This should be the mechanism used to extend the queues.
CNT	**Byte Count.** The CNT specifies the number of bytes in the data buffer to be transmitted. The host writes the CNT into the TD ($2 \leq CNT \leq 8,191$).
—	**Transmit Buffer Address.** This 24-bit address points to the starting address of the transmit buffer. **Note:** Like all pointers within shared memory, the printer must point to a word boundary (A0 = 0).
—	**Next Transmit Descriptor Address.** This 24-bit address points to the starting address of the next TD. If the next TD address of the last TD points to the starting address of the first TD in a chain, the SPYDER-T operates in a circular-queue fashion.
FINT	**Frame Interrupt.** If this bit is set by the host, the SPYDER-T interrupts at the end of the frame (EOF is set).
IDL	**Idle.** If this bit is set by the host, the SPYDER-T transmits the number of idle bytes specified in FCNT after this frame.
DCRC	**Discard CRC.** If this bit is set, the CRC bytes are not appended to this frame (see Figure 9).
FCNT	**Flag Count.** FCNT + 1 specifies the number of flags the SPYDER-T inserts between frames. In the HDLC mode, if the IDL bit is set, idle characters (11111111) are sent in place of the extra flags. In the transparent modes, the SPYDER-T transmits the flags defined in the control mask. In this case, FCNT specifies the number of flags the SPYDER-T must transmit after the last byte of the current descriptor and before the first byte of the next descriptor. If flag adjustment is selected in the HDLC mode, the SPYDER-T may reduce FCNT to compensate for stuffed bits. If FCNT = 0, a single flag is shared between two frames. **Exception:** An FCNT value of 1 gives three flags between frames. It is not possible to get only two flags between frames such that each frame has its own opening and closing flag.

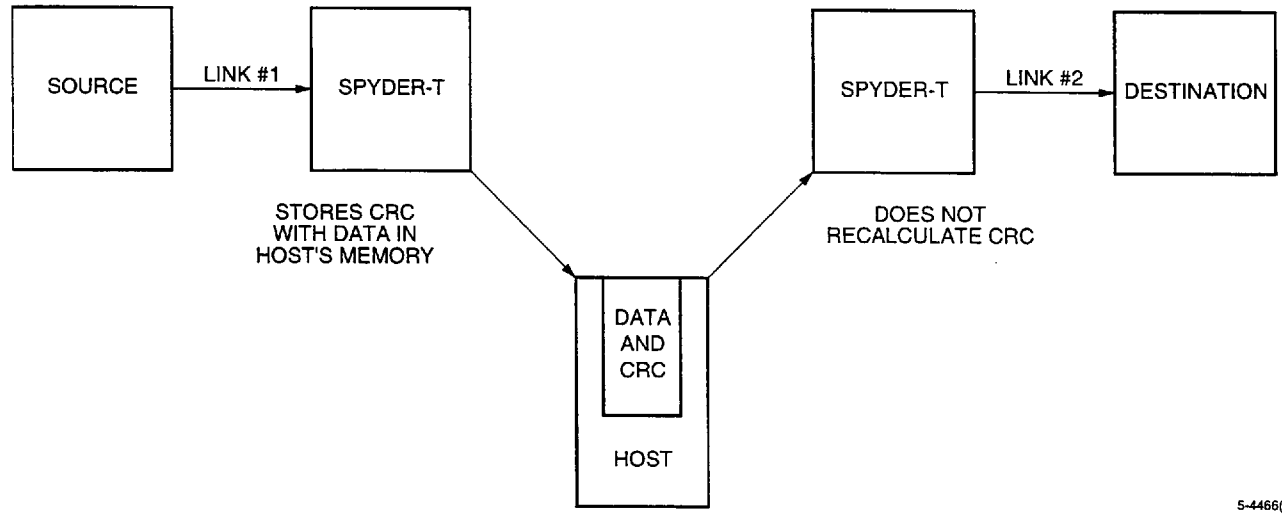
The SPYDER-T writes the status bits in the TD after transmitting the entire data buffer. These status bits indicate whether the current descriptor was successfully transmitted or whether it was aborted. Therefore, the host must clear the status bits before placing the TD in the transmit queue.

Table 26. Transmit Status

7	6	5	4	3	2	1	0
TFC	ABT	Not Used					

Memory Interface (continued)

Transmit Descriptor for the HDLC Mode (continued)



Note: In relay mode, the SPYDER-T retransmits the same CRC value it received to guard against the introduction of errors by the host memory.

Figure 9. SPYDER-T in Relay Mode

Table 27. Transmit Status Bit Descriptions for the HDLC Mode

Symbol	Name/Description
TFC	**Current Frame Transmitted.** If this bit is set, the SPYDER-T has completed transmission of the current frame.
ABT	**Current Frame Aborted.** If this bit is set, the SPYDER-T has aborted the current frame while transmitting from the current buffer. After an abort, the SPYDER-T polls TQD in the channel command byte until it is set by the host.

Transmit Descriptor for the Transparent Modes

Transparent mode TDs are almost identical to HDLC mode TDs except that three control bits (HCRC, IDL, and DCRC) are not used. The SPYDER-T does not send any opening or closing flags, but if EOF is set, it transmits the number of flag bytes (defined in the control mask) specified in FCNT. It is possible to have a TD point to itself as the next TD and continuously transmit the same data buffer (see Table 28). This procedure can be useful in some transparent modes.

The host sets INT to interrupt the SPYDER-T at the end of the current buffer. If EOL is set, the SPYDER-T transmits a continuous string of flags (defined in the control mask) until EOL is cleared by the host.

Memory Interface (continued)

Transmit Descriptor for the Transparent Modes (continued)

Table 28. Transmit Descriptor for the Transparent Modes

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EOF	—	EOL	CNT												
Not Used								Transmit Buffer Address (high 8 bits)							
Transmit Buffer Address (low 16 bits)															
Not Used								Next Transmit Descriptor Address (high 8 bits)							
Next Transmit Descriptor Address (low 16 bits)															
INT	—							FCNT							
Not Used								Status							

Table 29. Transmit Status Bit Descriptions for the Transparent Modes

Symbol	Name/Description
TFC	**Current Frame Transmitted.** If this bit is set, the SPYDER-T has completed transmitting the current buffer.
ABT	**Current Frame Aborted.** If this bit is set, the SPYDER-T has aborted the frame while transmitting the current buffer.

Receive Descriptor

The receive descriptor (RD) provides the byte count (CNT) and status of the receive frames, while the host provides the address of the next RD. The host also allocates a block of memory, or buffer, for the current RD, which immediately follows the descriptor. The SPYDER-T writes the received data bytes into this buffer until either the receive unit's BCNT is cleared or a closing flag is received. The SPYDER-T then returns to the receive descriptor, writes the status and CNT, and updates the EOF and C bits.

When the SPYDER-T receives a frame of data longer than the allocated buffer, it sets C, writes the CNT, and accesses the next RD. The SPYDER-T continues writing the received data in the buffer assigned by the new RD. The status of the received frame is written to the RD being used when the end-of-frame condition is detected.

Table 30. Receive Descriptor

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EOF	C	—	CNT												
Not Used															
Not Used															
Not Used								Next Receive Descriptor Address (high 8 bits)							
Next Receive Descriptor Address (low 16 bits)															
INT	EOL	—	BCNT												
Not Used								Status							
Receive Buffer															

Memory Interface (continued)

Receive Descriptor (continued)

Table 31. Receive Descriptor Bit Descriptions

Symbol	Name/Description
EOF	**End of Frame.** If this bit is set, the current frame has ended in this descriptor's buffer. If EOF is cleared, the frame continues in the next descriptor buffer.
C	**Complete.** If this bit is set, the SPYDER-T has completed filling the current descriptor buffer. If C is set and EOF is cleared, this frame continues in the next buffer. If both C and EOF are set, the frame and the current buffer have ended, and the frame is now ready for host processing. The SPYDER-T clears the C bit when it reads this descriptor and sets the C bit when it completes filling the buffer.
CNT	**Byte Count.** The SPYDER-T writes the number of bytes it has received in CNT. CNT reflects the total number of bytes received for the current frame regardless of the number of RDs needed to store that frame. When multiple RDs are used, the host may need to perform a subtraction to determine the number of bytes in the last descriptor buffer. If the current descriptor's EOF bit is set, CNT represents the final number of bytes received for the frame. The CNT includes the two CRC bytes stored in the buffer in the HDLC mode.
—	**Next Receive Descriptor Address.** This 24-bit address points to the starting address of the next RD. If the next RD address of the last RD points to the starting address of the first RD in a chain, the SPYDER-T operates in a circular-queue fashion.
INT	**Interrupt.** If this bit is set, the SPYDER-T interrupts at the end of the buffer. If the SPYDER-T receives an end-of-frame command (the closing flag), it interrupts without regard to INT.
EOL	**End of List.** If this is set, the SPYDER-T is prevented from writing to this buffer. The EOL bit must be cleared by the host before the SPYDER-T can begin writing to this buffer. If, while receiving a frame, the SPYDER-T encounters a receive descriptor with EOL set, the SPYDER-T aborts the receive frame. The SPYDER-T then makes the following modifications to the previous receive descriptor the EOF and C bits are set, the total number of bytes successfully stored in the frame are written in the CNT field, and then the abort (ABT) bit is set in the receive status field. An EOL interrupt is then generated by the SPYDER-T. The SPYDER-T polls the EOL bit until the bit is cleared by the host. Once the EOL bit is cleared, the SPYDER-T waits until it begins receiving a new frame.
BCNT	**Buffer Count.** The BCNT specifies the number of bytes (minimum four) allocated by the host for the receive buffer.

Note: When the SPYDER-T accesses a receive descriptor, it will always clear the first word in the descriptor (EOF, C, and CNT fields) even if the EOL bit is set.

If the maximum receive frame-length field of the SA register is 0, the SPYDER-T enforces no limit on the length of the receive frame. However, once the count exceeds 8,191, it is up to the user to keep track of the frame length. In this case, the MSB of the CNT remains set and the value stored in CNT cycles between 4,096 and 8,191 until an end-of-frame condition is detected.

The SPYDER-T writes to the status byte in the RD when it detects an end-of-frame, abort, or long-frame condition. The short frames (1, 2, or 3 bytes long) are discarded, and no status is reported.

Table 32. Bit Assignments for the Receive Status

7	6	5	4	3	2	1	0
GRF	BRF	BBC	ABT	LFR	Not Used		

Memory Interface (continued)

Receive Descriptor (continued)

Table 33. Receive Status Bit Descriptions

Symbol	Name/Description
GRF	**Good CRC.** If this bit is set, the CRC for the received frame is correct (good). In transparent mode 1, all complete frames are reported as correct.
BRF	**Bad CRC.** If this bit is set, the CRC for the received frame is incorrect (bad).
BBC	**Partial Byte Received.** If this bit is set, this indicates that a partial byte has been received. The frame's CRC status can still be good or bad.
ABT	**Abort.** If this bit is set, this indicates that the frame has been aborted.
LFR	**Long Frame Received.** If this bit is set, this indicates that a long frame (exceeding N1 bytes) has been received. N1 resides in the SPYDER attention register and is programmable up to 8,191 bytes. Upon receiving a long frame, the SPYDER-T sets the EOF and C bits, writes the CNT to the RD, and writes 0x08 to the status byte. When a closing flag is received, the status byte is updated to show the final status of the frame (0x88 for a good long frame or 0x48 for a bad long frame).

Receive Descriptor for Transparent Mode 0

The RD for transparent mode 0 is identical to the RD for the HDLC mode except for the status byte. The RD status byte for transparent mode 0 is shown below.

Table 34. Receive Status for Transparent Mode 0

7	6	5	4	3	2	1	0
Not Used			ABT	Not Used			

Reset and Initialization

Following a hardware reset, the SPYDER-T's serial data output is 3-stated, and its receive channels are disabled. The SPYDER-T remains in this state until after it receives an SA pulse. The SPYDER-T's internal registers and counters are reset by a hardware reset. The internal DMA registers are set to 0xFFFFFC, which points to the SPYDER-T configuration pointer.

The SPYDER-T reads the SA register, interrupt queue pointer, channel-configuration register, and all of the channel-control blocks. All internal registers, memories, and counters are then initialized. Thus, it is essential that the host initialize the entire control block before issuing the SA pulse. SPYDER-T initialization takes approximately 200 µs for the 32-channel mode and 150 µs for the 24-channel mode.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability. External leads can be bonded or soldered safely at temperatures up to 300 °C.

Parameter	Symbol	Min	Max	Unit
Voltage on Any Pin with Respect to Ground (Vss)	—	–0.5	7	V
Input Voltage	V_I	V_{SS} – 0.5	V_{DD} + 0.5	V
Storage Temperature	T_{stg}	–40	125	°C
Power Dissipation	P_D	—	800	mW

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection-design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters:

HBM ESD Threshold	
Device	**Voltage**
T7115A	1500 V

Electrical Characteristics

T_A = 0 °C to 70 °C or –40 °C to +85 °C (see Ordering Information), V_{DD} = 5 V ± 5%, V_{SS} = 0 V.

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Current:					
High	I_{IH}	$V_{IH} = V_{DD}$	—	7.5	A
Low	I_{IL}	V_{IL} = 0 V	—	7.5	A
Input Current (bidirectional pins):					
High	I_{IH}	$V_{IH} = V_{DD}$	—	37.5	A
Low	I_{IL}	V_{IL} = 0 V	—	37.5	A
Output 3-state (leakage current):					
High	I_{OZH}	$V_{OH} = V_{DD}$	—	30	A
Low	I_{OZL}	V_{OL} = 0 V	—	30	A
Input Voltage:					
High	V_{IH}	—	2.0	—	V
Low	V_{IL}	—	—	0.8	V
Output Voltage:					
High	V_{OH}	I_{OH} = 2.4 mA	2.4	—	V
Low	V_{OL}	I_{OL} = 2.4 mA	—	0.4	V
Power Dissipation	P_D	tCKHCKH = 60 ns, 100 pF load	—	650	mW

Timing Characteristics

C_L = 100 pF (all pins), 0 °C to 70 °C or –40 °C to +85 °C (see Ordering Information), V_{DD} = 5 V ± 5%, V_{SS} = 0 V.

Table 35. Timing Characteristics for Serial Data

Symbol	Parameter	Min	Max	Unit
tTKHTKH	TCLK Period (steady)	8tCKHCKH	100,000	ns
tTKHTKH	TCLK Period (burst)	4tCKHCKH*	—	ns
tTKHTKL	TCLK High	2tCKHCKL	—	ns
tTKLTKH	TCLK Low	2tCKLCKH	—	ns
tTKLTDV	Transmit Data Valid	10	45	ns
tTKLTDH	Transmit Data Hold	10	—	ns
tTKLTDZ	TD Float Delay	5	30	ns
tRKHRKL	RCLK High	2tCKHCKL	—	ns
tRKLRKH	RCLK Low	2tCKLCKH	—	ns
tRDVRKH	Receive Data Setup Time	15	—	ns
tRKHRDV	Receive Data Hold Time	15	—	ns
tTSYVTKH	TISYN Setup Time	5	—	ns
tTKHTSYV	TISYN Hold Time	15	—	ns
tRSYVRKH	RISYN Setup Time	5	—	ns
tRKHRSYV	RISYN Hold Time	15	—	ns
tRKHRKH	RCLK Period (steady)	8tCKHCKH	100,000	ns
tRKHRKH	RCLK Period (burst)	4tCKHCKH*	—	ns

* To prevent overrun/underrun conditions, the frequency of the system clock must be at least eight times the aggregate frequency of the serial line clock for any time slot.

Timing Characteristics (continued)

Table 36. Timing Characteristics for SPYDER-T Memory Interface

Symbol	Parameter	Min	Nom	Max	Unit
tCKHCKH	Input Clock Period[1]	60	—	—	ns
tCKLCKH	Clock Low Time	28	—	—	ns
tCKHCKL	Clock High Time	28	—	—	ns
tDRQLDRQH	$\overline{\text{DREQ}}$ Active Width	4tCKHCKH	—	—	ns
tDAKLSET	$\overline{\text{DACK}}$ to CLK Setup Time	45[2]	—	—	ns
tDAKLDAKH	$\overline{\text{AVAL}}$ Active Time	3.5tCKHCKH[3]	—	—	ns
tDAKLAVL	$\overline{\text{DACK}}$ to $\overline{\text{AVAL}}$ Delay	13	—	6tCKHCKH	ns
tDAKHDRQL	$\overline{\text{DACK}}$ to $\overline{\text{DREQ}}$ Delay	10[4]	—	—	ns
tDRQLDLY	CLK to $\overline{\text{DREQ}}$ Delay	—	—	60[5]	ns
tDRQLDAKL	$\overline{\text{DREQ}}$ to $\overline{\text{DACK}}$ Delay	—	—	6tCKHCKH[6]	ns
tADRVAVL	Address Valid	40	—	—	ns
tAVLAVH	Active Width	2.5tCKHCKH	—	—	ns
tAVHAVL	Intercycle Spacing	1.5tCKHCKH	—	—	ns
tAVLAVL	$\overline{\text{AVAL}}$ Cycle Time	4tCKHCKH	—	—	ns
tAVLDATV	Read Access Time	—	—	(3tCKHCKH) – 63	ns
tAVHADX	$\overline{\text{AVAL}}$ Address Hold Time	0.5tCKHCKH	—	—	ns
tREHADX	$\overline{\text{RE}}$ Address Hold Time	0[7]	—	—	ns
tWEHADX	$\overline{\text{WE}}$ Address Hold Time	tCKHCKH	—	—	ns

1. To prevent overrun/underrun conditions, the frequency of system clock must be at least eight times the aggregate frequency of serial line clock over any time slot.
2. Setup time defined relative to positive clock edge only.
3. $\overline{\text{DACK}}$ should be maintained until $\overline{\text{DREQ}}$ goes inactive.
4. Once $\overline{\text{DREQ}}$ has gone inactive, the bus will not be requested again until $\overline{\text{DACK}}$ goes inactive.
5. Delay time defined relative to positive clock edge only.
6. This requirement assumes a system clock to serial clock ratio of 8:1. If R = (system clock frequency/serial clock frequency), this figure may be increased by 8(R – 8).
7. Guarantees that address is valid through entire $\overline{\text{RE}}$ cycle.

Timing Characteristics (continued)

Figure 36. Timing Characteristics for SPYDER-T Memory Interface (continued)

Symbol	Parameter	Min	Nom	Max	Unit
tREHDATV	Read Data Hold Time	0	—	—	ns
tAVLREL	$\overline{AVAL}$ to $\overline{RE}$ Delay	(0.5tCKHCKH) – 5	0.5tCKHCKH	(0.5tCKHCKH) + 5	ns
tRELREH	$\overline{RE}$ Active Width	(2.5tCKHCKH) – 36	2.5tCKHCKH	(2.5tCKHCKH) + 28	ns
tREHREL	Inter-$\overline{RE}$ Spacing	(1.5tCKHCKH) + 1	—	—	ns
tRELREL	$\overline{RE}$ Cycle Time	(4tCKHCKH) – 1	4tCKHCKH	—	ns
tRELWEL	$\overline{RE}$ to $\overline{WE}$ Cycle Time	(4tCKHCKH) – 1	—	—	ns
tDATWEL	Write Setup Time	(0.5tCKHCKH) – 10	0.5tCKHCKH	(0.5tCKHCKH) + 10	ns
tWEHDATV	Write Data Hold Time	0.5tCKHCKH	—	—	ns
tAVLWEL	$\overline{AVAL}$ to $\overline{WE}$ Delay	(0.5tCKHCKH) – 5	0.5tCKHCKH	(0.5tCKHCKH) + 5	ns
tWELWEH	$\overline{WE}$ Active Width	(2tCKHCKH) – 30	2tCKHCKH	(2tCKHCKH) + 20	ns
tWELWEL	$\overline{WE}$ Cycle Time	(4tCKHCKH) – 10	4tCKHCKH	(4tCKHCKH) + 10	ns
tWELREL	$\overline{WE}$ to $\overline{RE}$ Cycle Time	(4tCKHCKH) – 1	—	—	ns
tINLINH	$\overline{INT}$ Active Width	(2tCKHCKH) – 39	2tCKHCKH	(2tCKHCKH) + 19	ns
tSAHSAL	SA High Active Width	tCKHCKH	—	—	ns
tSALSAH	SA Low Active Width	tCKHCKH	—	—	ns
tRSHRSL	RST High Active Width	2tTKHTKH	—	—	ns
tRSLRSH	RST Low Active Width	2tTKHTKH	—	—	ns

Timing Characteristics (continued)

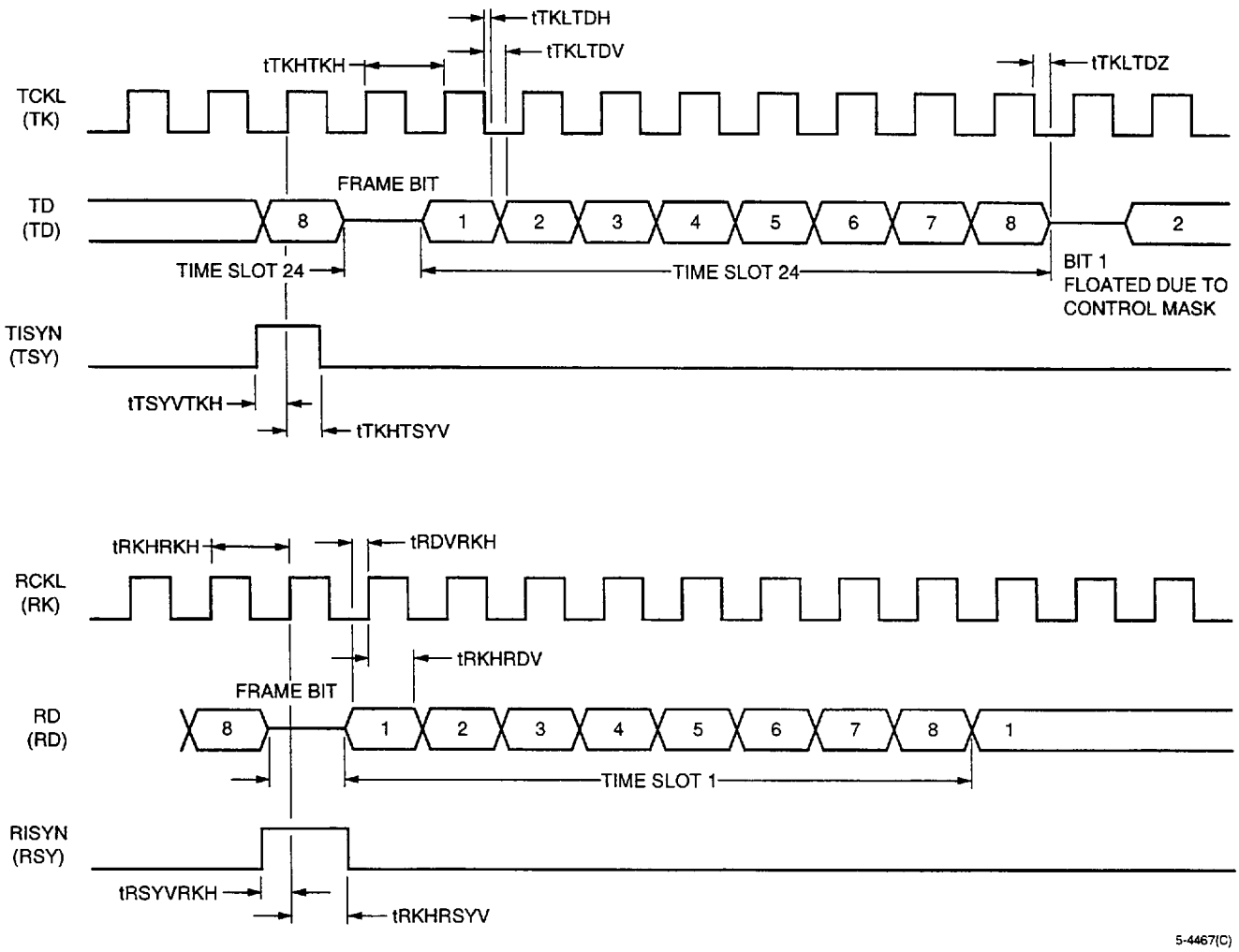


Figure 10. Serial Link Timing for T1 Mode

Timing Characteristics (continued)

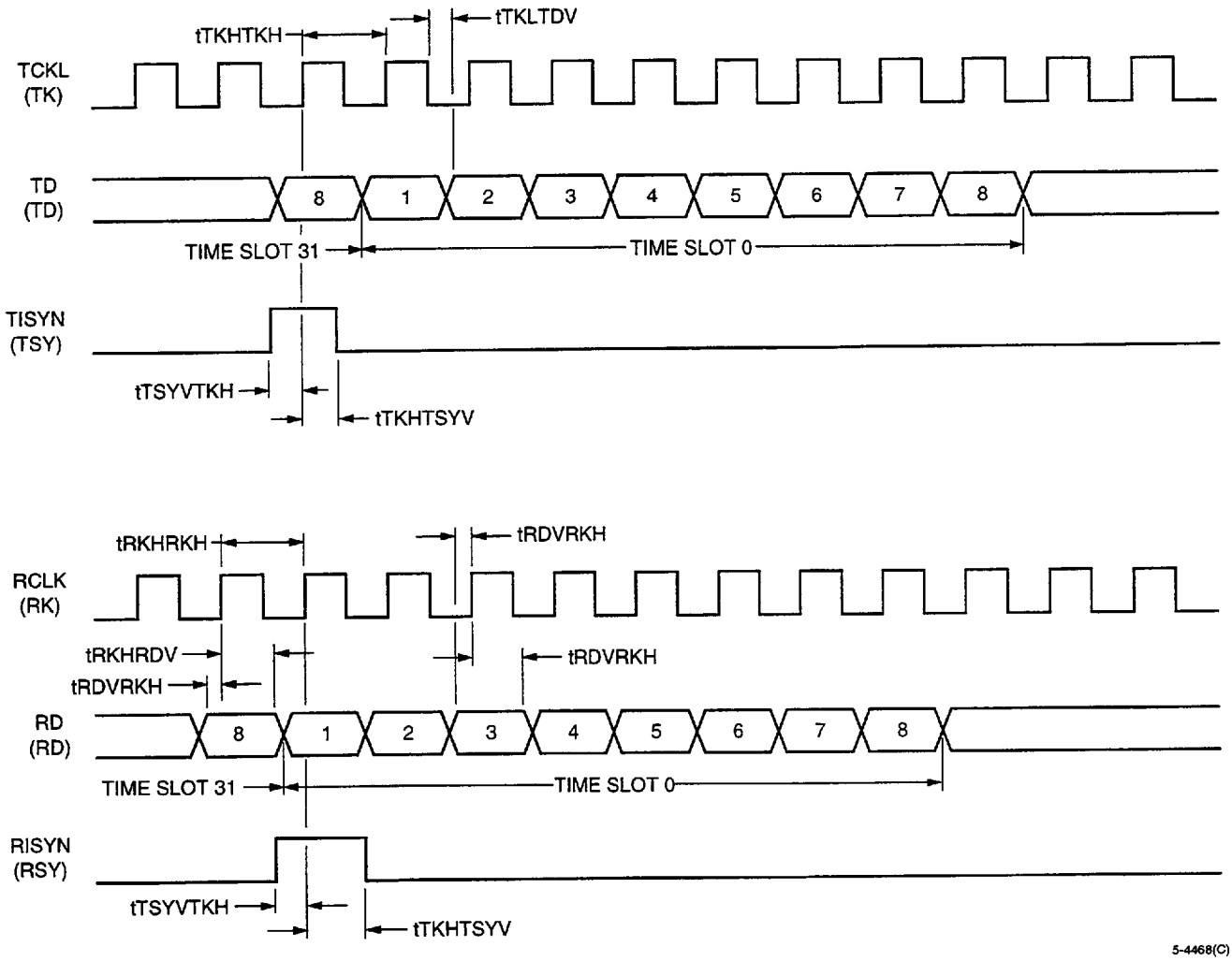
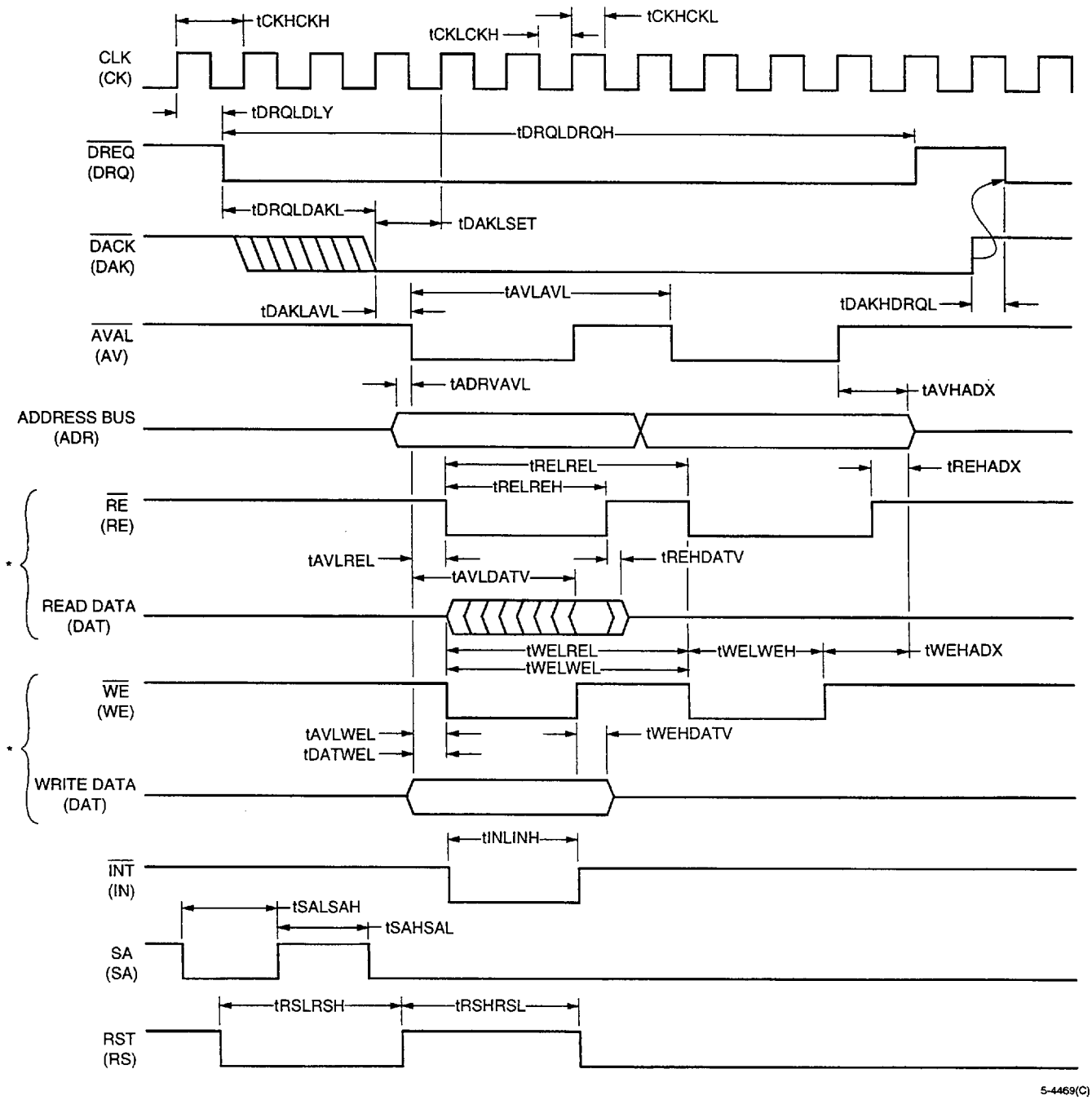


Figure 11. Serial Link Timing for CEPT/E1 Mode

Timing Characteristics (continued)



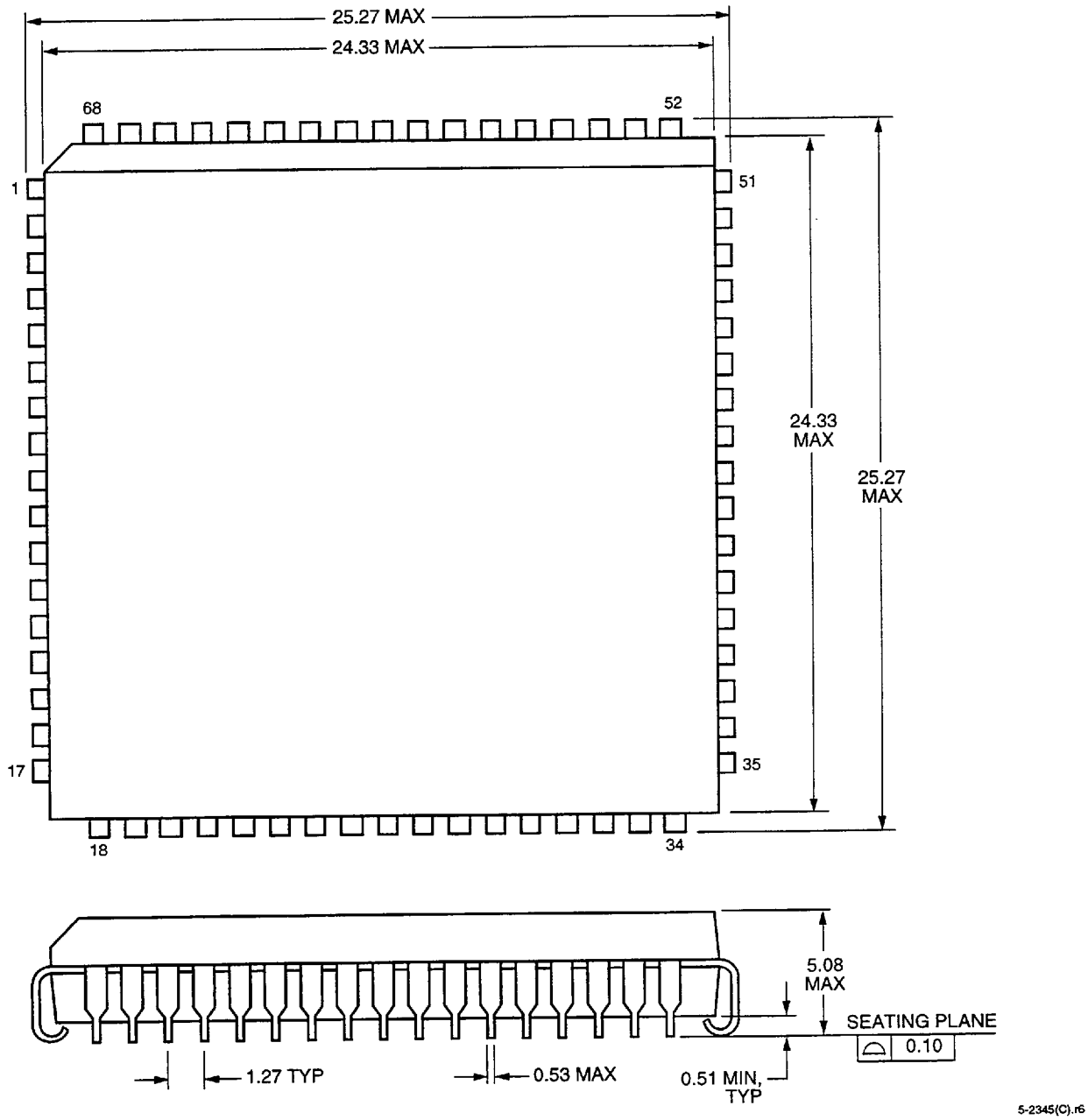
* For convenience, the data-read and data-write operations are shown together, but they do not occur simultaneously.

Figure 12. SPYDER-T to Shared-Memory Cycle Timing

Outline Diagrams

Nonindustry-Standard 68-Pin PLCC

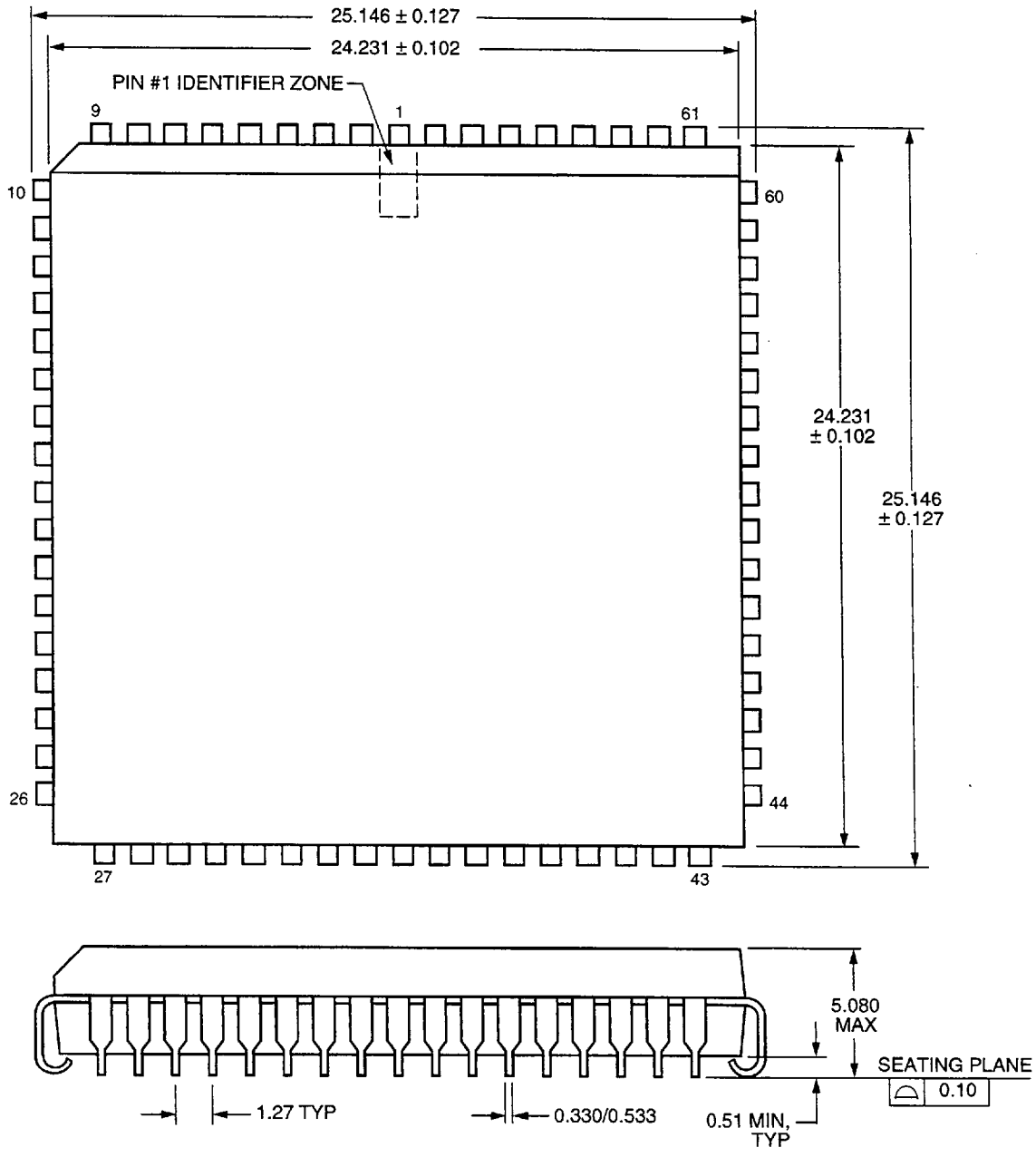
Dimensions are in millimeters.



Outline Diagrams (continued)

Industry-Standard 68-Pin PLCC

Dimensions are in millimeters.



5-2139(C).r14

Ordering Information

Device Code	Package	Temperature	Comcode (Ordering Number)
T - 7115A - - MC - D	68-Pin PLCC	0 °C to 70 °C	106039696
T - 7115A - - ML - D	68-Pin PLCC	–40 °C to +85 °C	106039704

Advisory

Under certain conditions of power supply voltage, temperature, CLK duty cycle, and HDLC frame rate, the T7115A device malfunctions. This malfunction is observed as a failure to write to the first word of a receive descriptor, i.e., the EOF, C, and CNT fields do not get updated. The data and the memory buffer structure do not get corrupted, and the device continues to process frames.

This malfunction is most likely to occur with the power supply at 4.75 V, temperature at 60 °C or higher, CLK low time less than 30 ns, and HDLC frame rates of several hundred packets per second or higher.

The probability of malfunction is device-dependent, even with devices from the same date code. Although the potential for malfunction is inherent in all devices, most devices do not malfunction.

DS97-226TIC Replaces DS92-074SMOS to Incorporate the Following Updates

1. Device advisory AY96-012TIC.
2. Page 39, revised industry-standard 68-pin PLCC outline diagram.
3. Page 40, added the comcode (ordering number) for each device code.
4. Data sheet format.

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