

Cascadable Amplifier 10 to 500 MHz

Rev. V2

Features

- HIGH POWER OUTPUT: +27.5 dBm (TYP.)
- HIGH THIRD ORDER I.P.: +39 DBm (TYP.)
- MODERATE NOISE FIGURE: 5.2 dB (TYP.)
- GaAs FET AMPLIFIER

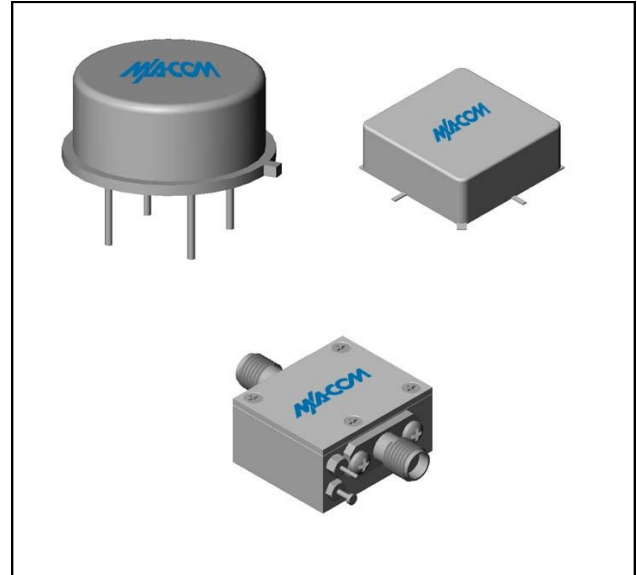
Description

The PA512 0.5 watt RF power amplifier is a discrete hybrid design, which uses thin film manufacturing processes for accurate performance and high reliability. This 2 stage GaAs FET transistor design uses a feedback loop for flat broadband performance. An active DC biasing network insures temperature-stable performance. MIL-STD-883 environmental screening is available.

Ordering Information

Part Number	Package
PA512	TO-8
SMPA512	Surface Mount
CPA512	SMA Connectorized

Product Image



Electrical Specifications: $Z_0 = 50\Omega$, $V_{CC} = +15 V_{DC}$

Parameter	Units	Typical	Guaranteed	
		25°C	0° to 50°C	-54° to +85°C*
Frequency	MHz	10-700	10-500	10-500
Small Signal Gain (min)	dB	18.0	16.0	15.0
Gain Flatness (max)	dB	±0.3	±0.7	±1.0
Reverse Isolation	dB	24		
Noise Figure (max)	dB	5.2	6.0	6.5
Power Output @ 1 dB comp. (min)	dBm	27.5	26.0	25.5
IP3	dBm	+33		
IP2	dBm	+45		
Second Order Harmonic IP	dBm	+50		
VSWR Input / Output (max)		1.4:1 / 2.0:1	1.8:1 / 2.2:1	2.0:1 / 2.3:1
DC Current @ 15 Volts (max)	mA	200	210	220

Absolute Maximum Ratings

Parameter	Absolute Maximum
Storage Temperature	-62°C to +150°C
Case Temperature	+85°C
DC Voltage	+17 V
Continuous Input Power	+17 dBm
Short Term Input power (1 minute max.)	100 mW
Peak Power (3 µsec max.)	0.5 W
"S" Series Burn-In Temperature (case)	+85°C

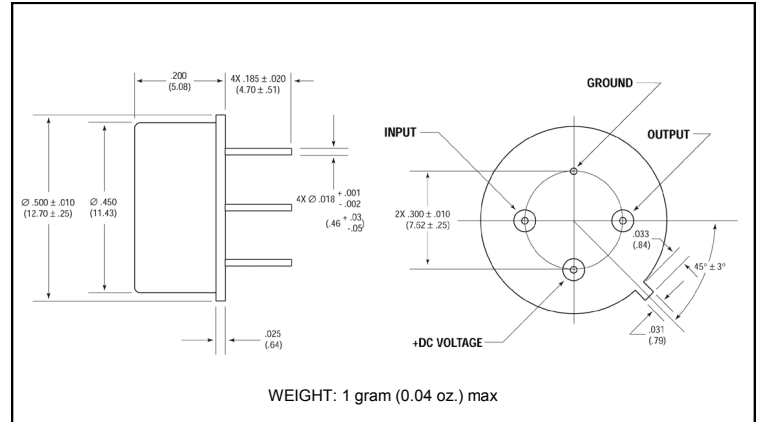
Thermal Data: $V_{CC} = +15 V_{DC}$

Parameter	Rating
Thermal Resistance θ_{jc}	°C/W
Transistor Power Dissipation P_d	W
Junction Temperature Rise Above Case T_{jc}	°C

* Over temperature performance limits for part number CPA512, guaranteed from 0°C to +50°C only.

Rev. V2

Outline Drawing: TO-8 *



Technical drawing of the 0603 package showing top, side, and cross-sectional views with dimensions and tolerances.

Top View:

- Overall width: 450 (11.43)
- Overall height: 450 (11.43)
- Input pad width: 450 (11.43)
- Output pad width: 450 (11.43)
- Product Identification Area (PIA) location: 450 (11.43) from the left edge.
- BIAS pad location: 450 (11.43) from the left edge.
- N/C pad location: 450 (11.43) from the left edge.

Side View:

- Package height: 005 ± 001 (.127 ± .025)
- Lead thickness: .170 (.432)

Cross-sectional View:

- Lead angle: 45°
- Lead thickness: .031 (.787)
- Lead width: .031 (.787)
- Lead height: 4X R .016 ± .002 (.406 ± .051)
- Lead radius: 4X R .018 (.46)
- Lead height: 4X R .061 (1.55)
- Lead height: 4X .060 (1.27)
- Lead height: 2X .200 ± .005 (5.080 ± .127)
- Lead height: 2X .225 ± .005 (5.720 ± .127)
- Lead height: .050 (1.27)
- Lead height: .075 (1.91)
- Lead height: .350 (8.89)
- Lead height: .375 (9.53)

WEIGHT: 1 gram (0.04 oz.) max

The drawing includes the following dimensions and features:

- Top View:**
 - Overall width: $820 \pm .010$ (20.83)
 - Overall height: $1.000 \pm .005$ (25.40)
 - Input connector offset: $2X .460 \pm .010$ (11.68)
 - Input connector spacing: $2X .375 \pm .010$ (9.52)
 - Output connector offset: $2X .810 \pm .010$ (20.57)
 - Output connector spacing: $2X .310 \pm .010$ (7.87)
 - Mounting hole diameter: $4X \varnothing .095 \pm .005$ (2.41)
 - Mounting hole position: $4X \varnothing .086 \pm .005$ UNC-2B
 - Dimensional tolerance: $\pm .15 \pm .10 \pm 2.5$ (3.8 - .0)
- Side View:**
 - PCB thickness: $.180 \pm .005$ (4.57)
 - Input connector height: $.500 \pm .010$ (12.70)
 - Output connector height: $.320 \pm .010$ (8.13)
- Bottom View:**
 - Product Identification Area
 - Input and Output labels
 - Grounding points labeled +VDC and GROUND

* Dimensions are inches (millimeters) ± 0.015 (0.38) unless otherwise specified.

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