HD153014RF/RTF

Data Separator with Buit-in Read Pulse Detector and (1, 7) Encoder/Decoder

The HD153014RF is a data separator with built-in read pulse detector and (1, 7) run-length-limit encoder/decoder developed for use in magnetic disk drives. In read mode it decodes the readback waveform output from the read/write amplifier to an NRZ signal. In write mode it encodes an NRZ signal from the controller to (1, 7) RLL coded data.

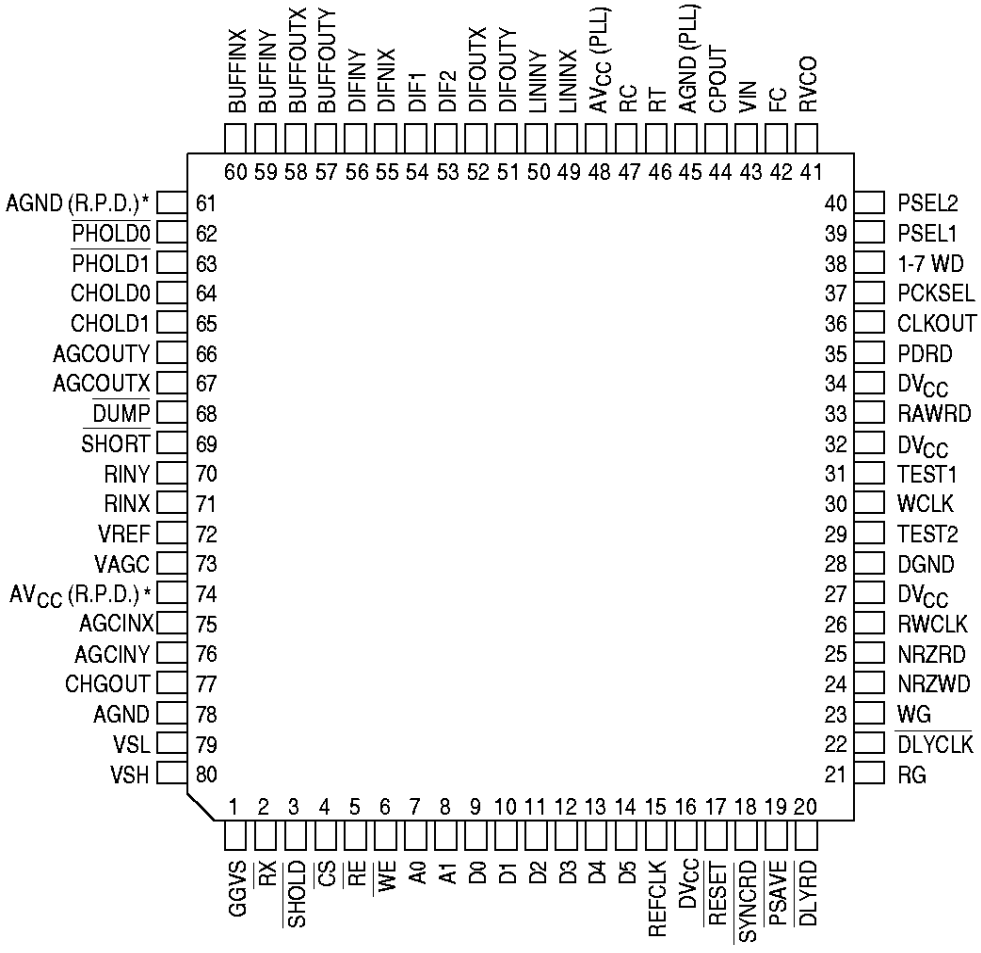
Features

- Data transfer rate: 10 to 24 Mbps.
- Data transfer clock frequency: 1.5 × data transfer rate.
- Built-in AGC amplifier for stable reproduction despite varying media and head characteristics.
- Gate generator enables incorrect read pulse problems that occur with time-domain filtering to be avoided by appropriate level setting. Head resolution can be increased without incorrect read pulse worries.
- AGC amplifier gain can be set to zero during writing.
- Servo signal full wave rectification. Circuitry for two sample and hold channels built in.
- Dual-mode phase detector compares both phase and frequency to ensure a wide capture range.
- High-speed acquisition can be combined with highly stable reproduction by switching between normal-gain and high-gain modes, and by switching loop filter constants.
- VCO oscillation timing capacitor is built in for excellent noise immunity.
- PLL characteristic frequency and damping rate are defined without (1, 7) RLL signal cycle (2T to 8T).
- Encoding and decoding: IBM (1, 7) RLL code.
- Built-in write precompensation with programmable delay.
- Decode window centering adjustment and monitoring functions
- Single 5 V power supply.
- QFP-80 package suitable for compact surface mounting (resin size: 14 mm × 14 mm).
- TTL compatible logic inputs and outputs.
- BiCMOS process achieves high speed with low power dissipation (475 mW).

Ordering Information

Type No.	Package
HD153014RF	80 pin QFP (FP-80A)
HD153014RTF	80 pin Thin QFP (TFP-80)

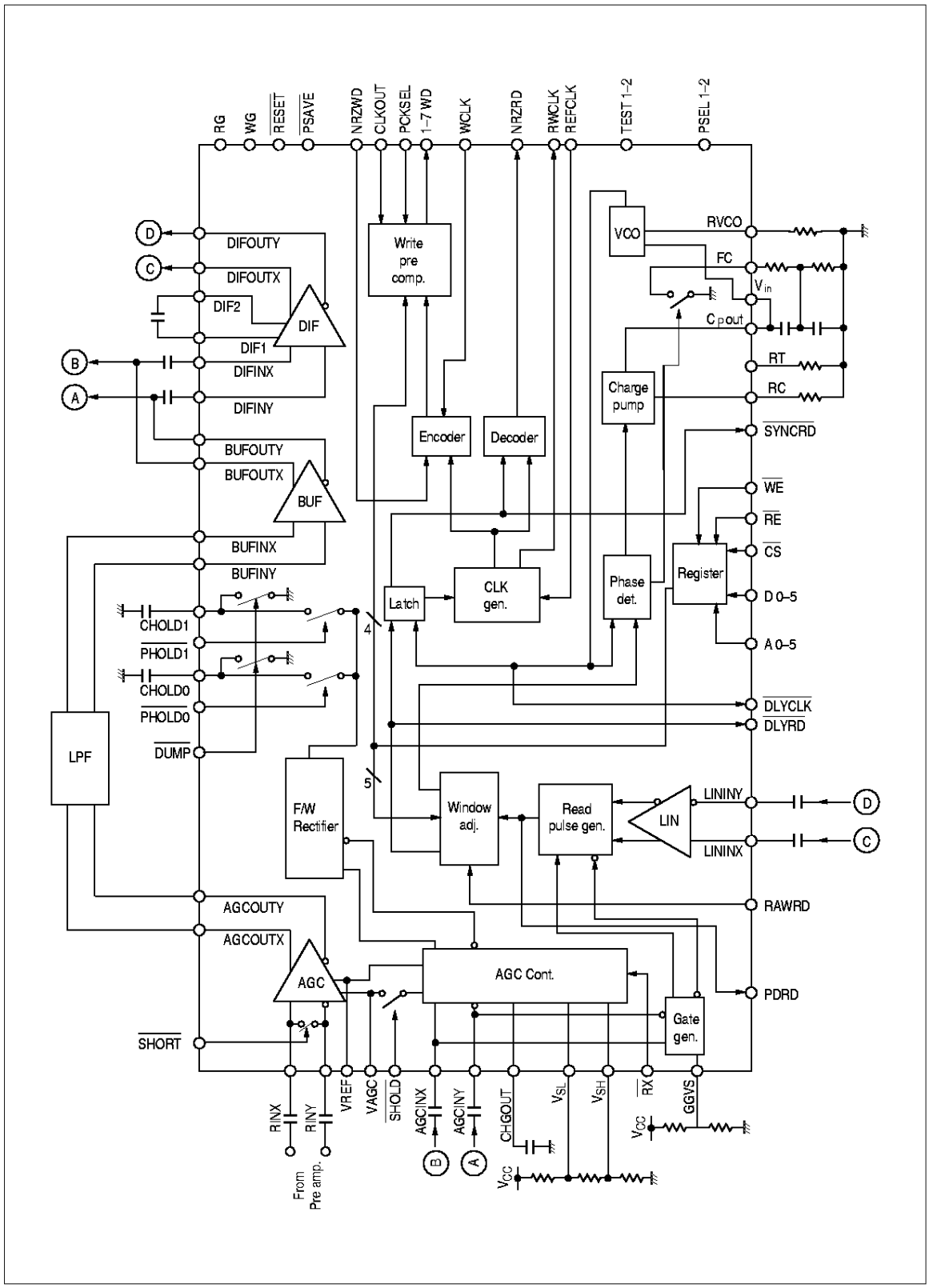
Pin Arrangement



* R.P.D.: Read pulse detector

(Top view)

Block Diagram



Specifications

No.	Item	Specification
1	Data transfer rate	24 Mbps max.
2	Encoding and decoding	(1, 7) RLL code
3	Read pulse detector	On-chip
4	Phase-lock acquisition time	6 Bytes or less
5	Disk format support	Hard sectoring
6	Write precompensation	On-chip (programmable)
7	Decode window centering adjustment	Digital selection: 5 bits, 32 settings, 1.3 ns steps
8	Power dissipation	475 mW during operation
9	Inputs and outputs	TTL compatible
10	Power supply	Single 5 V supply

Pin Functions

Pin name	Pin No.	Type	Function
RAWRD	33	In	Input line for (1, 7) encoded pulses when only the HD153014 RF's VFO and encoder/decoder are used, or for checking data separator operation. The leading edge of the input pulse indicates magnetic reversal. The PLL is phase-synchronized with this leading edge. The polarity of this input can be selected by PSEL2.
WG	23	In	High input selects write mode, in which the NRZ write data signal is converted to (1, 7) code and output.
RG	21	In	High input selects read mode, in which (1, 7) encoded data read from disk are converted to an NRZ signal and output. This signal switches the clock for counters and internal circuits, enables NRZ signal output, and begins phase synchronization of the VFO with the (1, 7) coded data.
CS	4	In	Control input for the HD153014RF's internal registers. HD153014RF registers connected to the microcontroller's bus are selected when this line is driven low.

Pin Functions (cont)

Pin name	Pin No.	Type	Function
WE	6	In	Control input for the HD153014RF's internal registers. Data on the microcontroller's bus are written on the rising edge of WE to the HD153014RF register selected by address input. CS must be low.
RE	5	In	Control input for the HD153014RF's internal registers. While this line is low, contents of the HD153014RF register selected by address input are output on the microcontroller's bus, permitting register contents to be verified. CS must be low.
D0 to D5	9 – 14	In/Out	Data lines for the HD153014RF's internal registers, normally connected to the microcontroller's data bus. Input lines when RE is high. Output lines when RE is low.
A0 to A1	7 – 8	In	Address input lines for the HD153014RF's internal registers, normally connected to the microcontroller's address bus.
PSAVE	19	In	Low input halts operation of logic circuits to reduce power dissipation. The read pulse detector continues to operate, and servo information can be read out. Keep this line high during normal operation.
WCLK	30	In	Apply a clock signal synchronized with the NRZ write data input to NRZWD. Connect this input line to the HD153014RF's RWCLK output line. The input to NRZWD must then be synchronized with the RWCLK output.
NRZWD	24	In	Input line for the NRZ signal to be written to disk. Must be synchronized with the clock signal input to WCLK. The HD153014RF inverts the input on this line, then converts it to (1, 7) code.
RESET	17	In	Low input initializes internal circuits, and locks the built-in VCO to its center frequency. Drive this line low at power-up. Also, the AGC loop is set to the off state. Keep this line high during normal operation.
REFCLK	15	In	Input line for the HD153014RF's reference clock. When not reading data, the VCO is synchronized with this reference clock. Data writing is also clocked by this reference clock. Apply a clock signal with frequency 1.5 times the data transfer rate.
PCKSEL	37	In	Control input line for the CLKOUT line used for external write precompensation. The CLKOUT line is enabled when PCKSEL is driven high. Also, when low, internal precompensation is performed.

Pin Functions (cont)

Pin name	Pin No.	Type	Function
DLYRD	20	Out	Decode window adjustment monitor output. Low output on this line corresponds to 1s in (1, 7) code read from disk. During decode window adjustment, set the falling edge of this pin's output to be in between one falling edge and the next of the DLYCLK output (i.e., in the center of a single cycle). DLYRD output is enabled by low input on the TEST2 test mode selection line. See 1. Test Mode Settings on page 10 for details.
DLYCLK	22	Out	Decode window adjustment monitor output. Provides clock output synchronized with the (1, 7) codes read from disk. The (1, 7) codes can be latched on this clock. During decode window adjustment, set the falling edge of this pin's output to be in between one falling edge and the next of the DLYRD output (i.e., in the center of a single cycle). DLYCLK output is enabled by low input on the TEST2 test mode selection line. See 1. Test Mode Settings on page 10 for details.
SYNCRD	18	Out	Decode window adjustment monitor output. (1, 7) codes read from the disk are latched on the decode clock and output on this line. SYNCRD output is equivalent to capturing the (1, 7) codes output from DLYRD on the DLYCLK output. Use this line to monitor window margin tests. SYNCRD output is enabled by low input on the TEST2 test mode selection line. See 1. Test Mode Settings on page 10 for details.
NRZRD	25	Out	(1, 7) codes read from the disk are converted to an NRZ signal and output on this line. The NRZRD signal is synchronized with the RWCLK signal.
RWCLK	26	Out	In read mode, a clock signal synchronized with the converted NRZ read data is output on this line. At other times, a reference clock is output for input by the disk controller. In read mode, the disk controller should latch the NRZ read data on the RWCLK output. Connect RWCLK to the HD153014RF's WCLK line. The signal input at NRZWD must then be synchronized with the RWCLK output. RWCLK output is free of glitches at clock switchover. The duty cycle of the RWCLK output can be selected by bits 0 to 3 in the HD153014RF's DTC register.
CLKOUT	36	Out	Clock output used in write mode for external write precompensation. The clock signal output on this line is synchronized with the 1, 7WD output. Output on this line is enabled when PCKSEL input is high.
1–7WD	38	Out	Output signal to be written to disk, consisting of (1, 7) codes obtained by encoding the NRZ signal. The polarity of the output on this line can be selected by PSEL1 input. For external write precompensation, output on the CLKOUT line is synchronized with the 1, 7WD output.

Pin Functions (cont)

Pin name	Pin No.	Type	Function
PSEL1	39	In	Input on this line selects the polarity of 1-7WD. **1, 7WD output polarity** / **PSEL1** Active high / High Active low / Low Note: Drive lines 27 and 32 high, or leave them unconnected.
PSEL2	40	In	Input on this line selects the input polarity on RAWRD of (1, 7) codes read from the disk. **RAWRD input polarity** / **PSEL2** Active high / High Active low / Low Note: RAWRD input is active when TEST1 is driven low. Drive lines 27 and 32 high, or leave them unconnected.
TEST1 TEST2	31 29	In	Input lines for selecting decode window centering adjustment mode and other test modes. See "Test Modes and Registers, 1. Test Mode Settings".
PDRD	35	Out	Output line for the data read from disk as reshaped into digital data by the read pulse detector.
RVCO	41	External component connection	Connect a resistor to set the center frequency of the VCO. The resistance value depends on the data transfer rate.
FC	42	External component connection	Used to adapt the loop filter attenuation ζ. Enables independent settings of the attenuation for high gain and normal gain. High gain: The internal transistor connected to this line saturates, grounding this line. Normal gain: The internal transistor connected to this line cuts off, placing this line in the high-impedance state.
VIN	43	External component connection	Voltage input controlling the built-in VCO. The voltage applied to this line varies the VCO's oscillation frequency. Low input on the RESET line causes a VCO bias voltage generated on-chip to be applied to VIN through an analog switch, making the VCO oscillate at its center frequency. Normally this line should be connected to CPOUT.

Pin Functions (cont)

Pin name	Pin No.	Type	Function
CPOUT	44	External component connection	Current output to an external loop filter. Normally this line should be connected to VIN as well as to the loop filter.
RT	46	External component connection	Connect a resistor to set the T/I converter's sampling feedback gain to 1 (nominal). The resistance value depends on the data transfer rate.
RC	47	External component connection	Connect a resistor to set the charge pump output current for high gain. The resistance value determines the gain of the charge pump.
RINX RINY	71 70	Differen-tial input	Differential input lines for the signal read from the recording medium.
BUFFINX BUFFINY	60 59	Differen-tial input	Differential input lines for the low-pass filter (LPF) buffer amplifier.
DIFINX DIFINY	55 56	Differen-tial input	Differential input lines for the differentiating amplifier.
LININX LININY	49 50	Differen-tial input	Differential input lines for the zero-crossing comparator.
AGCINX AGCINY	75 76	Differen-tial input	Differential input lines for the AGC output amplitude detector.
RX	2	In	TTL-level input that switches the AGC loop on or off.
SHOLD	3	In	TTL-level input that locks the AGC amplifier gain. When SHOLD goes low, the gain is locked at its immediately preceding value.
AGCOUTX AGCOUTY	67 66	Differen-tial output	Differential output lines for emitter-follower output from the AGC amplifier.
BUFFOUTX BUFFOUTY	58 57	Differen-tial output	Differential output lines for emitter-follower output from the low-pass filter buffer amplifier.
DIFOUTX DIFOUTY	52 51	Differen-tial output	Differential output lines for emitter-follower output from the differentiating amplifier.
DIF1 DIF2	54 53	External component connection	Connect a resistor and capacitor to set the differential frequency and voltage gain of the differentiating amplifier.

RX input	AGC loop
High	AGC loop on
Low	AGC loop off

Pin Functions (cont)

Pin name	Pin No.	Type	Function
VSL	79	External component connection	Voltage input line for setting the slice voltage of the AGC output amplitude detector. Corresponds to the discharge current threshold.
VSH	80	External component connection	Voltage input line for setting the slice voltage of the AGC output amplitude detector. Corresponds to the charge current threshold.
CHGOUT	77	External component connection	Current output line for the AGC output amplitude detector.
GGVS	1	External component connection	Voltage input line for setting the gate generator's slice level.
VREF	72	Monitor line	Monitor line for the AGC amplifier reference voltage.
VAGC	73	Monitor line	Monitor line for the AGC amplifier gain setting voltage.
PHOLD0 PHOLD1	62 63	IN	Peak voltage sample and hold timimg control pin used during servo information read out. When a TTL low level signal is input to this pin, the full-wave rectified output voltage sampled when this pin was high is held.
CHOLD0 CHOLD1	64 65	External component connection	External capacitors are attached to these pins and used to hold the peak voltage.
DUMP	68	IN	The TTL level input signal pin for initialization of the (hold pin's) peak voltage hold circuit. Initialization is performed when this pin is pulled low.
SHORT	69	IN	Control pin for shorting AGC amp input pin through the analog switch. When this pin is pulled low, the AGC amp input will be shorted.
DV_{CC}	16	Power	Digital V_{CC} power supply.
DGND	28	Power	Digital ground.
AV_{CC} (PLL)	48	Power	Analog V_{CC} power supply. Powers the built-in PLL.
AGND (PLL)	45	Power	Analog ground. Powers the built-in PLL.
AV_{CC} (R.P.D.)	74	Power	Analog V_{CC} power supply. Powers the built-in read pulse detector.

Pin Functions (cont)

Pin name	Pin No.	Type	Function
AGND (R.P.D.)	61	Power	Analog ground. Powers the built-in read pulse detector.
AGND	78	Power	Analog ground.

Absolute Maximum Ratings (Ta = 25°C)

Description	Symbol	Ratings	Unit	Notes
Supply voltage	V_{CC}	7	V	AV_{CC}, DV_{CC}
Input voltage	V_I	–0.3 to 5.5	V	*1
Output voltage	V_O	5.5	V	*2
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	–55 to +125	°C	

Notes: 1. SHOLD, RX, RAWRD, WG, RG, CS, WE, RE, D0, D1 to D5, A0, A1, PSAVE, WCLK, NRZWD, RESET, REFCLK, PCKSEL, PSEL1, PSEL2, TEST1, TEST2, PHOLD0, PHOLD1, DUMP, SHORT
2. DLYRD, DLYCLK, SYNCRD, NRZRD, RWCLK, CLKOUT, 1, 7WD, PDRD

DC Characteristics (Ta = 0 to +70°C) (V_{CC} = 5.0 V ±5% unless otherwise noted)

Item Pin	Symbol	Min	Typ	Max	Unit	Test conditions	
Supply voltage	V_{CC}	4.75	5.0	5.25	V		DV_{CC} AV_{CC}
Input voltage	V_{IH}	2.2	—	5.5	V		* 1
	V_{IL}	–0.3	—	0.8	V		* 1
Input current	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V V_I = 2.7 V	* 1
	I_{IL}	—	—	–400	µA	V_{CC} = 5.25 V V_I = 0.4 V	* 1
Output voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V I_{OH} = –400 µA	* 2
	V_{OL}	—	—	0.5	V	V_{CC} = 4.75 V I_{OL} = 8 mA	* 2
Output short-circuit current 5.25 V	I_{OS} * 2	–20	—	–120	mA		V_{CC} =
Input clamp voltage	V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V	* 1

I_{IN} = –18 mA

DC Characteristics (Ta = 0 to +70°C) (V_{CC} = 5.0 V ±5% unless otherwise noted) (cont)

Item	Symbol	Min	Typ	Max	Unit	Test conditions	Pin
Off-state output current	I_{OZH}	—	—	20	µA	V_{CC} = 5.25 V V_O = 2.7 V	NRZRD
	I_{OZL}	—	—	–20	µA	V_{CC} = 5.25 V V_O = 0.4 V	NRZRD
Current consumption	I_{CC}	—	95	145	mA	V_{CC} = 5.25 V, at 24 Mbps	
DV_{CC}							AV_{CC}
Charge pump output current V, R_C = 470 Ω	I_{CI} CPOUT	—	–1.9	—	mA	V_{CPOUT} = 2.15 V	V_{CC} = 5.0
	I_{CD}	—	1.9	—	mA		
T/I converter output current V, V_{CPOUT} =	I_{TI} CPOUT	—	–20	—	µA	2.15 V, input signal phase offset +π/2 (rad), R_T = 8.2 kΩ, at 24 Mbps	V_{CC} = 5.0
CPOUT	I_{TD}	—	20	—	µA	V_{CC} = 5.0 V, V_{CPOUT} = 2.15 V, input signal phase offset –π/2 (rad), R_T = 8.2 kΩ, at 24 Mbps	
CPOUT	I_{TO}	—	0	—	µA	V_{CC} = 5.0 V, V_{CPOUT} = 2.15 V, input signal phase offset 0 (rad), R_T = 8.2 kΩ, at 24 Mbps	

Notes: 1. SHOLD, RX, RAWRD, WG, RG, CS, WE, RE, D0 to D5, A0, A1, PSAVE, WCLK, NRZWD, RESET, REFCLK, PCKSEL, PSEL1, PSEL2, TEST1, TEST2, PHOLD0, PHOLD1, DUMP, SHORT

2. DLYRD, DLYCLK, SYNCRD, NRZRD, RWCLK, CLKOUT, 1–7WD, PDRD

AC Characteristics (Ta = 25°C, V_{CC} = 5.0 V)

Item	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
Data transfar rate		—	—	24	Mbps		
RESET time	t_{RS}	50	—	—	ns		Figure 1
NRZRD set up time NRZRD	t_{SNR}	15	—	—	ns	With DUTY adjusted, 24 Mbps	Figure 2
		10	—	—	ns	With DUTY not adjusted, 24 Mbps	
NRZRD hold time	t_{HNR}	15	—	—	ns	With DUTY adjusted, 24 Mbps	
		15	—	—	ns	With DUTY not adjusted, 24 Mbps	
Decode time	t_{DD}	—	10	—	VCO CLK	NRZRD	Figure 3
NRZWD set up time	t_{SNW}	10	—	—	ns	NRZWD	Figure 4
NRZWD hold time	t_{HNW}	5	—	—	ns		
Encode time	t_{ED}	—	13	—	REF CLK	No write precompensation 1-7WD	Figure 5
		—	16	—		With write precompensation	
Write precompensation delay time	t_{EN}	—	0	—	ns	Minimun delay time	Figure 6
		—	–9.1	—	ns	Maximum delay time	
	t_{NL}	—	0	—	ns	Minimun delay time	
		—	9.1	—	ns	Maximum delay time	
Register write cycle	t_{WC}	50	—	—	ns	A0 to A1	Figure 7
Address set up time	t_{AS}	5	—	—	ns	WE	
Address hold time	t_{AH}	0	—	—	ns	WE	
Write chip select	t_{CW}	30	—	—	ns	CS	
Write enable time	t_{WW}	20	—	—	ns	WE	
Write data set up time	t_{DS}	10	—	—	ns		D0 to D5

Write data hold time	t_{DH}	5	—	—	ns	D0 to D5

AC Characteristics (Ta = 25°C, V_{CC} = 5.0 V) (cont)

Item	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
Register read cycle	t_{RC}	50	—	—	ns	A0 to A1	Figure 8
Address access time	t_{AA}	—	—	50	ns	D0 to A5	
Output hold time	t_{OH}	5	—	—	ns	D0 to A5	
Read chip select time	t_{CE}	—	—	30	ns	CS	
Read enable time	t_{RE}	—	—	30	ns	RE	
Read disable time	t_{RD}	0	—	30	ns	RE	
Read chip select disable time	t_{CD}	0	—	30	ns	CS	

VFO AC Characteristics (Ta = 25°C, V_{CC} = 5.0 V)

Item	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
VCO center frequency			34.2	36	37.8	MHz	At 24 Mbps
VCO maximum clamp frequency		—	54	—	MHz	At 24 Mbps	
VCO minimum clamp frequency		—	18	—	MHz	At 24 Mbps	
VCO Gain		—	208	—	Mrad/S•V	At 24 Mbps	
Phase pull-in time	taq	—	—	6	Byte	At 24 Mbps, with recommended constants set	
Capture range		±15	—	—	%	At 24 Mbps, with recommended constants set	
Locking range		±15	—	—	%		
Window margin loss		—	—	3.0	ns	During window adjustment	

Note: At 24 Mbps the recommended constants are: R_{VCO} = 2.5 kΩ, R_C = 470 Ω, R_T = 8.2 kΩ
C_1 = 2000 pF, C_2 = 82 pF, R_1 = 910 Ω, R_2 = 330 Ω

R.P.D. DC Characteristics (Ta = 25°C, V_{CC} = 5.0 V)

Item Pin	Symbol Notes		Min	Typ	Max	Unit	Test conditions
Differential input resistance	R_{IA}	2.1	3.0	3.9	kΩ		RINX RINY
Input bias voltage	V_{BA}	2.3	2.5	2.7	V		
Differential output offset voltage	V_{OFA}	—	0	—	mV		AGCOUTX AGCOUTY
In-phase output voltage	V_{OCA}	—	2.4	—	V		
Output sink current	I_{OSA}	—	1.8	—	mA		
Differential input resistance	R_{IB}	8.4	12	15.6	kΩ		BUFFINX BUFFINY
Input bias voltage	V_{BB}	—	3.5	—	V		
Differential output offset voltage	V_{OFB}	—	0	—	mV		BUFFOUTX BUFFOUTY
In-phase output voltage	V_{OCB}	—	3.0	—	V		
Output sink current	I_{OSB}	—	1.9	—	mA		
Differential input resistance	R_{ID}	8.4	12	15.6	kΩ		DIFINX DIFINY
Input bias voltage	V_{BD}	—	3.5	—	V		
DIF sink current	I_{DSD}	—	2.4	—	mA		DIF 1 DIF 2
Differential output offset voltage	V_{OFD}	—	0	—	mV		DIFOUTX DIFOUTY
In-phase output voltage	V_{OCD}	—	3.0	—	V		
Output sink current	I_{OSD}	—	1.9	—	mA		
Differntial input resistance	R_{IC}	8.4	12	15.6	kΩ		AGCINX AGCINY
Input bias voltage	V_{BC}	—	3.5	—	V		
Input bias current	I_{BS}	—	3.0	—	µA		VSL, VSH

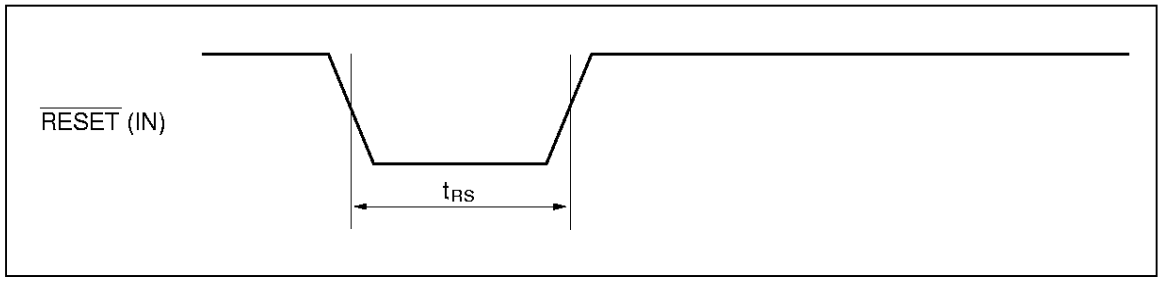


Figure 1 Reset Input

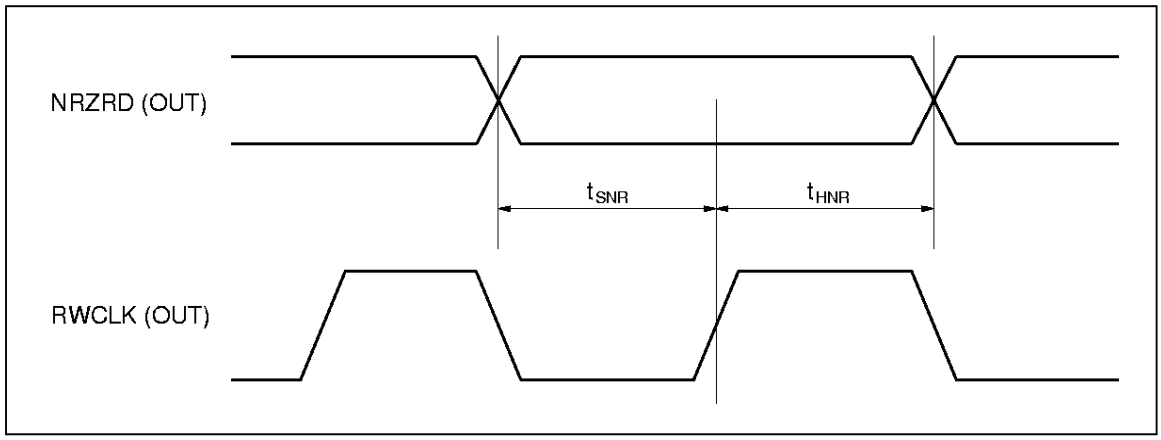


Figure 2 NRZ Read Data Output

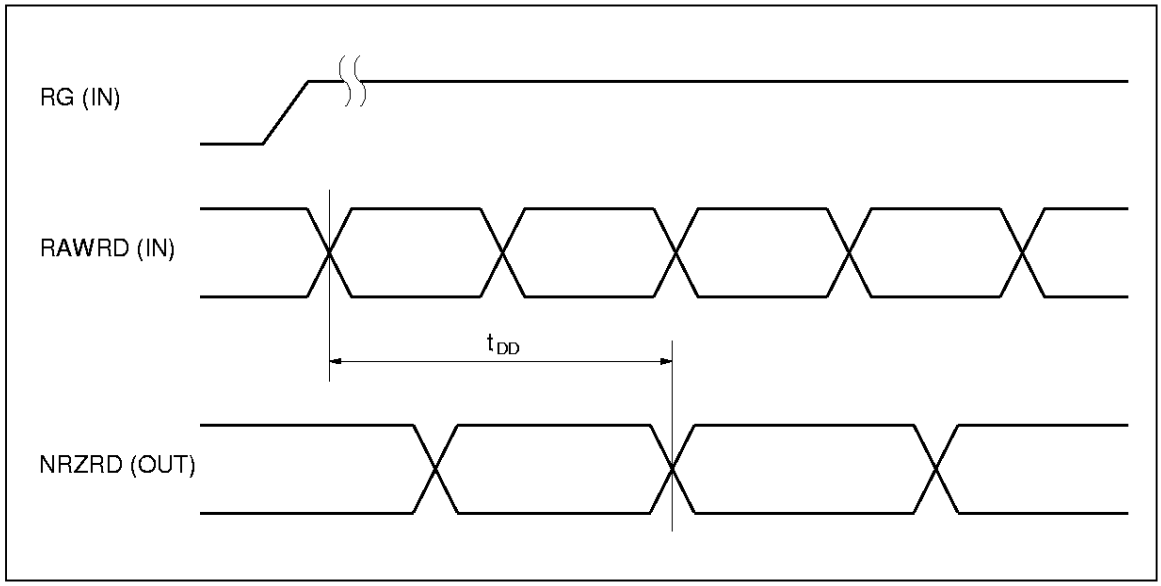


Figure 3 Decode

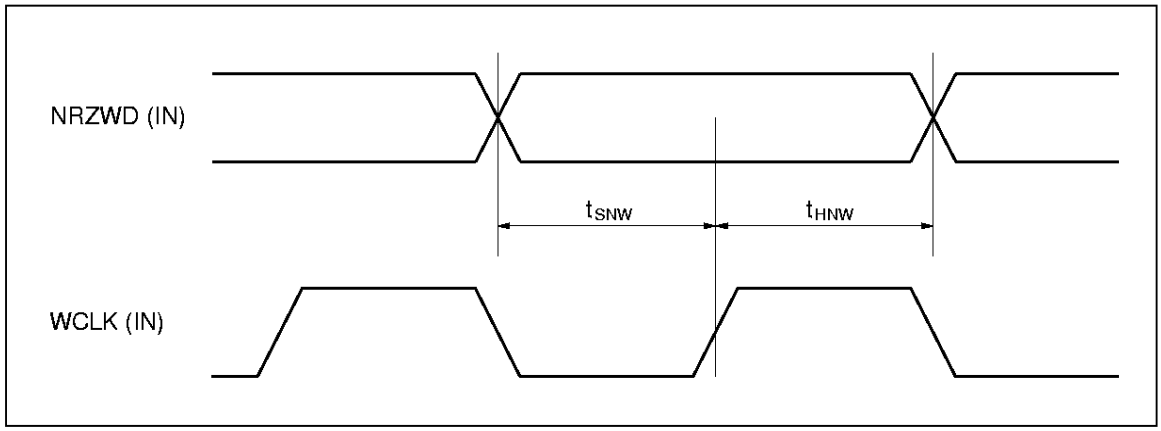


Figure 4 NRZ Write Data Output

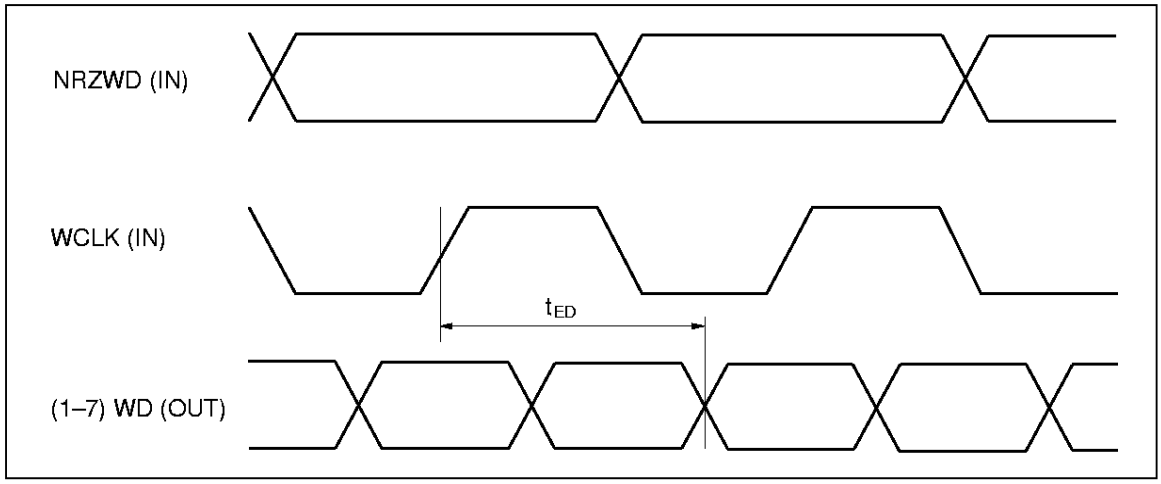


Figure 5 Encode and (1, 7) Code Write Data Output

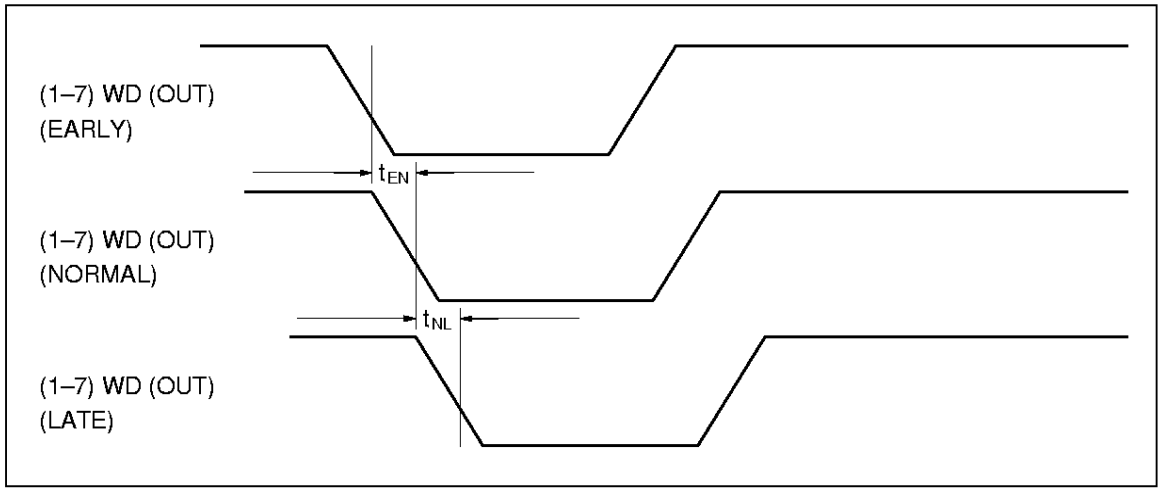


Figure 6 White Precompensation Delay

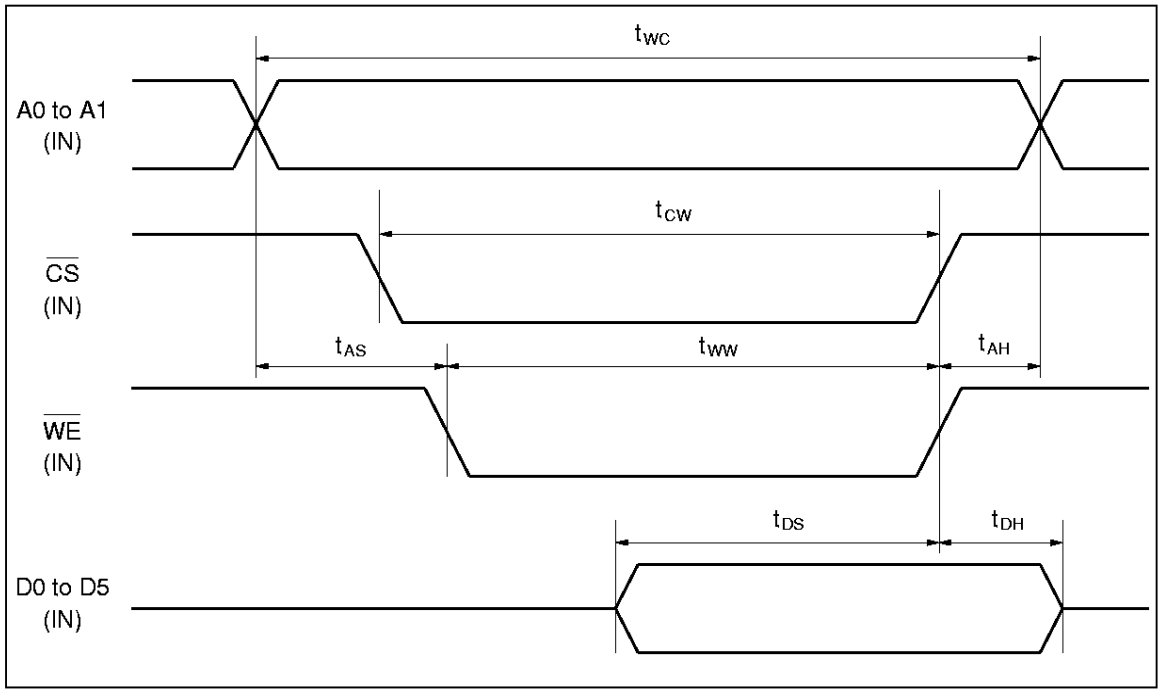


Figure 7 Register Write

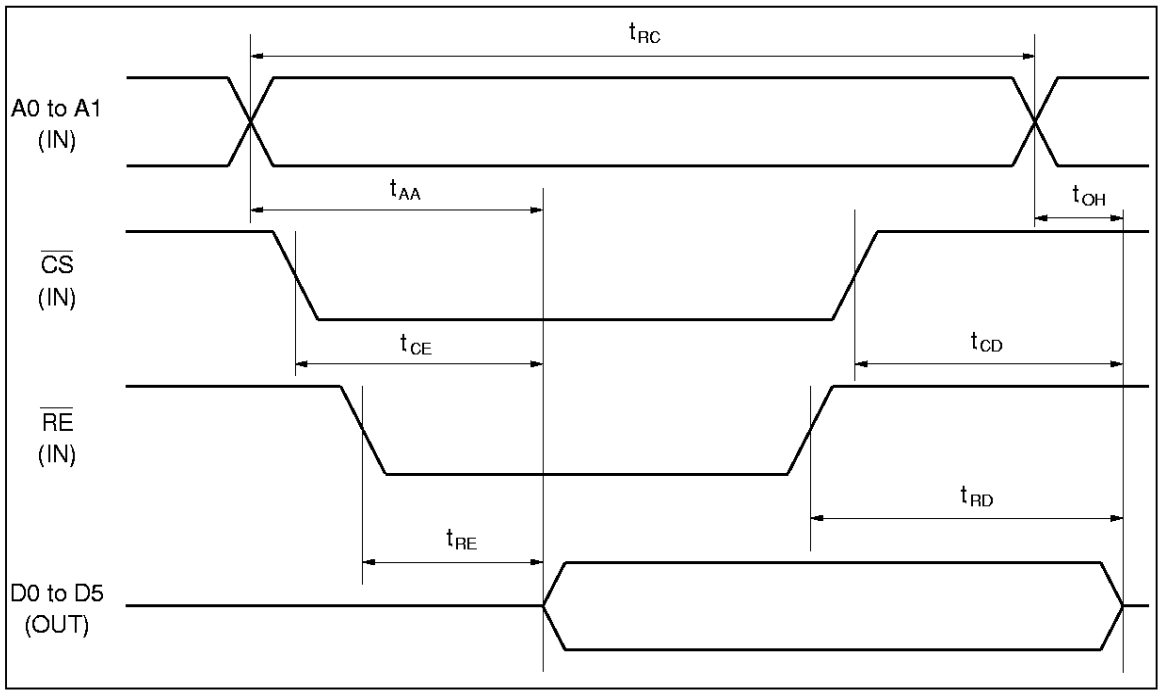


Figure 8 Register Read

Differential voltage gain	A_{VA}	—	40.8	—	dB	f_{IN} = 1 MHz	AGCOUTX AGCOUTY	
Bandwidth MHz	B_{WA}	—	40	—		–3 dB		

						f_{IN} = 1 MHz	DIFOUTY	
Bandwidth MHz	B_{WD}	—	40	—		–3 dB		
PDRD	t_{WPD}	—	—	22.7 ns				

TEST2	TEST1	RAWRD input*1	DLYRD, DLYCLK, and SYNCRD outputs*2	Operating mode
High	High	Don't care	Always high	Normal mode
High	Low	Active (input)	Always high	Test modes
Low	High	Don't care	Output lines	
Low	Low	Active (input)	Output lines	

Notes: *1. When only the HD153014RF VFO and ENDEC functions are used, input the (1, 7) RLL signal from the RAWD input pin.
*2. When monitoring the decode window, set these output pins to the output enabled state.

Common mode rejection ratio	CMRR	—	60	—	dB	f_{IN} = 1 MHz		

PDRD
Output pulse wide

(1) Register Names and Functions

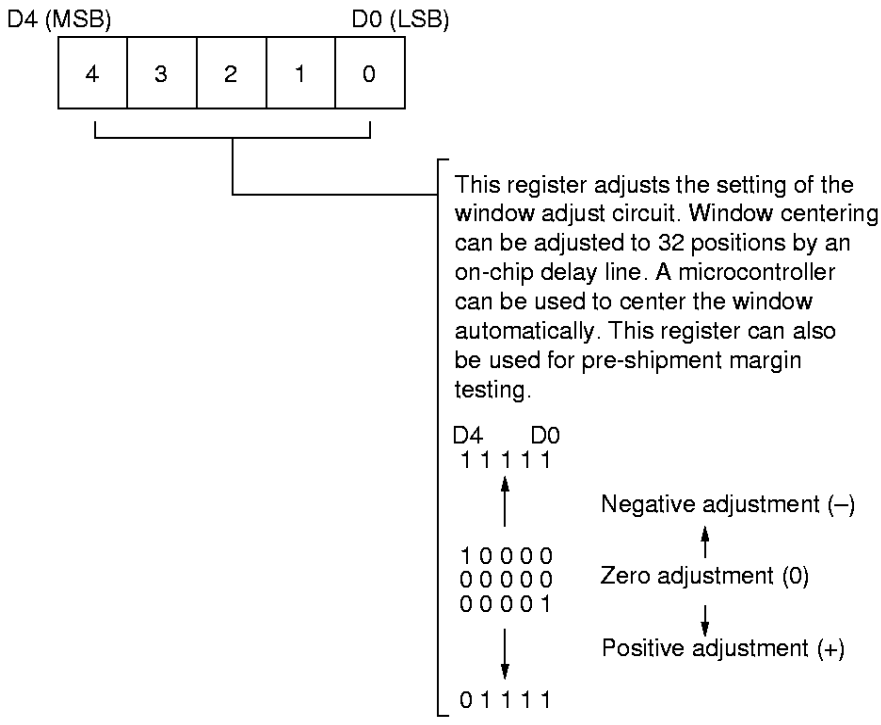
A1	A0	Address	Name	Function
0	0	0	WAJ register	Decode window adjustment
0	1	1	DTC register	RWCLK duty adjustment
1	0	2	WPC register	Write precompensation delay adjustment

Note: The registers are initialized to 0 by a low input on the RESET line at power-up.

Differential voltage gain	A_{VB}	—	6.4	—	dB	f_{IN} = 1 MHz	BUFFOUTX BUFFOUTY	
Bandwidth MHz	B_{WB}	—	40	—		–3 dB		
Differential voltage gain	A_{VD}	—	1.1	—	dB	R_E = 680 Ω	DIFOUTX	

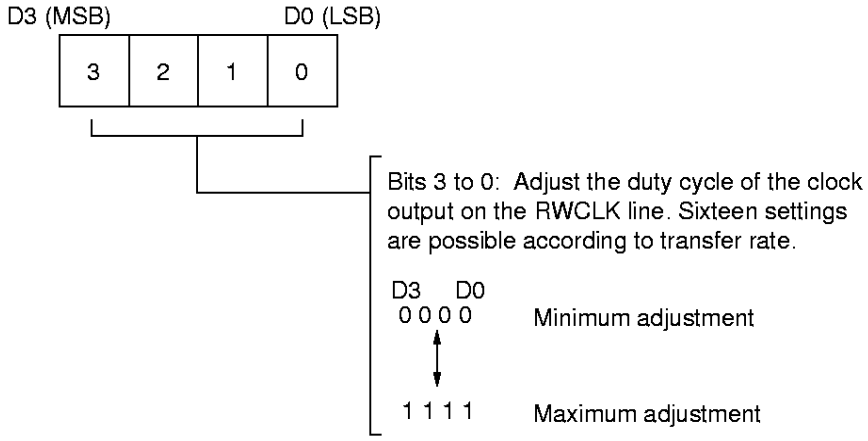
(2) Register Descriptions

Window Adjust Register (WAJ)



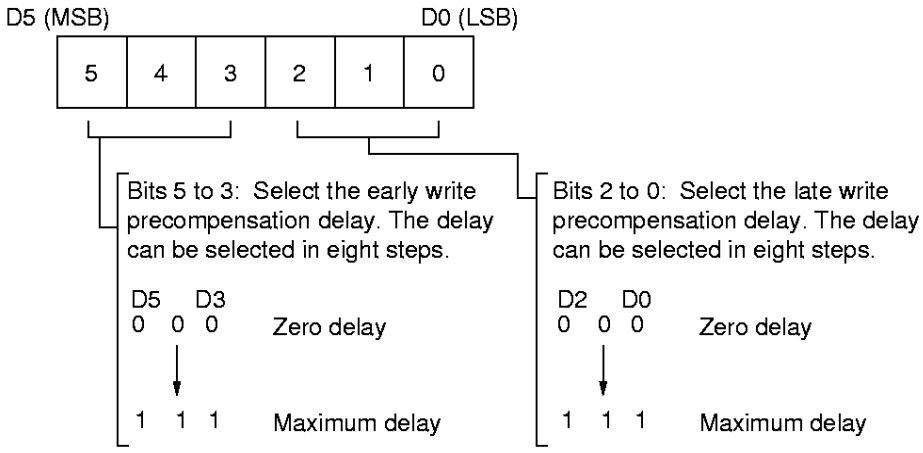
For further details, see "3. Window Adjustment Circuit".

(3) Duty Control Register (DTC)



For further details, see "4. Duty Adjustment Circuit".

(4) Write Precompensation Control Register (WPC)



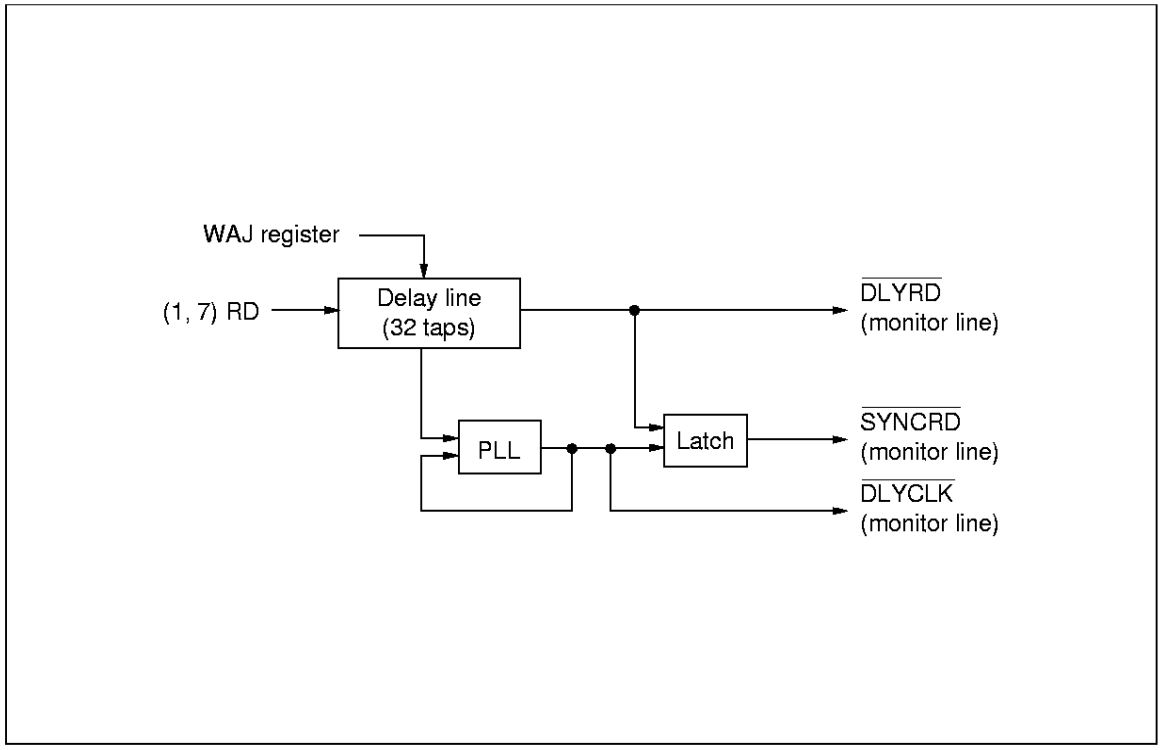
For further details, see "5. Write Precompensation Circuit".

3. Window Adjustment Circuit

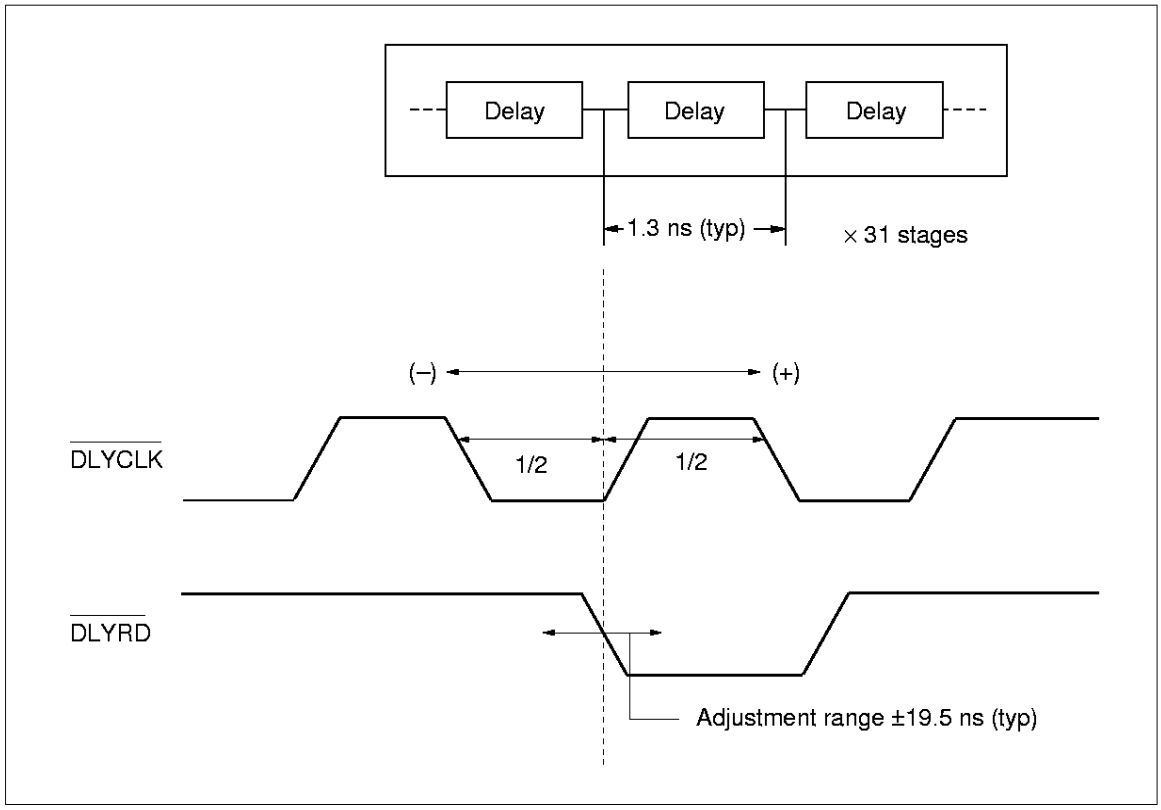
The HD153014RF has an on-chip delay line for centering the decode window. The delay line has 32 taps that can be selected by register WAJ.

Centering adjustment can be performed automatically by a microcontroller. This adjustment function can also be used for pre-shipment margin tests.

(1) Circuit Configuration



(2) Delay Line



WAJ Register

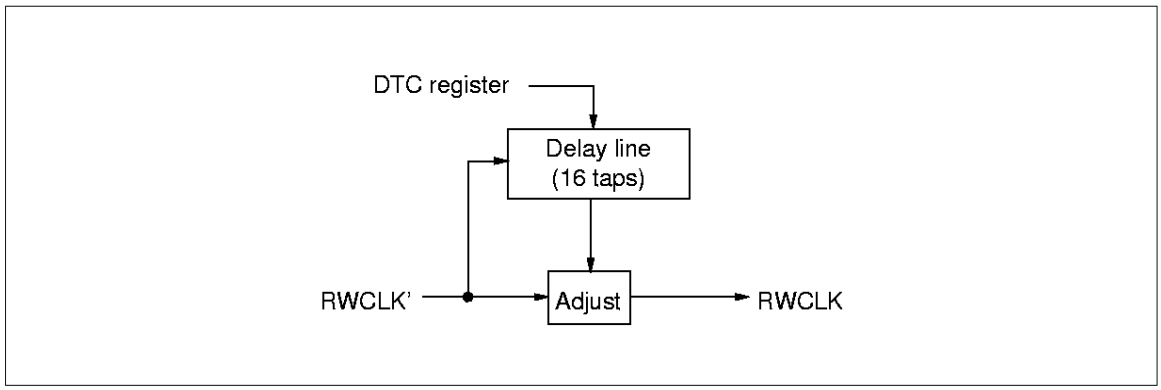
WAJ Register

5	4	3	2	1	0	Delay line tap No.
—	1	1	1	1	1	–16
		⋮				⋮
—	1	0	0	0	1	–2
—	1	0	0	0	0	–1
—	0	0	0	0	0	0
—	0	0	0	0	1	+1
—	0	0	0	1	0	+2
		⋮				⋮
—	0	1	1	1	1	+15

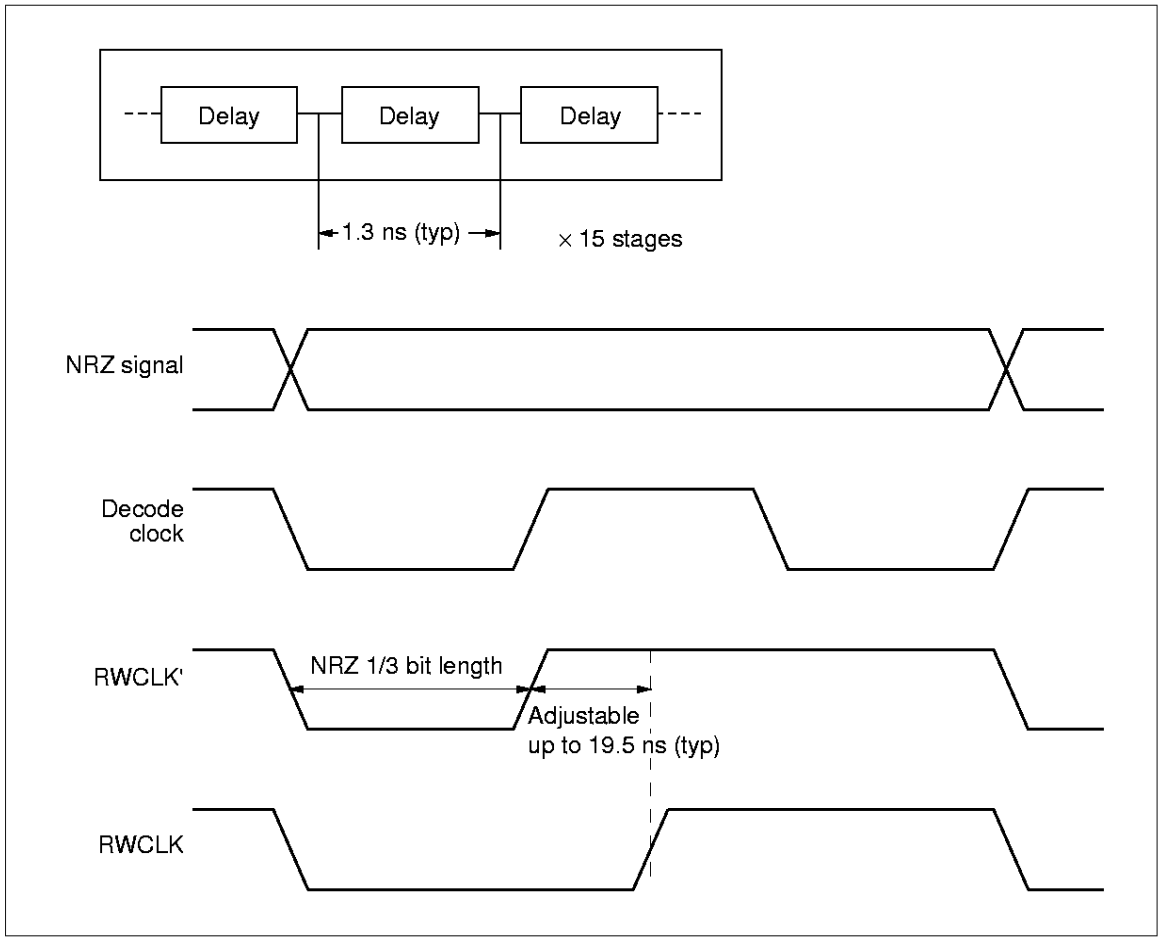
4. Duty Adjustment Circuit

The duty cycle of the clock output to the disk controller on the RWCLK line can be adjusted by setting the DTC register.

(1) Circuit Configuration



(2) Delay Line



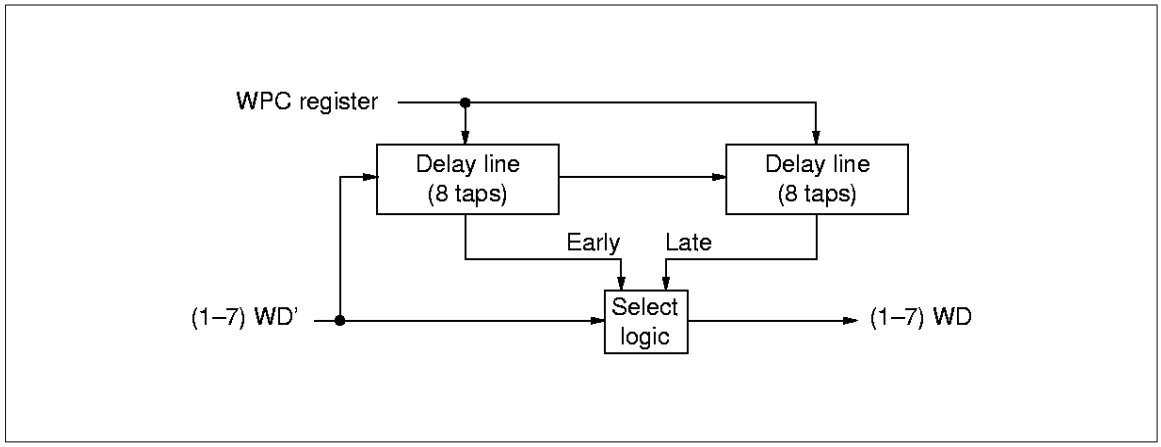
(2) Register Descriptions

Window Adjust Register (WAJ)

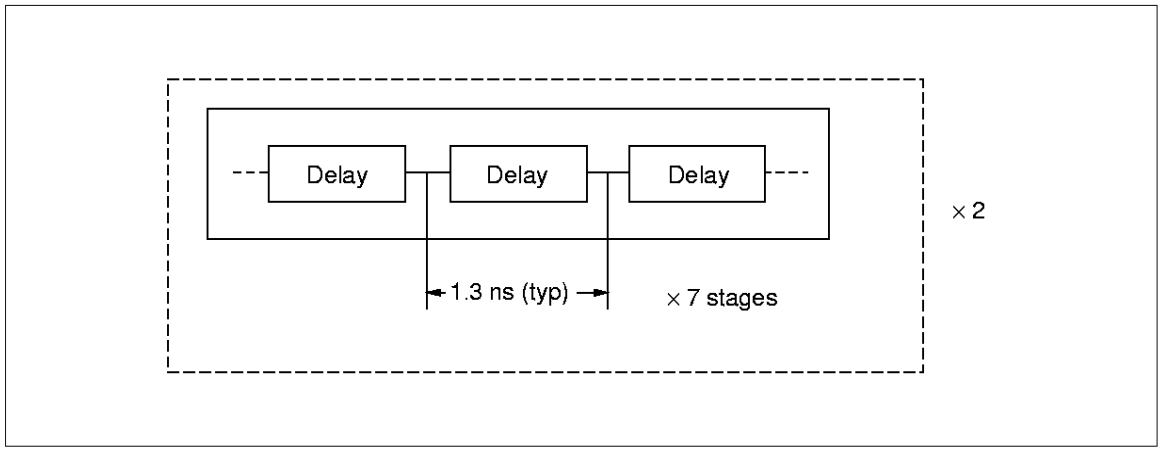
5. Write Precompensation Circuit

The HD153014RF has a built-in write precompensation circuit and a built-in WPC register that can be used to select independent early and late write precompensation delays. Write precompensation can also be performed externally, using a clock signal output on the CLKOUT line in synchronization with the output on the 1–7WD line.

(1) Circuit Configuration



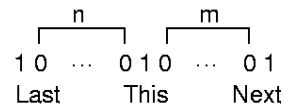
(2) Programmable Delay Line



(3) Table

n \ m	1	2	3	4	5	6	7
1	N	E					
2	L	N					
3							
4							
5							
6							
7							

E: Early
N: Normal (no precompensation)
L: Late
E≤N≤L



n: Number of 0s between this 1 bit and last 1 bit.
m: Number of 0s between this 1 bit and next 1 bit.

The early and late precompensation delays can be selected independently in the WPC register (8 selections for each).

(4) External Write Precompensation Mode

For external write precompensation, drive the PCKSEL line high and use the clock signal output on the CLKOUT line, which is synchronized with the 1, 7WD output .

4. Duty Adjustment Circuit

The duty cycle of the clock output to the disk controller on the RWCLK line can be adjusted by setting the DTC register.

(1) Circuit Configuration

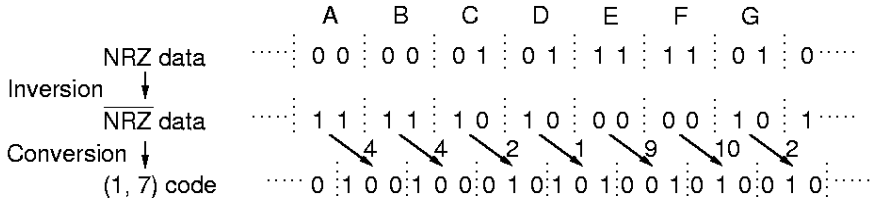
(2) Delay Line

Conversion Table

		NRZ data bits						
No.	Last bit of previous (1, 7) code	Current		Next		(1, 7) Code bits		
1	0	1	0	0	x	1	0	1
2	0	1	0	1	x	0	1	0
3	0	1	1	0	0	0	1	0
4	0	1	1	$\overline{0}$	$\overline{0}$	1	0	0
5	0	0	0	0	x	0	0	1
6	0	0	0	1	x	0	0	0
7	0	0	1	0	x	0	0	1
8	0	0	1	1	x	0	0	0
9	1	0	0	0	x	0	0	1
10	1	0	0	1	x	0	1	0
11	1	0	1	0	0	0	1	0
12	1	0	1	$\overline{0}$	$\overline{0}$	0	0	0

$\overline{0}$ $\overline{0}$: Not 0 0
x: Don't care

An example of the conversion of an NRZ signal to (1, 7) coded data is given below.



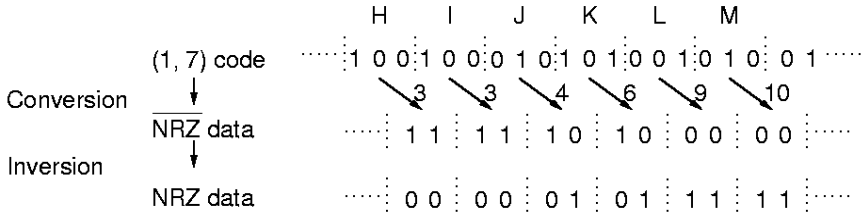
The NRZ data is inverted before it is converted into (1, 7) code. For example, when the above NRZ B data ('00') is converted, it is first inverted to give the NRZ data '11', then the last bit ('0') of the resultof converting A ('100') and the next NRZ data status C '01' (C = '10') dictate that 4 is selected from the conversion table, so that the B data '00' is converted into the (1, 7) code '100'.

Conversion Table ((1, 7) code → NRZ)

	1, 7 code bits			
No.	**Previous**	**Current**	**Next**	**NRZ data bits**
1	X 1 0	0 0 0	X X X	0 0
2	X 0 0	0 0 0	X X X	0 1
3	X X X	1 0 0	X X X	1 1
4	X X 0	0 1 0	0 0 X	1 0
5	X X 0	0 1 0	0 0 X	1 1
6	X X X	1 0 1	X X X	1 0
7	X 0 0	0 0 1	X X X	0 1
8	X 1 0	0 0 1	X X X	0 0
9	X X 1	0 0 1	X X X	0 0
10	X X 1	0 1 0	0 0 X	0 0
11	X X 1	0 1 0	0 0 X	0 1
12	X X 1	0 0 0	X X X	0 1

x: Don't care
0 0: Not 0 0

An example of the conversion of (1, 7) coded data to an NRZ signal is given below.



For example, when the above (1, 7) coded I = '100' data is converted into NRZ data, the previous status H = '100' and the next status J = '010' dictate that 3 is selected from the conversion table, so the data is converted into the NRZ data '11'. This is inverted and output as the NRZ data '00'

HD153014RF PLL Constant Determination Procedure

This section uses 24 Mbps as an example to describe the procedure for determining the HD153014RF PLL constants.

1. Phase Pull-in Time

The HD153014RF high gain period is 6 bytes. Therefore, the phase pull-in time Taq must be set to be less than that.

Example: If the data transfer rate is 24 Mbps, phase pull-in within 5 bytes requires that:

$$Taq = 1/24\ Mbps \times 8\ bits \times 5\ bytes = 1.67\ \mu s \quad (1\text{-}1)$$

2. High Gain ωn (H)

From the formula for computing the PLL phase step response, the phase pull-in completion time is given by the formula 2-1:

$$\omega nT = 5.4 \quad (2\text{-}1)$$

Substituting formula 1-1 gives the high gain ωn(H):

$$\omega n(H) = 3.2\ Mrad/s \quad (2\text{-}2)$$

3. VCO Constants

The VCO center frequency f_{VCO} is:

$$f_{VCO} = \text{transfer rate} \times 1.5 = 24\ Mbps \times 1.5 = 36\ MHz \quad (3\text{-}1)$$

The external resistance R_{VCO} is given by:

$$R_{VCO} = K1/f_{VCO}\ (Hz) \qquad (K1 = 9.0 \times 10^{10}) \quad (3\text{-}2)$$

Therefore at 24 Mbps:

$$R_{VCO} = 2.5\ k\Omega \quad (3\text{-}3)$$

Also, at this time the VCO gain K0 will be:

$$K0 = K2/\sqrt{R_{VCO}} \qquad (K2 = 1.04 \times 10^{10}) \quad (3\text{-}4)$$

Therefore at 24 Mbps:

$$K0 = 208\ Mrad/S \cdot V \quad (3\text{-}5)$$

4. T/I Conversion Circuit Constants

Next, we derive the T/I conversion circuit external resistance R_T and the phase detector gain Kd(N) (normal gain).

$$R_T = K3/f_{VCO} \qquad (K3 = 3.0 \times 10^{10}) \quad (4\text{-}1)$$

Therefore, at 24 Mbps:

$$R_T = 8.33\ k\Omega \rightarrow 8.2\ k\Omega \quad (4\text{-}2)$$

Also, Kd(N) is given by:

$$Kd(N) = K4/\pi \cdot R_T \qquad (K4 = 0.28) \quad (4\text{-}3)$$

Therefore, at 24 Mbps:

$$Kd(N) \fallingdotseq 34/\pi\ \mu A/rad \quad (4\text{-}4)$$

5. Charge Pump Circuit Constants

Next, we derive the external resistance R_C which determines the charge pump circuit's output current and the phase detector gain Kd(H) (high gain).
R_C should be in the range $250\ \Omega \leq R_C \leq 1\ k\Omega$. We recommend initially setting R_C to:

$$R_C = 470\ \Omega \quad (5\text{-}1)$$

Next we derive the phase detector gain Kd(H) (high gain).

$$Kd\ (H) = \frac{0.9}{6\pi \cdot Rc} \quad (5\text{-}2)$$

Therefore, when $R_C = 470\ \Omega$,

$$Kd(H) = 319/\pi \cdot \mu A/rad \quad (5\text{-}3)$$

6. Loop Filter Constants [1]

First we derive the loop filter C1 capacitance:

$$C1 = \frac{K0 \cdot Kd\ (H)}{\omega n^2\ (H)} \quad (6\text{-}1)$$

Substituting the values from formulas (2-2), (3-5), and (5-3) gives:

$$C1 = 2062\ pF \rightarrow 2000\ pF \quad (6\text{-}2)$$

7. Normal Gain ωn(N)

$$\omega n\ (N) = \sqrt{\frac{K0 \cdot Kd\ (N)}{C1}} \quad (7\text{-}1)$$

Substituting the values from formulas (3-5), (4-4), and (6-2) gives:

$$\omega n(N) = 1.06\ Mrad/s \quad (7\text{-}2)$$

8. Loop Filter Constants [2]

We derive the values for the external resistances R1 and R2, setting the high gain attenuation factor $\zeta(H) = 0.8$, and the low gain attenuation factor $\zeta(L) = 1.0$.

$$R1 = \frac{2\ \zeta \cdot (N)}{C1 \cdot \omega n(N)} \quad (8\text{-}1)$$

Substituting the values from formulas (6-2) and (7-2) gives:

$$R1 = 943\ \Omega \rightarrow 910\ \Omega \tag{8-2}$$

Also, R2 is given by:

$$R1 = \left(\frac{C1 \cdot \omega n(H)}{2 \cdot \zeta(H)} - \frac{1}{P1}\right)^{-1} \tag{8-3}$$

Substituting the values from formulas (6-2), (2-2), and (8-2) gives:

$$R2 = 344\ \Omega \rightarrow 330\ \Omega \tag{8-4}$$

9. Loop Filter Constants (3)

Next we construct the Bode diagram and derive the loop filter C2 capacitance.
The system open loop transfer function G(S) is given by:

$$G(S) = \frac{K0 \cdot Kd}{C1} \cdot \frac{1}{S^2} \cdot \frac{1 + S \cdot (C1 + C2) \cdot R}{1 + S \cdot C2 \cdot R} \tag{9-1}$$

Therefore, the Bode diagram can be constructed by the following procedure.

a. Draw a straight line of –40 dB/dec through (ωn, 0).

b. Proceed at –20 dB/dec from $\omega = \frac{1}{(C1 + C2) \cdot R}$

Here, temporarily substitute a value of about 1/20 C1 for C2.

c. Read off the unity gain frequency ω0(N) and ω0(H) from the graph.

Next, we derive the loop filter C2 capacitance. C2 performs the function of reducing the system gain in the high frequency region. The break frequency ω2 which is delayed by –40 dB/dec is expressed by:

$$\omega 2 = \frac{1}{C2 \cdot R} \tag{9-2}$$

When ω2 is large, it is easy to follow high frequency components such as jitter, and when it is small the system phase margin is reduced, and furthermore, the second order approximation error is increased. Therefore, set C2 near the value in the formula below as a first approximation.

$$C2 = \frac{0.65}{C1 + R1^2 \cdot \omega 0(N)^2} \tag{9-3}$$

ω0(N): Unity gain frequency at normal gain.

Example: When ω0(N) is 2.15 Mrad/s:

$$C2 = \frac{0.65}{2000\text{pF} \times 910^2 \times (2.15 \times 10^6)^2} = 84.9\ \text{pF} \rightarrow 82\ \text{pF} \tag{9-4}$$

Next, we continue with the construction of the Bode diagram.

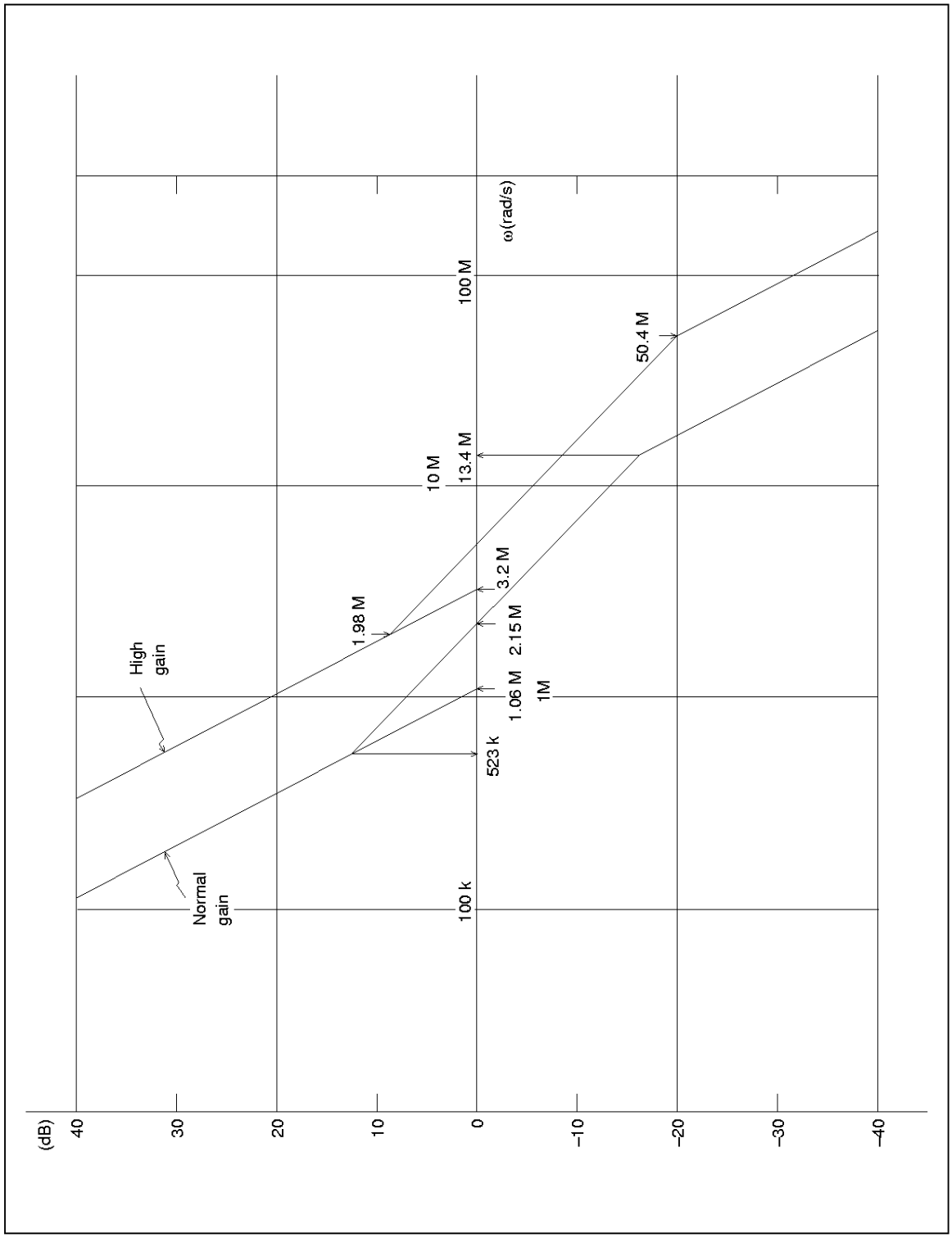
d. With $\omega = \frac{1}{C2 \cdot R}$, it is delayed by – 40 dB/dec. (9-5)

This means that the formulas in b, (9-2), and d above which include R have different values at high gain and normal gain settings.

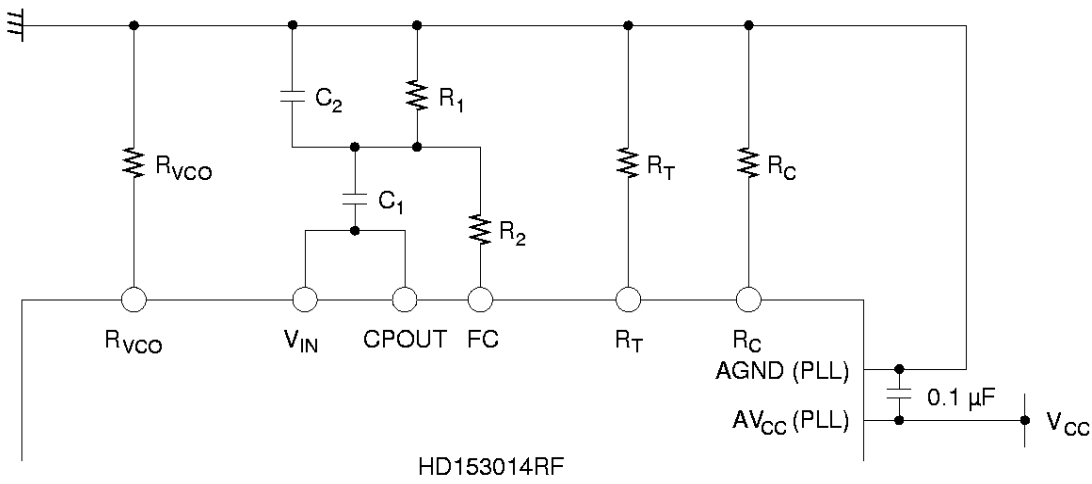
$$R = \begin{cases} R1 & : \text{Normal Gain} \\ R1 \,//\, R2 & : \text{High Gain} \rightarrow \left(\frac{1}{R1} + \frac{1}{R2}\right)^{-1} \end{cases}$$

The Bode diagram derived by the above procedure is shown below.

HD153014RF Bode Diagram for 24 Mbps



External Circuit Example

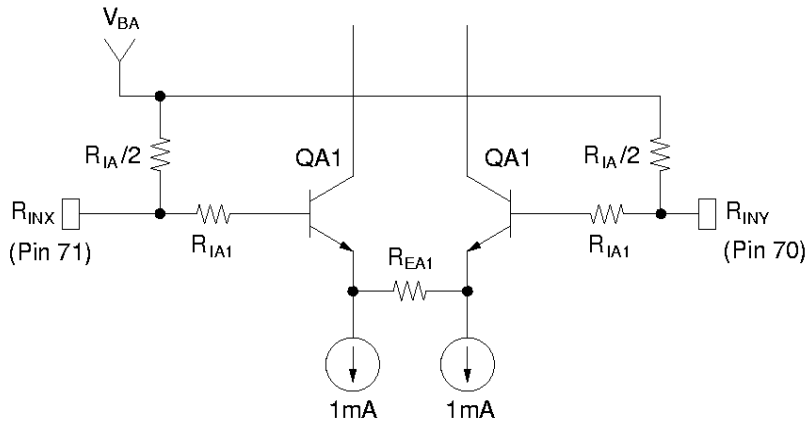


Transfer rate	R_C	R_T	R_{VCO}	C_1	C_2	R_1	R_2
24 Mbps	470 Ω	8.2 kΩ	2.5 kΩ	2000 pF	82 pF	910 Ω	330 Ω
20 Mbps	470 Ω	10 kΩ	3 kΩ	2700 pF	120 pF	910 Ω	270 Ω
15 Mbps	470 Ω	13 kΩ	4 kΩ	4300 pF	160 pF	910 Ω	240 Ω
12 Mbps	470 Ω	16 kΩ	5 kΩ	5600 pF	240 pF	910 Ω	220 Ω
10 Mbps	470 Ω	20 kΩ	6 kΩ	7500 pF	330 pF	910 Ω	200 Ω

HD153014RF R.P.D. Amplifier Input Output Impedance

1. AGC Amplifier

a. Input resistance (Applicable pins: RINX (pin 71), RINY (pin70))



$R_{IN\ (AGC)} = R_{IA}/2\ //\ \{ R_{IA1} + h_{FEQA1} \times (R_{EQA1} + R_{EA1}/2)\}$

$= 1.5\ k\Omega\ //\ 12.03\ k\Omega$

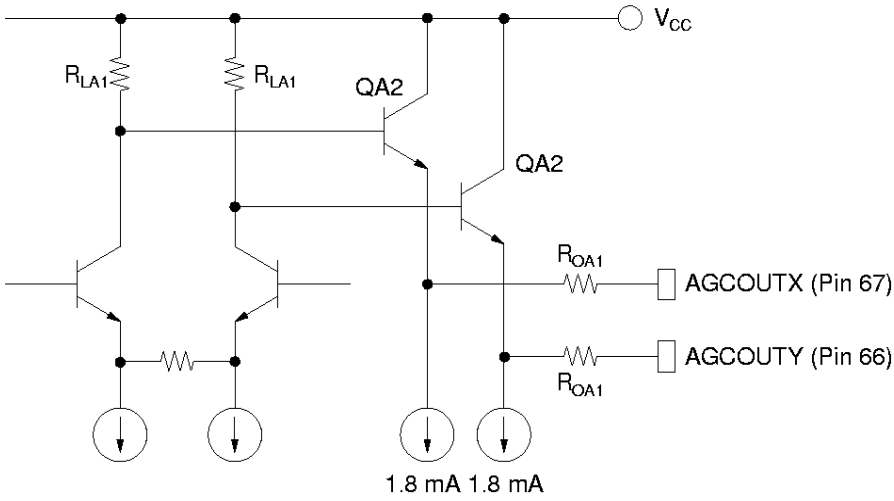
$= 1.33\ k\Omega$

h_{FEQA1} ; Transistor QA1's current amplification ratio

R_{EA1} ; Transistor QA1's emitter resistance

$R_{IA}/2$	1.5 kΩ
R_{IA1}	75 Ω
R_{EQA1}	25.7 Ω
R_{EA1}	187.5 kΩ
h_{FEQA1}	100

b. Output resistance (Applicable pins: AGCOUTX (pin 67), AGCOUTY (pin 66))



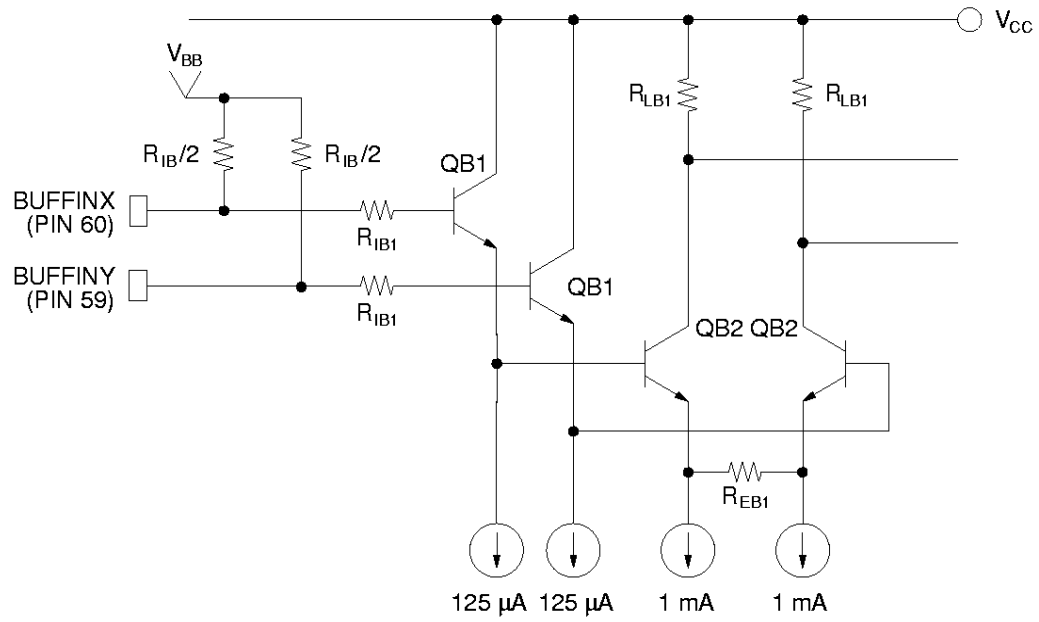
$R_{OUT\ (AGC)} = R_{OA1} + R_{EQA2} + R_{LA1}/h_{FEQA2}$

$\cong 59\ \Omega$

R_{OA1}	20 Ω
R_{EQA2}	14.3 Ω
R_{LA1}	2.5 kΩ
h_{FEQA2}	100

2. Buffer Amplifier

a. Input resistance (Applicable pins: BUFFINX (pin 60), BUFFINY (pin 59))

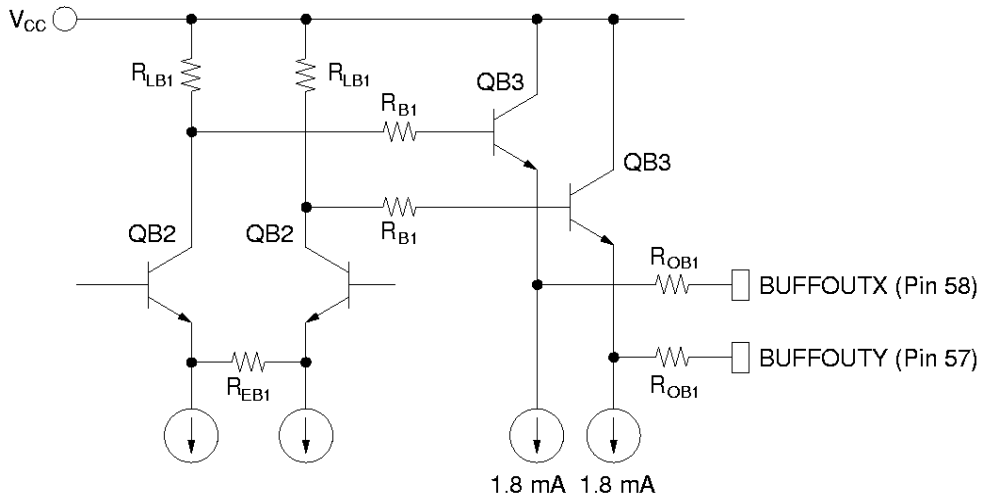


$R_{IN\ (BUFF)} = R_{IB}/2\ //\ \{R_{IB1} + h_{FEQB1} \times h_{FEQB2} \times (R_{EQB2} + R_{EB1}/2)\}$

$\cong 6\ k\Omega$

$R_{IB}/2$	6 kΩ
R_{IB1}	200 Ω
h_{FEQB1}	100
h_{FEQB2}	100
R_{EQB2}	25.7 Ω
R_{EB1}	1.1 kΩ

b. Output resistance (Applicable pins: BUFFOUTX (pin 58), BUFFOUTY (pin 57))



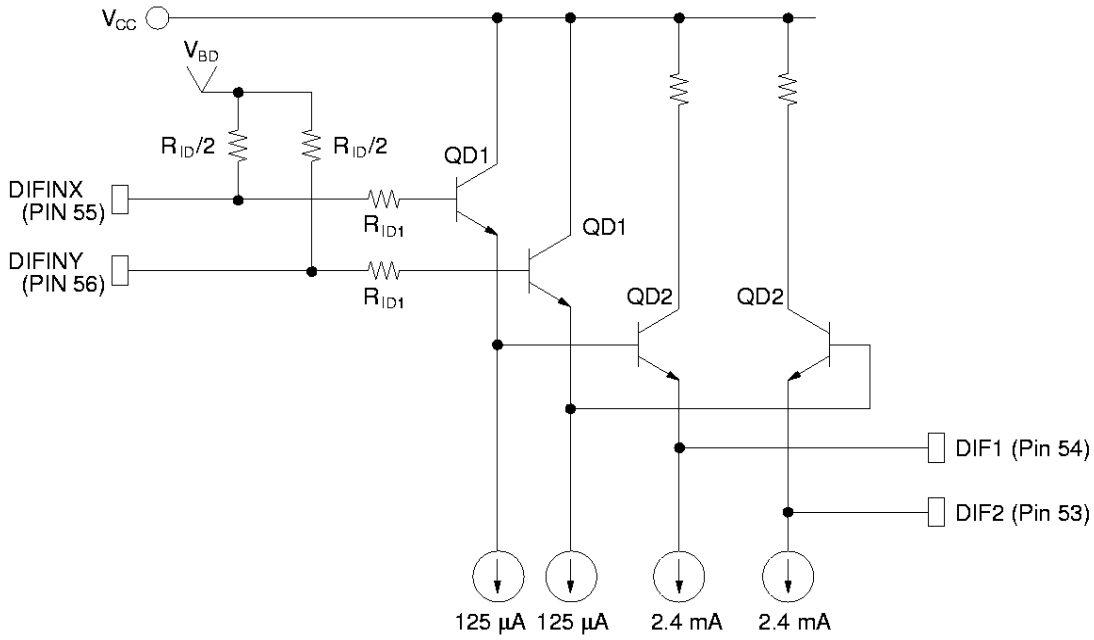
$R_{OUT\ (BUFF)} = R_{OB1} + R_{EQB3} + (R_{B1} + R_{LB1}) / h_{FEQB3}$

$\cong 102\ \Omega$

R_{OB1}	75 Ω
R_{EQB3}	14.3 Ω
R_{B1}	100 Ω
R_{LB1}	1.2 kΩ
h_{FEQB3}	100

3. Differential Amplifier

a. Input resistance (Applicable pins: DIFINX (pin 55), DIFINY (pin 56))



$$R_{IN\ (DIF)} \cong R_{ID}/2\ //\ \{\ R_{ID1} + h_{FEQD1} \times h_{FEQD2} \times (R_{EQD2} + R_{EX}/2)\ \}$$

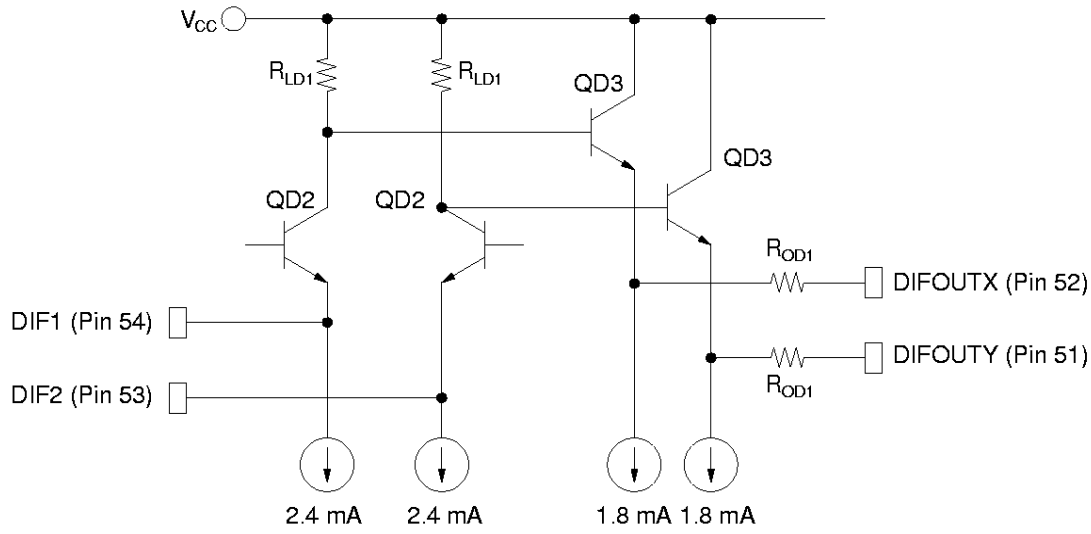
$$\cong 6\ k\Omega\ //\ \{\ 107.28\ \Omega + 5000 \times\ R_{EX}\ \}$$

$$\cong 6\ k\Omega$$

R_{EX}: External resistance between DIF1 and DIF2.

$R_{ID}/2$	6 kΩ
R_{ID1}	200 Ω
h_{FEQD1}	100
h_{FEQD2}	100
R_{EQD2}	10.7 Ω

b. Output resistance (Applicable pins: DIFOUTX (pin 52), DIFOUTY (pin 51))



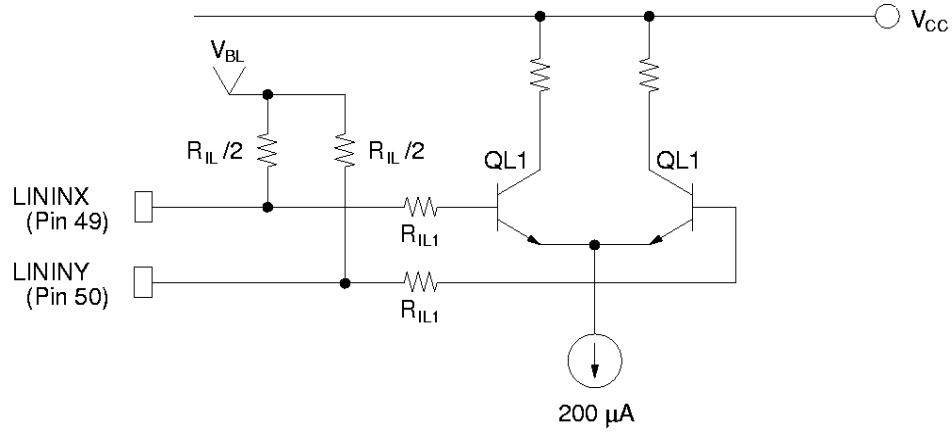
$R_{OUT\ (DIF)} \cong R_{OD1} + R_{EQD3} + R_{LD1} / h_{FEQD3}$

$\cong 93.3\ \Omega$

R_{OD1}	75 Ω
R_{EQD3}	14.3 Ω
R_{LD1}	400 Ω
h_{FEQD3}	100

4. Line Amplifier

a. Input resistance (Applicable pins: LININX (pin 49, LININY (pin 50))

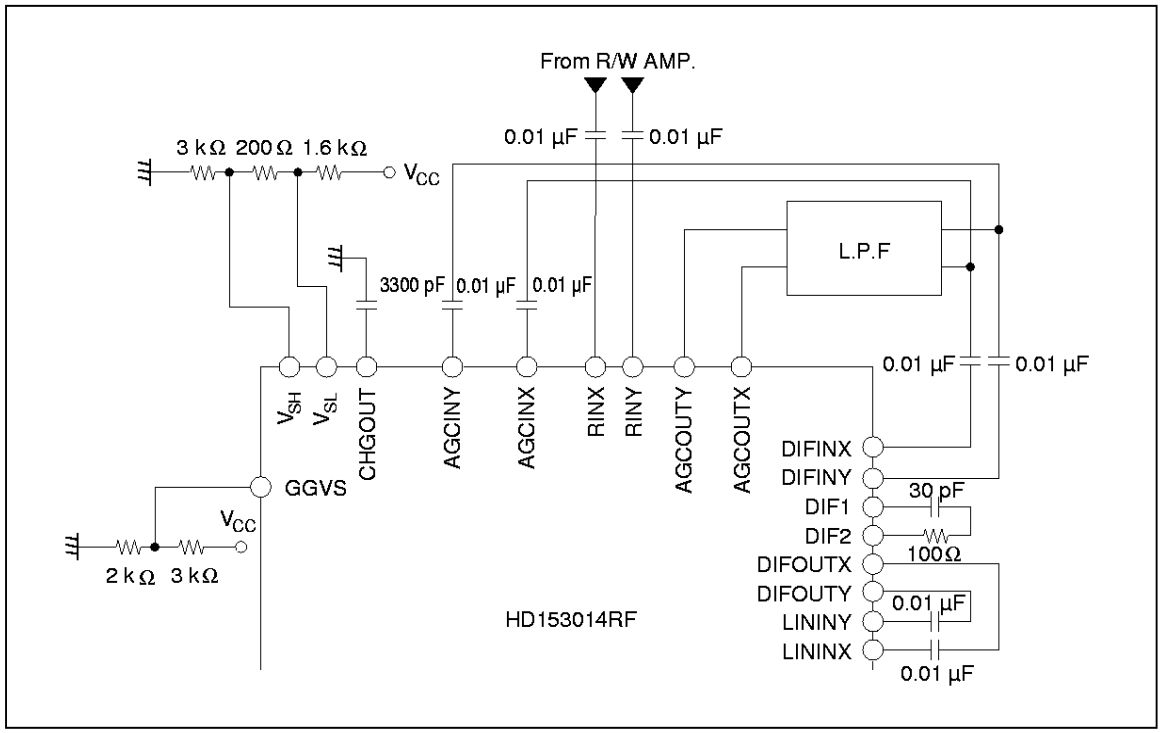


$R_{IN\ (LIN)} \cong R_{IL}/2\ //\ \{ R_{IL1} + (h_{FEQL1} \times R_{EQL1}) \}$

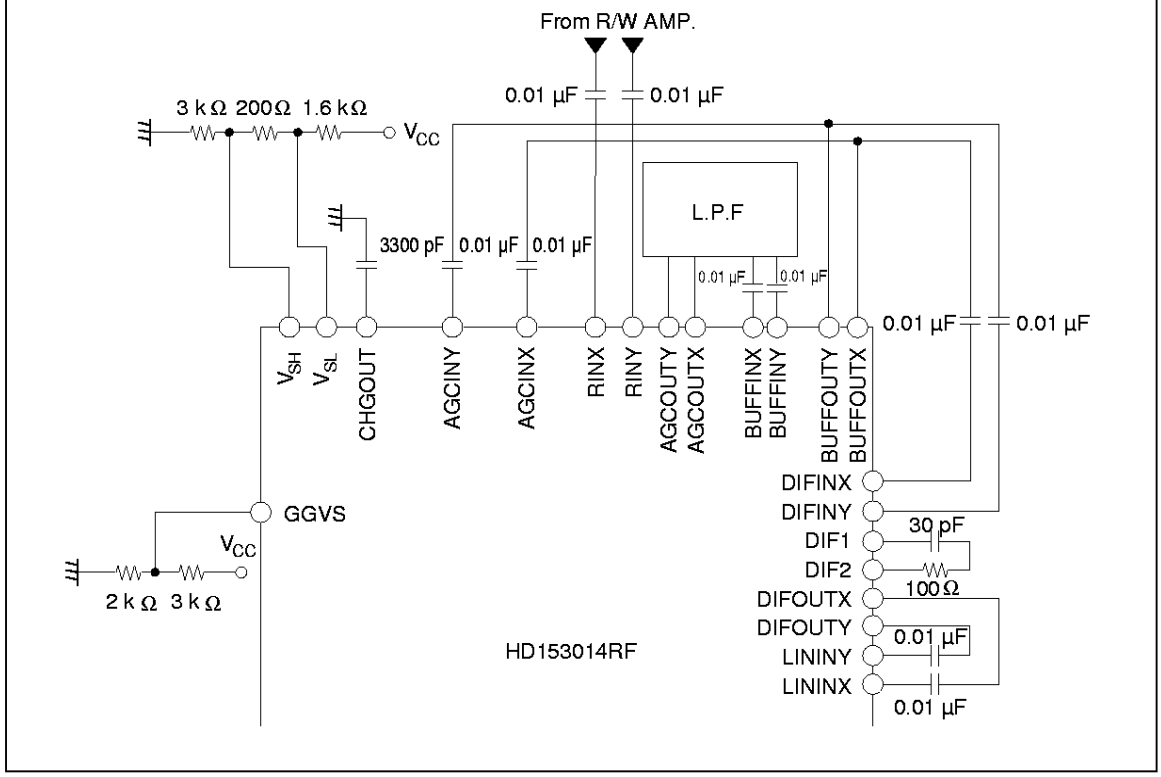
$\cong 3.83\ k\Omega$

$R_{IL}/2$	4.5 kΩ
R_{IL1}	100 Ω
h_{FEQL1}	100
R_{EQL1}	257 Ω

b. External R.P.D. Circuit Example 1 (At 24 Mbps)



c. External R.P.D. Circuit Example 2 (At 24 Mbps)



5. AGC (Automatic Gain Control) Amplifier Circuit

The HD153014RF AGC amplifier is constructed from two differential amplifier stages, with the first stage gain variable, and the second stage gain fixed. The AGC amplifier gain is determined by the difference between V_{REF} and the AGC control circuit output V_{AGC}. Figure 5-1 shows the structure of the AGC amplifier.

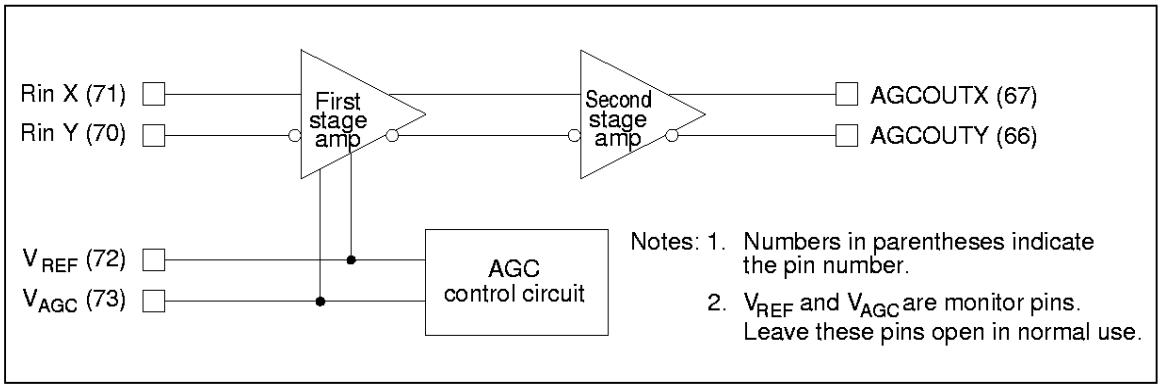


Figure 5-1 The AGC Amplifier Structure

(1) The AGC Amplifier Gain

The AGC amplifier gain is determined by the difference between V_{REF} and the AGC control circuit output V_{AGC}, and is expressed by the equations (5-1) below.

$$A_{V\,(V/V)} = K_1 \times \left(\frac{1}{1 + \exp\,(qV_C/kT)}\right) \qquad (5\text{-}1)$$

K_1 = 110 V/V (= 40.8 dB)
:AGC Full Gain
$V_C = V_{AGC} - V_{REF}$
q: elementary
k: Boltzman's constant
T: absolute temperature (KT/q ≈ 26 mV)

6. Differential Amplifier Circuit

The current flowing in the collector due to the external capacitance C_{EX} connected between pins Dif.1 and 2, can be expressed by the following formula.

$$ic\,(t) = C_{EX} \times \frac{dVin}{dt}$$

Taking the differentiation circuit input voltage Vin(t) to be $Vp \times \sin \omega t$ gives:

$$ic\,(t) = C_{EX} \times Vp \times \omega \times \cos \omega t$$

Here, the value of the external capacitor C_{EX} should be chosen so that the ic(t) current slew rate is as large as possible, so the waveform will not be distorted. Here, the maximum value of ic(t) (i.e., ic (t) max) can be expressed by the following formula.

$$ic\ max = C_{EX} \times Vp \times \omega$$

Set ic max to be less than the fixed current I_{DSD} (2.4 mA (typ): the dif. sink current). If ic max is grater than I_{DSD}, waveform distortion will occur.
Therefore, it is necessary for C_{EX} to fulfill the following condition.

$$C_{EX} < I_{DSD}/Vp \times \omega$$

The frequency characteristics of ic(t) are determined by the sum of the internal transistor emitter resistance (R_{EQD2}) and the external resistance R_{EX}.
A pole is generated at $1/R_O \cdot C_{EX}$ by the output resistance R_O, and as a result, the frequency characteristics of ic(t) are as shown in the figure below.

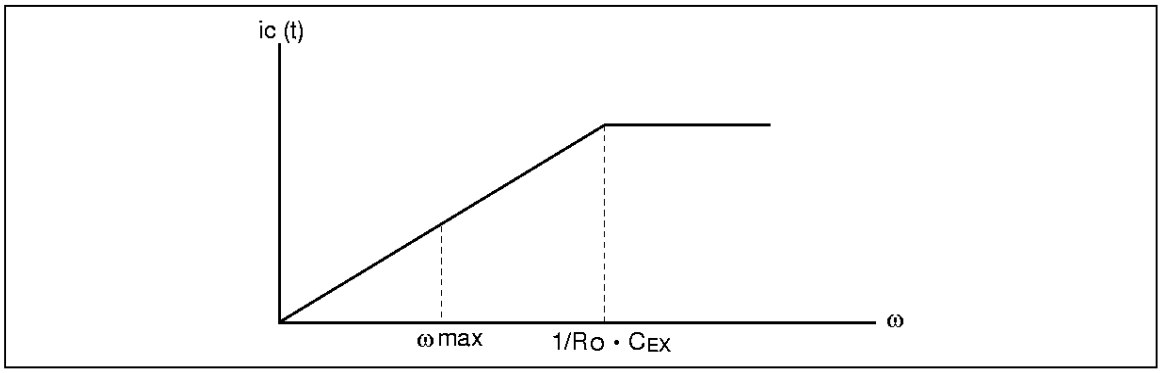


Figure 6-1 Frequency Characteristics due to C_{EX}

Note: The frequency characteristics for C_{EX} in figure 6-1 are for an ideal substrate, and in actual use the position of the pole may not agree with the computation due to parasitic C, L, and R from the substrate. We therefore recommend confirmation of the frequency characteristics in the actual circuit.

$$R_O = \frac{1}{n \cdot C_{EX} \cdot \omega max} \quad (n = 1.5 \text{ to } 3.0)$$

When R_O is larger than the right hand side of the above formula, connect a resistance R_{EX} in series with C_{EX}. In this case the formula becomes:

$$R_O + R_D = \frac{1}{n \cdot C_{EX} \cdot \omega max} \quad (n = 1.5 \text{ to } 3.0)$$

In this case, the gain (A_{VD}) of the differential amplifier will be:

$$A_{VD} = \frac{R_{LD1}}{R_{EQD2} + (R_{EX} + \frac{1}{j\omega C_{EX}}) /2}$$

7. Gate Generator Circuit

A gate signal is applied at positions corresponding to read signal peaks, and it is the gate signal which is used to exclude source and other noise. The HD153014RF has functions for generating this gate signal. In principle, the method adopted for generating the gate signal, is to compare a signal shifted by ΔV_S only, with a signal produced by rectifying the signal input to the AGCINX and AGCINY pins.

Here, ΔV_S is:

$$\Delta V_S = \frac{V_{GGVS}}{3}$$

Where V_{GGVS} is the voltage on the GGVS pin.

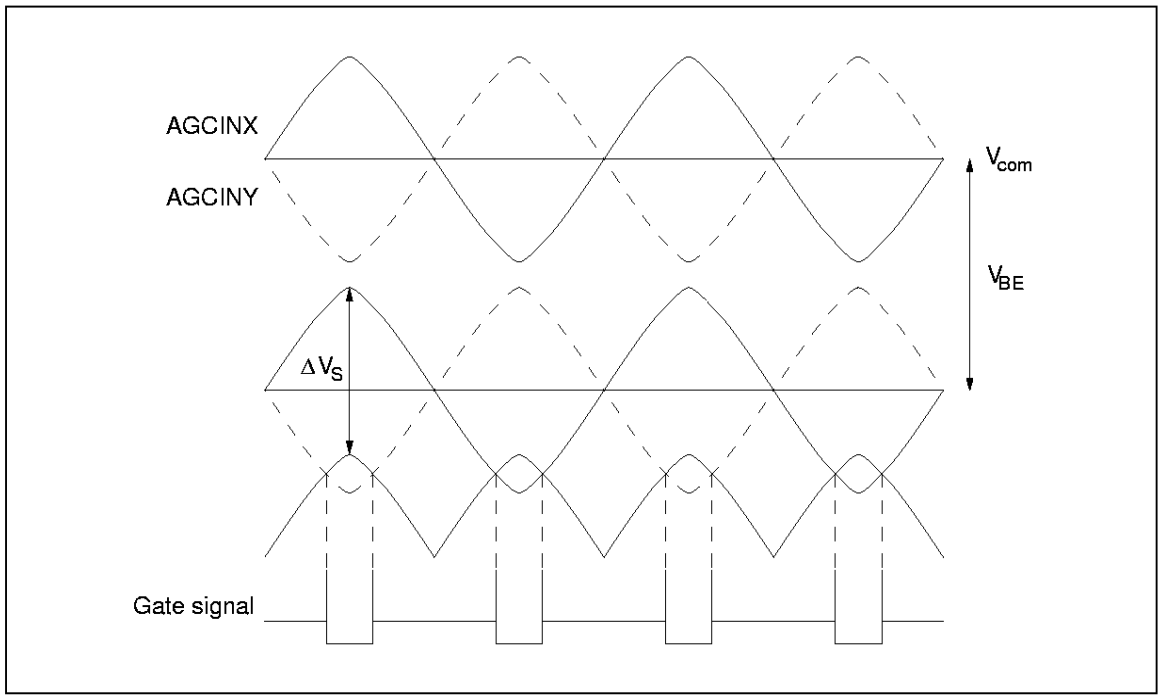
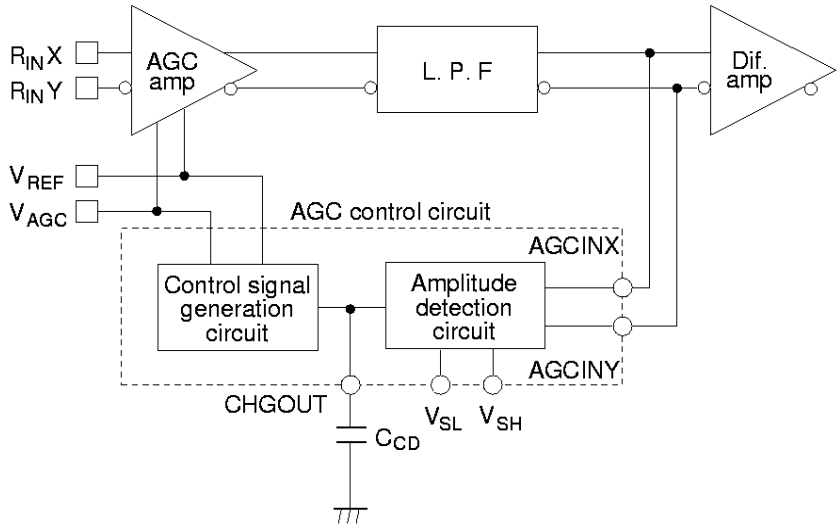
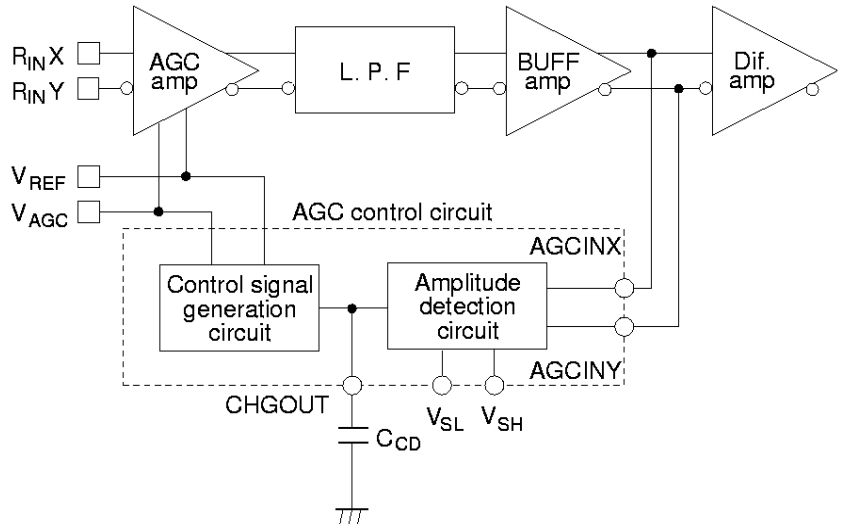


Figure 7-1 Gate Signal Generation Principles

8. AGC Loop



a. AGC Loop Structure, Example 1



b. AGC Loop Structure, Example 2

Figure 8-1 AGC Loop Structures

Figure 8-1 shows examples of AGC loop structures. Example 1 is an example where there is no attenuation in the L.P.F., and example 2 is an example where the type of L.P.F. with a –6 dB loss is used. However, even when an attenuating L.P.F. is used, if an adequate signal amplitude can be obtained with the AGC amplifier gain, then we recommend using the circuit structure in example 1.
Here, the AGC amplifier gain control is handled by the AGC control circuit shown in figure 8-1. In the AGC control circuit, the signals input from the AGCINX, and AGCINY pins are compared with the externally set reference voltages (V_{SL} and V_{SH}), and an external capacitor is charges and discharged. The AGC amplifier gain is controlled by the changes in the control signal VAGC which are due to the charge and discharge of this external capacitor.
The final amplitude Vp (the waveform at the pins AGCINX and AGCINY) in the above control system, can be derived from the following formulas, assuming that the signals are sine waves.

$$T_1 \times Ich = T_2 \times Idis \quad (8\text{-}1)$$

$$T_1 = (1 - \frac{2}{\Pi} \sin^{-1} \frac{V\,com - V_{SH}}{Vp}) \times T \quad (8\text{-}2)$$

$$T_2 = (1 - \frac{2}{\Pi} \sin^{-1} \frac{V\,com - V_{SL}}{Vp}) \times T \quad (8\text{-}3)$$

From formulas (8-1), (8-2), and (8-3) we have:

$$\sin^{-1} \frac{Vcom - V_{SH}}{Vp} - \frac{Idis}{Ich} \sin^{-1} \frac{Vcom - V_{SL}}{Vp} = \frac{\Pi}{2} (1 - \frac{Idis}{Ich}) \quad (8\text{-}4)$$

Here, since the final amplitude of the AGC loop is mainly determined by V_{SH}, the above formulas give the final differential peak voltage V_{PDF} to be:

$$V_{PDF} = 4\,(Vcom - V_{SH}) \times m \quad (8\text{-}5)$$

$m = 1.02$ to 1.04

$Vcom = 0.824 \times (V_{CC} - V_{BE})$

$V_{BE} = 0.75$ V

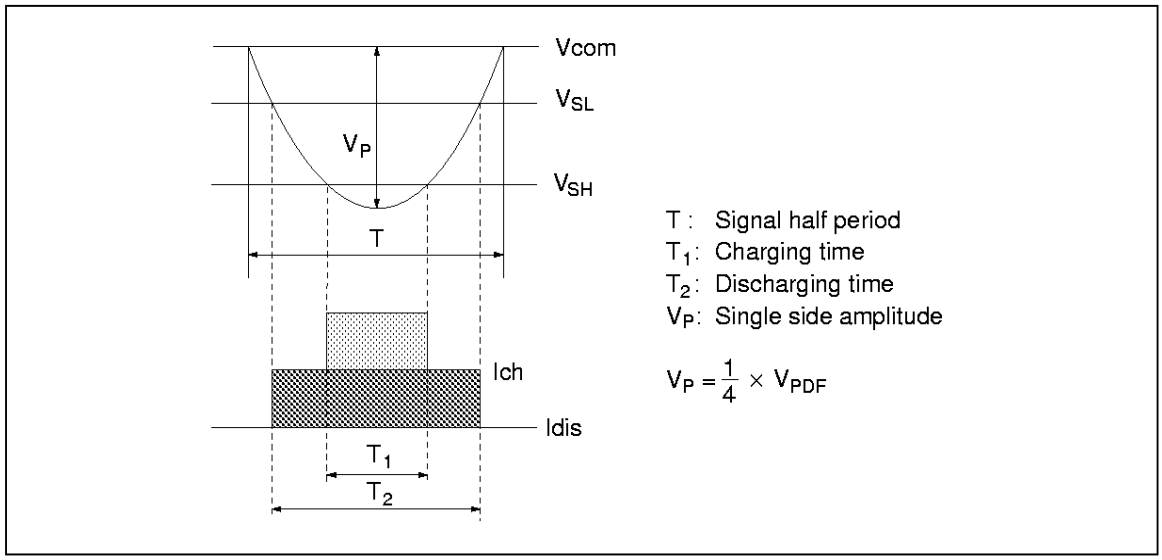


Figure 8-2 Amplitude Detection

Although the V_{PDF} mentioned above is determined from the I/O dynamic range and other parameters of the various amplifiers, A V_{PDF} of about 1.5 V is appropriate. Therefore, (Vcom – V_{SH}) will be in the 0.36 to 0.37 V range. Also, although a V_{SL} level of about

$$Vcom - V_{SL} = \frac{1}{2}(Vcom - V_{SH}) \quad (8\text{-}6)$$

is usually acceptable, it is necessary to determine it according to the discrimination specifications. That is, determine V_{SH} an Vp from formula (8-4), and V_{SL} based on an Ich of 0.55 mA and an Idis of 0.13 mA. Here, attenuation of signal amplitude within the disk with respect to external amplitudes must be considered.

When the input amplitude at this time is attenuated instantaneously from the previous levels, if that attenuated amplitude is not larger than (Vcom – V_{SL}), then the time to recover to a fixed voltage will become extremely long.

9. Application Hints

When the AGC amplifier inputs (RINX and RINY) are attenuated to 50% of their prior values, since the AGC amplifier will continue to amplify at the previous gain for the period of a single cycle, the signals on AGCINX and AGCINY (the AGC control circuit inputs) will also be attenuated by 50%. Next, to increase these to the amplitude determined by V_{SH}, the charge/discharge capacitor will begin to discharge. Since this discharge must take a 50% amplitude to 100%, the amount of the discharge will correspond to the VAGC potential for increasing the gain by a factor of 2. Here, the AGC amplifier gain is given by formula (5-1), and since the required discharge should double this, taking $V_2 = \frac{1}{a}(V_{AGC2} - V_{REF})$ to be the voltage to double the amplification at $V_1 = \frac{1}{a}(V_{AGC2} - V_{REF})$, the formula

$$[1/\{1 + \exp(qV_1/kT)\}] \times 2 = 1/\{1 + \exp(qV_2/kT)\} \quad (9\text{-}1)$$

is established. Also, since the amount of the voltage drop due to this discharge is $V_1 - V_2 = \frac{1}{a}(V_{AGC1} - V_{AGC2})$, the time required for this drop is:

$$t = \frac{C_{CD}(V_1 - V_2)}{Idis} = \frac{C_{CD}\frac{1}{a}(V_{AGC1} - V_{AGC2})}{Idis} \quad (9\text{-}2)$$

Inversely, if the AGC amplifier input is suddenly doubled, the time required is:

$$t = \frac{C_{CD}(V_1 - V_2)}{Ich} = \frac{C_{CD}\frac{1}{a}(V_{AGC1} - V_{AGC2})}{Ich} \quad (9\text{-}3)$$

Note that if the AGC amplifier input is attenuated, it is necessary that the attenuated amplitude be grater than (Vcom – V_{SL}). If it is smaller than (Vcom – V_{SL}), the recovery will be extremely slow.