

Signetics

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FAST 74F1766 Burst Mode DRAM Controller (BMDC)

FEATURES

- Allows burst-mode access for systems using Nibble/Page/Static column mode DRAMs
- Complete control of DRAM access, acknowledge, refresh and address multiplexing functions
- True RAS interleaving for minimum refresh and RAS precharge overhead
- Asynchronous arbitration to speed up accesses
- Selectable Precharge and Acknowledge times
- Selectable Row address hold times
- Supports CAS before RAS refresh
- Allows control of dynamic RAMs with row access times down to 30ns
- Output drivers designed for incident wave switching

DESCRIPTION

The Signetics Burst Mode DRAM Controller (BMDC) is a high performance memory timing generator designed to support Page, Nibble or Static Column modes of operation in addition to the normal DRAM access cycles. It performs memory access/refresh arbitration, refresh and memory access timing, RAS interleaving, CAS byte decoding and controls up to four banks of DRAM.

The BMDC generates DRAM timing and thus requires a companion address multiplexer like the 74F1762 Memory Address Multiplexer for row and column address generation. This provides the flexibility of using the controller with any size of DRAM array by simply using an appropriate address multiplexer. For example when used with the 74F1762, it can control 4Mbit DRAMs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1766	150MHz	200mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$
48-Pin Plastic DIP	N74F1766N
44-Pin PLCC	N74F1766A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

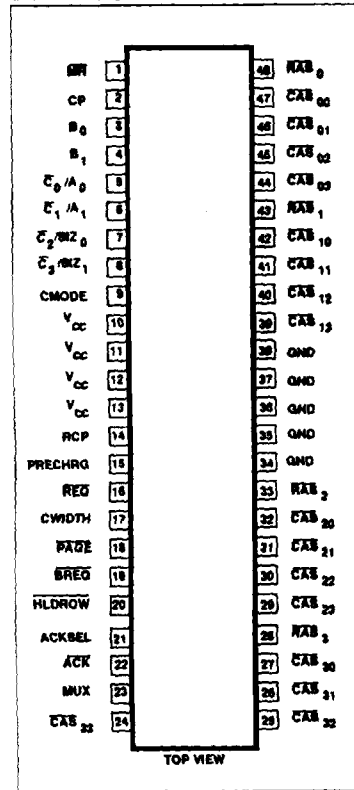
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{C}_0/A_0, \overline{C}_1/A_1,$ $\overline{C}_2/SIZ_0, \overline{C}_3/SIZ_1,$	CAS Enable inputs	1.0/1.0	20 μ A/0.6mA
PRECHRG	RAS Precharge Select Input	1.0/1.0	20 μ A/0.6mA
\overline{REQ}	Memory access request input	1.0/1.0	20 μ A/0.6mA
CP	Clock input	1.0/1.0	20 μ A/0.6mA
RCP	Refresh clock input	1.0/1.0	20 μ A/0.6mA
B_0, B_1	Bank select inputs	1.0/1.0	20 μ A/0.6mA
\overline{MR}	Reset input	1.0/1.0	20 μ A/0.6mA
\overline{BREQ}	Burst request input	1.0/1.0	20 μ A/0.6mA
ACKSEL	Acknowledge select input	1.0/1.0	20 μ A/0.6mA
\overline{HLDROW}	Row address hold select input	1.0/1.0	20 μ A/0.6mA
PAGE	Page mode select input	1.0/1.0	20 μ A/0.6mA
CMODE	CAS mode select input	1.0/1.0	20 μ A/0.6mA
CWIDTH	CAS width select input	1.0/1.0	20 μ A/0.6mA
\overline{ACK}	Acknowledge output	750/40	3.0mA/24mA
MUX	Address Multiplexer output	150/40	15.0mA/24mA
\overline{RAS}_{0-3}	Row address strobe outputs	750/40	15.0mA/24mA
\overline{CAS}_{00-33}	Column address strobe outputs	750/40	15.0mA/24mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state

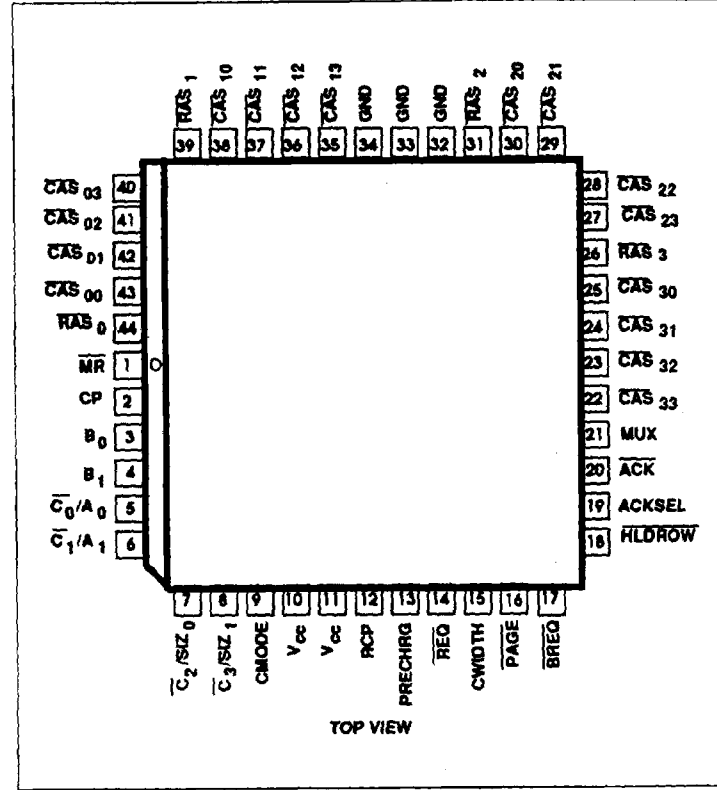
Burst Mode DRAM Controller (BMDC)

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DIP PIN CONFIGURATION



PLCC PIN CONFIGURATION



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PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
CP	2	2	Input	Clock input. Used by the controller for all timing and arbitration functions.
RCP	14	12	Input	Refresh clock input. Divided internally by 64 to produce an internal Refresh Request.
PRECHRG	15	13	Input	$\overline{\text{RAS}}$ Precharge input. A Low will program the Controller to guarantee 4 CP clock cycles of precharge. A High will guarantee 3 clock cycles of precharge.
$\overline{\text{REQ}}$	16	14	Input	Active Low Memory Access Request input, must be asserted for the entire DRAM access cycle. $\overline{\text{REQ}}$ is sampled on the rising edge of the CP clock.
B_0, B_1	3,4	3,4	Input	$\overline{\text{RAS}}$ Bank Select inputs. See Table 1 for decoding information.
$\overline{\text{BREQ}}$	19	17	Input	Active Low Burst Request input. If active during an access cycle, the controller automatically toggles $\overline{\text{CAS}}_x$ outputs for burst access. The duration of the $\overline{\text{CAS}}_x$ outputs are controlled by the $\overline{\text{CWIDTH}}$ and $\overline{\text{PAGE}}$ inputs.
ACKSEL	21	19	Input	Acknowledge timing Select input. A Low will program the Controller to assert $\overline{\text{ACK}}$ output 2 CP clock cycles after $\overline{\text{CAS}}_x$ is asserted. When High $\overline{\text{ACK}}$ output will be asserted at the time of assertion of $\overline{\text{CAS}}_x$.
$\overline{\text{HLDROW}}$	20	18	Input	Row Address Hold input. A Low will program the Controller to assert MUX output 1/2 CP clock cycles after $\overline{\text{RAS}}_x$ is asserted. When High MUX output will be asserted at the time of assertion of $\overline{\text{RAS}}_x$.
$\overline{\text{ACK}}$	22	20	Output	Active Low, 3-state Acknowledge output. Asserted as selected by the ACKSEL input. This is asserted only once during a burst or non-burst memory access cycle, and is not asserted during a memory refresh cycle.
CMODE	9	9	Input	$\overline{\text{CAS}}$ Mode select input. When Low $\overline{\text{CAS}}_x$ outputs are enabled directly by the $\overline{\text{C}}_{0-3}$ inputs. When High $\overline{\text{CAS}}_x$ outputs are enabled by decoding the A_{0-1} and SIZ_{0-1} inputs (see Table 2).
$\overline{\text{C}}_0/A_0$	5	5	Input	$\overline{\text{CAS}}_{x0}$ enable input. As selected by the CMODE input. "X" indicates Banks 0-3.
$\overline{\text{C}}_1/A_1$	6	6	Input	$\overline{\text{CAS}}_{x1}$ enable input. As selected by the CMODE input. "X" indicates Banks 0-3.
$\overline{\text{C}}_2/SIZ_0$	7	7	Input	$\overline{\text{CAS}}_{x2}$ enable input. As selected by the CMODE input. "X" indicates Banks 0-3.
$\overline{\text{C}}_3/SIZ_1$	8	8	Input	$\overline{\text{CAS}}_{x3}$ enable input. As selected by the CMODE input. "X" indicates Banks 0-3.
$\overline{\text{RAS}}_{0-3}$	48,43, 33,28	44,39, 31,26	Output	Active Low Row Address Strobe outputs. Asserted as dictated by the B_{0-1} inputs. (see Table 1 for decoding information)
$\overline{\text{CWIDTH}}$	17	15	Input	$\overline{\text{CAS}}_x$ pulse Width select input. This input selects the initial $\overline{\text{CAS}}_x$ pulse width in the burst mode. When Low the initial $\overline{\text{CAS}}_x$ pulse is selected equal to 3 CP clock cycles and when High it's selected equal to 2 CP clock cycles. This input is ignored in the non-burst mode.
MUX	23	21	Output	Row/Column address Multiplex output. Asserted as selected by the $\overline{\text{HLDROW}}$ input and is used by an external address multiplexer like the 74F1762.
$\overline{\text{CAS}}_{00-33}$	47-44, 42-39, 32-29, 27-24	43-40, 38-35, 30-27, 25-22	Output	Active Low Column Address Strobe outputs. Asserted when enabled by the $\overline{\text{CAS}}_x$ enable inputs (Table 2) and $\overline{\text{RAS}}_x$ bank circuitry.
$\overline{\text{PAGE}}$	18	16	Input	$\overline{\text{PAGE}}$ mode select input. Controls $\overline{\text{CAS}}_x$ pulse width after the initial $\overline{\text{CAS}}_x$ pulse in the burst mode. When this input is Low the $\overline{\text{CAS}}_x$ pulse is selected equal to 2 CP cycles and when High it's selected equal to 1 CP cycle. This is ignored in the non-burst mode.
$\overline{\text{MR}}$	1	1	Input	Active Low Master Reset input. The first Low to High transition on the CP clock after $\overline{\text{RESET}}$ is Low will reset the controller. After reset, the 74F1766 remains in test mode until the first rising edge of CP clock.
Vcc	10-13	10,11		Power
GND	34-38	32-34		Ground

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ARCHITECTURE

The 74F1766 Burst Mode DRAM controller is a synchronous device, with all signal generation being a function of the input clock (CP).

The F1766 Block Diagram (Figure 1) shows the overall architecture of the device. The refresh generator uses CAS before RAS refresh and produces refresh requests based upon the frequency of the refresh clock (RCP). A memory refresh request is generated for all four banks every 64 cycles of the RCP clock. This request is arbitrated individually for all banks with it's corresponding memory access request made through the REQ input. If both memory access and refresh requests are active at a given time the request sampled first will begin immediately and the other request (if still asserted) will be serviced upon completion of the current cycle and it's associated

precharge time.

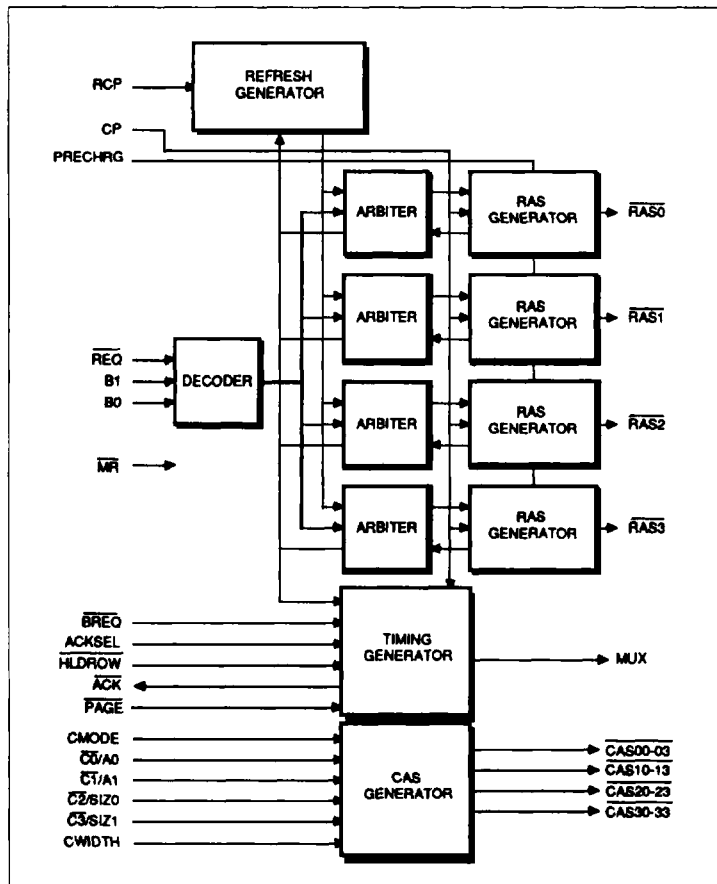
Every one of the four banks have individual refresh monitors to keep track of any missed refreshes during a long page mode access. A total of 127 missed refreshes can be stored by each bank. After the page mode access cycle the controller will burst refresh that bank until all missed refreshes have been performed. In order to limit the number of outputs switching at the same time the refresh generator will stagger the refresh cycles to individual banks, starting from Bank 0. The bank select inputs (B_{0-3}) select which RAS_x output will be enabled during the access cycle. Each RAS_x output has it's own arbiter and timing generator to allow true RAS interleaving between access cycles and refresh cycles. This also enables transparent RAS precharge between access cycles. The RAS precharge time can be selected by the PRECHRG input to be equal to either 3 or

4 CP clock cycles.

The timing generator allows burst or non-burst accesses selected by the BREQ input. If BREQ input is asserted during a memory access cycle the controller will automatically toggle CAS_x outputs for burst accesses. The duration of the first CAS_x pulse is determined by the CWIDTH input, and by the PAGE input for subsequent CAS_x pulses. This is particularly useful when block moves are made into and out of memory for cache transfers. The CAS_x outputs may be gated by the byte select inputs (C_{0-3}) or by a decoding function generated by the $A_0/A_1/SIZ_0/SIZ_1$, using the CMODE input. Each RAS output has an associated set of CAS outputs for that bank, for example RAS_0 uses CAS_{00-03} outputs. This allows simultaneous refresh of RAS banks while another bank is being accessed by the processor.

The ACKSEL input allows the assertion of Acknowledge (ACK) output to be either when CAS_x is asserted or 2 CP clock cycles after that. ACK stays asserted in the burst mode until REQ is negated. The HLDROW input can be used to assert MUX output when RAS_x is asserted or one-half CP clock cycle after that.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Most DRAMs require that RAS and CAS inputs be toggled a number of times before the DRAM may be used. The BMDC has an initialization feature which allows the automatic exercising of the DRAMs. This is done by resetting the device, which forces the refresh counter to be offset by ten, thus forcing ten refresh cycles before allowing any memory access cycles. The REQ input is sampled on the rising edge of the CP clock. If no refresh request is being serviced, one of the RAS_x outputs (depending on the B_{0-1} inputs) will be asserted immediately. Depending on the state of the HLDROW input, the MUX output will be driven High either at the assertion of RAS_x or one-half CP cycle after that. One CP cycle after the assertion of RAS_x , the CAS_x outputs enabled either by the C_{0-3} inputs or the decoded function of $A_0/A_1/SIZ_0/SIZ_1$ (as selected by the CMODE input) will be asserted. If the ACKSEL input is High, the ACK output will be asserted at this time; otherwise it will be asserted 2 CP cycles after this time.

The BREQ input is sampled when the CAS_x outputs are initially asserted, and this determines what will take place on the CAS_x outputs after their initial assertion. If BREQ is High, the RAS_x , MUX and CAS_x outputs will remain in their present state until the negation of REQ, at which time all these signals are negated. Negation of REQ is asynchronous to the CP clock cycle and therefore is not sampled

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by the clock. If the $\overline{\text{BREQ}}$ is Low at the assertion of CAS_x , the RAS_x and MUX outputs will stay in their existing state but the CAS_x outputs after staying Low for 2 CP cycles will alternately be negated and asserted for one CP clock cycle if PAGE input is High or for two CP clock cycles if PAGE input is Low. This process will continue until the negation of the $\overline{\text{REQ}}$ input, at which time the RAS_x , MUX, $\overline{\text{CAS}}_x$ and $\overline{\text{ACK}}$ outputs will be negated.

As mentioned before, the controller guarantees a RAS precharge on all the RAS_x outputs to be either 3 or 4 CP clock cycles as selected by the $\overline{\text{PRECHRG}}$ input. This precharge function is independent among the RAS_x outputs, which means that, by connecting the appropriate low-order address lines from the processor to the $\text{B}_{0,1}$ inputs, sequential accesses, a common occurrence with microprocessors, will result in no precharge overhead.

The refresh function is also independent

between the RAS_x outputs, which means that three RAS_x outputs can be performing a CAS before RAS refresh, while the fourth is in the precharge mode or is being accessed, thus reducing the overall refresh overhead.

Output driving Characteristics

Considering the transmission line characteristics of the DRAM arrays, the outputs of the DRAM controller have been designed to provide incident-edge switching (in Dual-In-line-Packaged memory arrays), needed in high performance systems. For more information on the driving characteristics, please refer to Signetics application note number AN218. The driving characteristics of the 74F1766 are the same as those of the 74F765 shown in the application note.

Testing the BMDC

Precautions have been taken in the design of the BMDC to facilitate testing of the device. After a $\overline{\text{MR}}$ is issued and the

CP input is toggled from Low to High all internal flip-flops are brought into a known state, and the device goes into the test mode from the time $\overline{\text{MR}}$ is deasserted till the time the first Low to High transition occurs on the CP clock. During the test mode, bank refresh counters (that keep track of missed refreshes) are clocked by a High to Low transition on the $\overline{\text{C}}_{0,3}$ inputs and the main refresh counter is clocked on the rising RCP clock edge. The comparators that compare the contents of the main refresh counter and refresh counters of individual banks are clocked by the Low to High transition on the $\overline{\text{PRECHRG}}$ input and are gated on to RAS_x outputs by the $\overline{\text{C}}_{0,3}$ inputs. So whenever $\overline{\text{C}}_{0,3}$ are Low, RAS outputs are disabled (pulled High). If the contents of the main refresh counter and the individual bank counters are equal, the corresponding RAS output will be High, if not equal the corresponding RAS output will be Low. This allows full testing of the Counters and comparators with relatively few lines of code.

B_0	B_1	RAS_0	RAS_1	RAS_2	RAS_3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	0	1	0	1
1	1	0	1	1	0

TABLE 1: BANK SELECT DECODE

CMODE	OPERATION	$\overline{\text{C}}_3/\text{SIZ}_1$	$\overline{\text{C}}_2/\text{SIZ}_0$	$\overline{\text{C}}_1/\text{A}_1$	$\overline{\text{C}}_0/\text{A}_0$	$\overline{\text{CAS}}_{x3}$	$\overline{\text{CAS}}_{x2}$	$\overline{\text{CAS}}_{x1}$	$\overline{\text{CAS}}_{x0}$
1	LONG WORD	0	0	0	0	0	0	0	0
1		0	0	0	1	0	0	0	1
1		0	0	1	0	0	0	1	1
1		0	0	1	1	0	1	1	1
1	BYTE	0	1	0	0	1	1	1	0
1		0	1	0	1	1	1	0	1
1		0	1	1	0	1	0	1	1
1		0	1	1	1	0	1	1	1
1	WORD	1	0	0	0	1	1	0	0
1		1	0	0	1	1	0	0	1
1		1	0	1	0	0	0	1	1
1		1	0	1	1	0	1	1	1
1	THREE BYTES	1	1	0	0	1	0	0	0
1		1	1	0	1	0	0	0	1
1		1	1	1	0	0	0	1	1
1		1	1	1	1	0	1	1	1

TABLE 2: BYTE SELECT DECODE

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ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current	All pins except \overline{ACK}		-15	mA
		\overline{ACK} output		-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹			LIMITS			UNIT
						Min	Typ ²	Max	
V_{OH}	High-level output voltage	All pins except \overline{ACK}	$V_{CC} = \text{MIN},$ $V_{IL} = \text{MAX},$ $V_{IH} = \text{MIN}$	$I_{OH} = -15\text{mA}$	$\pm 10\%V_{CC}$	2.5	3.2		V
V_{OH2}^3					$\pm 5\%V_{CC}$	2.7	3.4		V
V_{OH}		\overline{ACK}	$V_{CC} = \text{MIN},$ $V_{IL} = \text{MAX},$ $V_{IH} = \text{MIN}$	$I_{OH} = \text{MAX}$	$\pm 10\%V_{CC}$	2.4			V
					$\pm 5\%V_{CC}$	2.7	3.3		V
V_{OL}	Low-level output voltage	All pins except \overline{ACK}	$V_{CC} = \text{MIN},$ $V_{IL} = \text{MAX},$ $V_{IH} = \text{MIN}$	$I_{OL} = 24\text{mA}$	$\pm 10\%V_{CC}$		0.35	0.50	V
V_{OL2}^3					$\pm 5\%V_{CC}$		0.35	0.50	V
V_{OL}		\overline{ACK}	$V_{CC} = \text{MIN},$ $V_{IL} = \text{MAX},$ $V_{IH} = \text{MIN}$	$I_{OL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.35	0.50	V
					$\pm 5\%V_{CC}$		0.35	0.50	V
V_{IK}	Input clamp voltage		$V_{CC} = \text{MIN}, I_1 = I_{IK}$				-0.73	-1.2	V
I_1	Input current at maximum input voltage		$V_{CC} = 0.0\text{V}, V_1 = 7.0\text{V}$					100	μA
I_{IH}	High-level input current		$V_{CC} = \text{MAX}, V_1 = 2.7\text{V}$					20	μA
I_{IL}	Low-level input current		$V_{CC} = \text{MAX}, V_1 = 0.5\text{V}$					-0.6	mA
I_{OZH}	Off-state output current, High level voltage applied		$V_{CC} = \text{MAX}, V_o = 2.7\text{V}$					50	μA
I_{OZL}	Off-state output current, Low level voltage applied		$V_{CC} = \text{MAX}, V_o = 0.5\text{V}$					-50	μA
I_{OS}^4	Short-circuit output current		$V_{CC} = \text{MAX}$	All pins except \overline{ACK}	-100		-225	mA	
				\overline{ACK} output	-60		-150	mA	
I_{CC}	Supply current (total)	I_{CCH}	$V_{CC} = \text{MAX}$			185	240	mA	
		I_{CCL}				200	260	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- I_{OH}^2 & I_{OL}^2 are transient currents necessary to guarantee a Low to High & a High to Low transition in a 30 OHM transmission line respectively. Refer to Application note number AN218 for further explanation.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shoring of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS

NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A=25^\circ\text{C}$ $V_{cc}=+5.0\text{V}\pm 10\%$ $C_L=300\text{pF}$ $R_L=70\Omega$			$T_A=0^\circ\text{C to }+70^\circ\text{C}$ $V_{cc}=+5.0\text{V}\pm 10\%$ $C_L=300\text{pF}$ $R_L=70\Omega$		
			Min	Typ	Max	Min	Max	
1	CP clock period (tcp)		10			10		ns
2	CP clock low time		4			4		ns
3	CP clock high time		6			6		ns
4	RCP clock period		100			100		ns
5	RCP clock low time		10			10		ns
6	RCP clock high time		10			10		ns
7	Setup time $\overline{\text{REQ}}(\downarrow)$ to CP(\uparrow)		2.5			4		ns
8	Setup time B ₀ , B ₁ to CP(\uparrow)		3			4		ns
9	Setup time $\overline{\text{BREQ}}$ to CP(\uparrow)		3			4		ns
10	Propagation delay CP(\uparrow) to $\overline{\text{RAS}}(\downarrow)$		3	7.5	9.5	3	10	ns
11	Propagation delay $\overline{\text{REQ}}(\uparrow)$ to $\overline{\text{RAS}}(\uparrow)$		4	9	12	3	13	ns
12	Propagation delay CP(\uparrow) to MUX(\uparrow)	$\overline{\text{HLDROW}} = 1$	3	8	10	3	11	ns
13	Propagation delay CP(\downarrow) to MUX(\uparrow)	$\overline{\text{HLDROW}} = 0$	2	5.5	7.5	2	8.5	ns
14	Propagation delay $\overline{\text{REQ}}(\uparrow)$ to MUX(\downarrow)		4	8.5	10.5	4	11.5	ns
15	Propagation delay CP(\uparrow) to $\overline{\text{CAS}}(\downarrow)$		3	8.5	11.5	3	12	ns
16	Propagation delay $\overline{\text{REQ}}(\uparrow)$ to $\overline{\text{CAS}}(\uparrow)$		4	9.5	12	4	14	ns
17	Propagation delay CP(\uparrow) to $\overline{\text{CAS}}(\uparrow)$	$\overline{\text{BREQ}} = 0$	3	8	10	3	11	ns
18	Propagation delay CP(\uparrow) to $\overline{\text{CAS}}(\downarrow)$	$\overline{\text{BREQ}} = 0$	3	9	11	3	12	ns
19	Propagation delay $\overline{\text{REQ}}(\downarrow)$ to $\overline{\text{ACK}}$ (3-state to High)		2	5	7	2	8	ns
20	Propagation delay CP(\uparrow) to $\overline{\text{ACK}}(\downarrow)$	ACKSEL = 1	3	7.5	9.5	3	10	ns
21	Propagation delay CP(\uparrow) to $\overline{\text{ACK}}(\downarrow)$	ACKSEL = 0	3	7.5	9.5	3	10	ns
22	Propagation delay $\overline{\text{REQ}}(\uparrow)$ to $\overline{\text{ACK}}$ (Low to 3- state)		2	5	7	2	7.5	ns
23	Propagation delay CP(\uparrow) to $\overline{\text{CAS}}(\downarrow)$ *	REFRESH CYCLE	4	9.5	12	4	13	ns
24	Propagation delay CP(\uparrow) to $\overline{\text{RAS}}(\downarrow)$ *	REFRESH CYCLE	3	7.5	9.5	3	10	ns
25	Propagation delay CP(\uparrow) to $\overline{\text{CAS}}(\uparrow)$ *	REFRESH CYCLE	4	9.5	12	4	14	ns
26	Propagation delay CP(\uparrow) to $\overline{\text{RAS}}(\uparrow)$ *	REFRESH CYCLE	4	9	11	3	13	ns
27	Propagation delay $\overline{\text{RAS}}(\downarrow)$ to $\overline{\text{CAS}}(\downarrow)$		1tcp-1	1tcp+1	1tcp+2.5	1tcp-1	1tcp+3	ns

* The same parameters will hold for a refresh cycle during $\overline{\text{RAS}}_1$, $\overline{\text{RAS}}_2$ and $\overline{\text{RAS}}_3$ access cycles.

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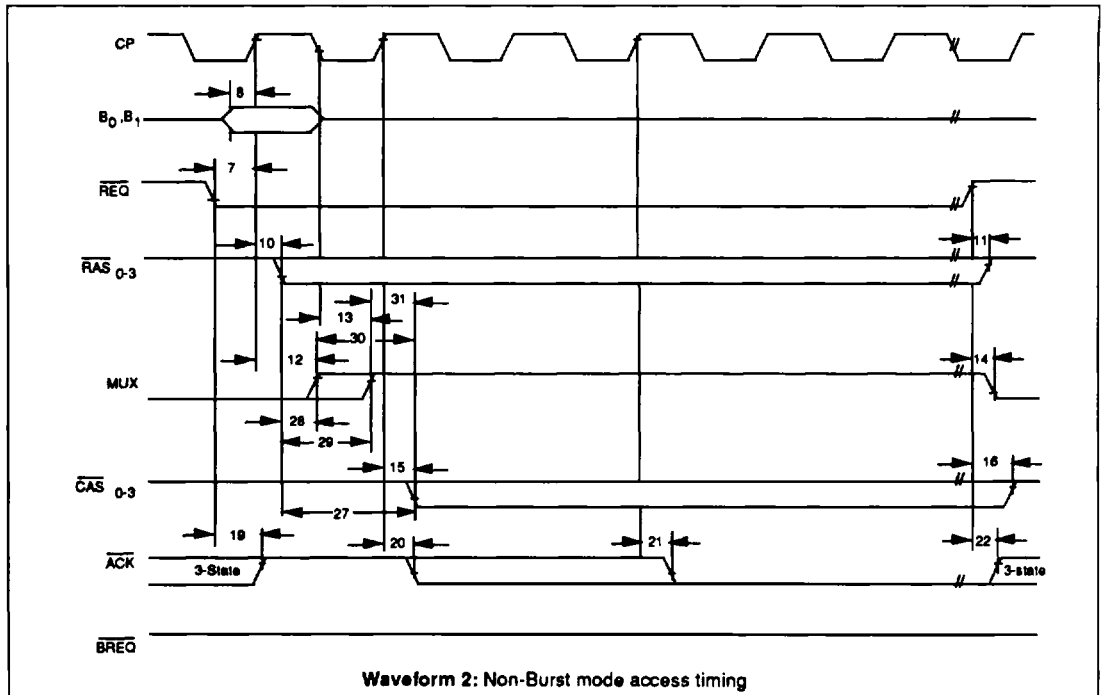
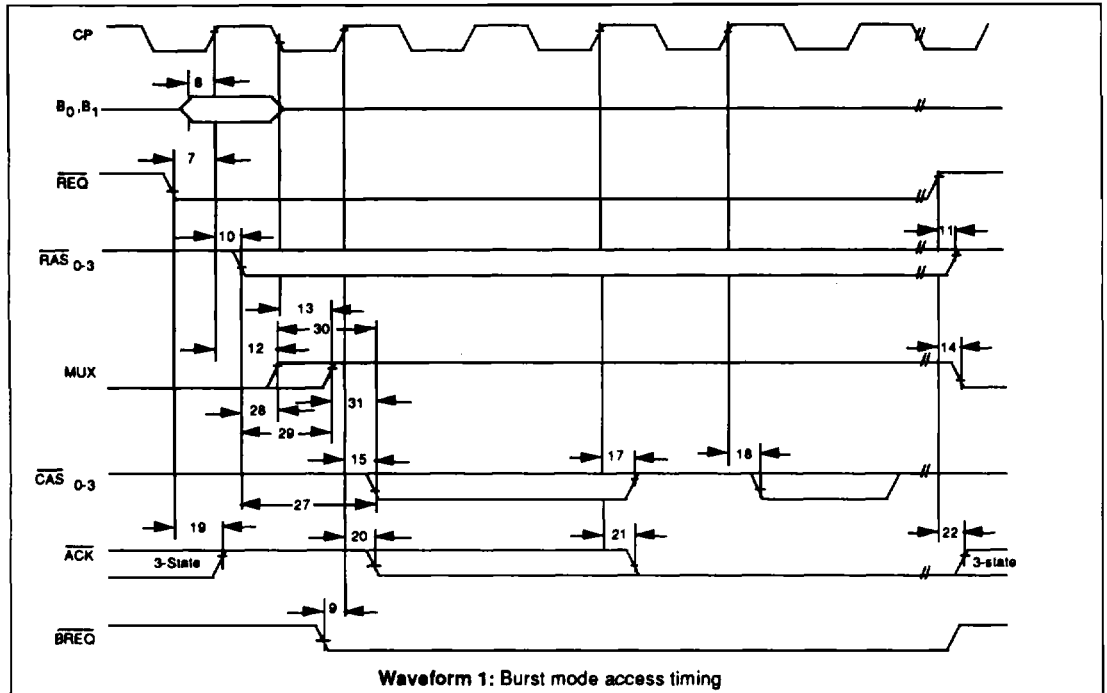
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AC ELECTRICAL CHARACTERISTICS

NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _A =25°C V _{cc} =+5.0V ±10% C _L =300pF RL=70Ω			T _A =0°C to +70°C V _{cc} =+5.0V ±10% C _L =300pF RL=70Ω		
			Min	Typ	Max	Min	Max	
28	Propagation delay $\overline{\text{RAS}}(\downarrow)$ to MUX(\uparrow)	HLDROW = 1	-1	0.5	2	-1.5	2.5	ns
29	Propagation delay $\overline{\text{RAS}}(\downarrow)$ to MUX(\uparrow)	HLDROW = 0	1/2t _{cp} -3.5	1/2t _{cp} -1.5	1/2t _{cp}	1/2t _{cp} -1.5	1/2t _{cp} +2.5	ns
30	Propagation delay MUX(\uparrow) to $\overline{\text{CAS}}(\downarrow)$	HLDROW = 1	t _{cp} -1.5	t _{cp} +0.5	t _{cp} +2	t _{cp} -2.5	t _{cp} +2.5	ns
31	Propagation delay MUX(\uparrow) to $\overline{\text{CAS}}(\downarrow)$	HLDROW = 0	1/2t _{cp} +0.5	1/2t _{cp} +2	1/2t _{cp} +4.5	1/2t _{cp} -0.5	1/2t _{cp} +5	ns

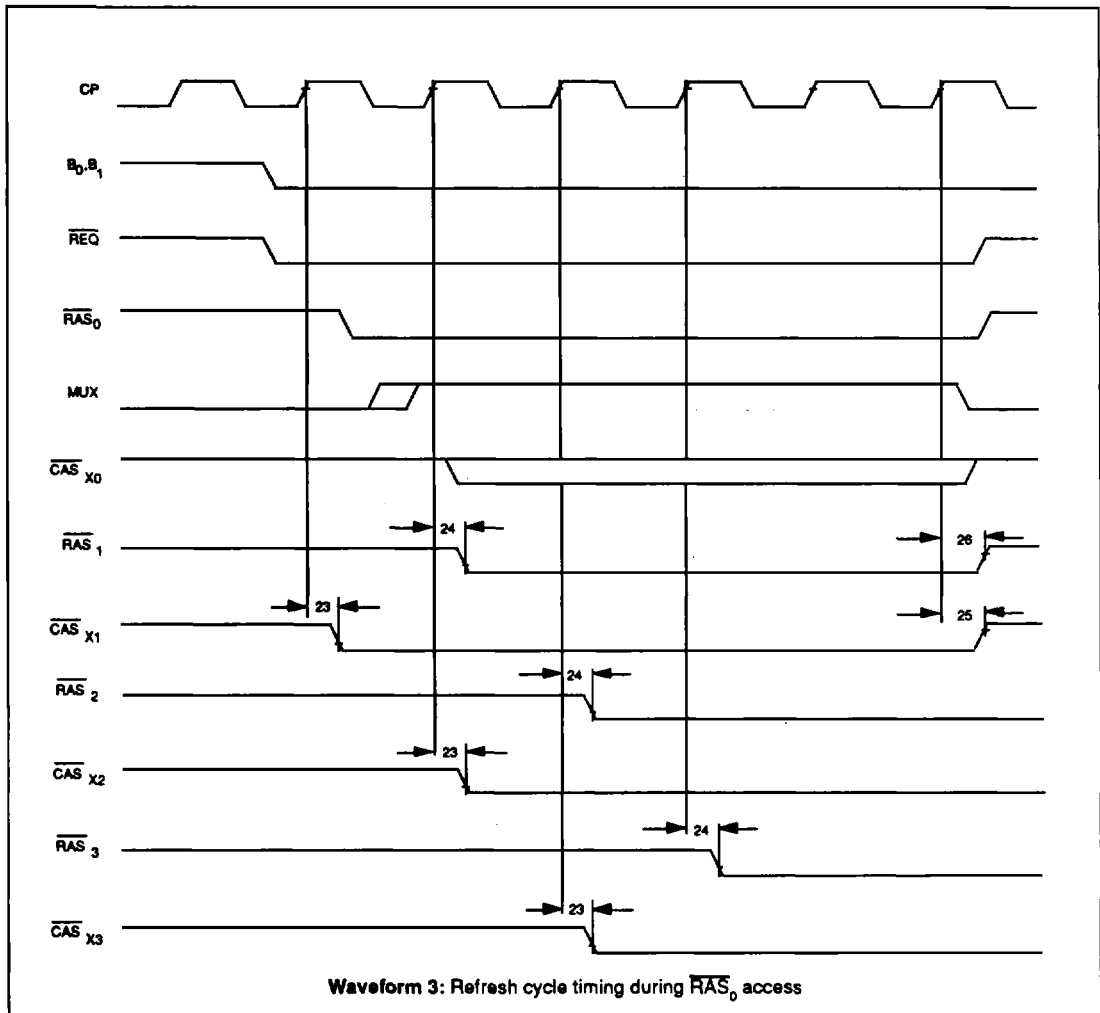
Burst Mode DRAM Controller (BMDC)

FAST 74F1766



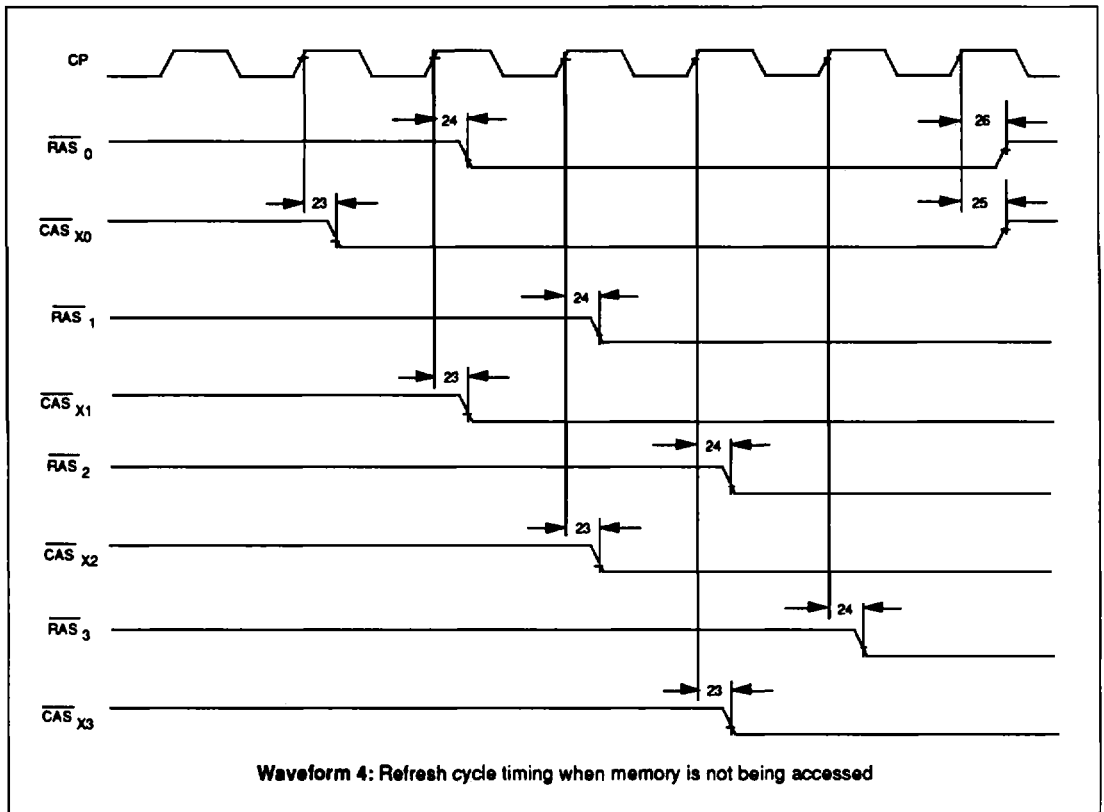
Burst Mode DRAM Controller (BMDC)

FAST 74F1766

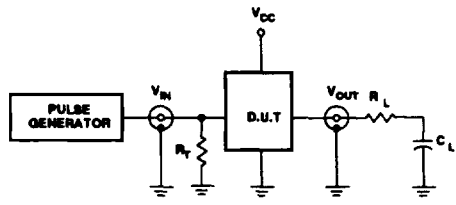


Burst Mode DRAM Controller (BMDC)

FAST 74F1766



TEST CIRCUIT AND WAVEFORMS



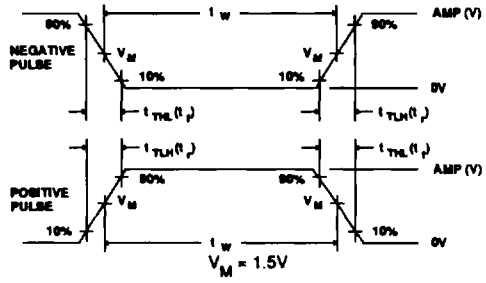
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns