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PCM 'A'-LAW CODEC

MJ1480 DIGITAL CONTROLLER SL1480 ANALOGUE PROCESSOR

8-BIT COMPANDED 'A'-LAW A-D AND D-A CONVERTER

The bipolar SL1480 and NMOS MJ1480 integrated circuits together form a Codec system for the analogue to digital and digital to analogue conversion of telephony speech signals to PCM, as shown in Fig.2. The system is suitable for use in asynchronous transmission equipment and synchronous subscriberline cards. The conversion law is non-linear and conforms to the A law as defined by the CCITT Orange Book, Vol III—2, G711. The SL1480 performs the analogue signal processing functions, and the MJ1480 provides the successive approximation register and PCM interface circuits. The system is designed to operate at a 2.048MHz clock rate and requires a channel clock input to initiate an encode-decode cycle. Digital inputs and outputs are in serial NRZ form with alternate bits inverted, synchronous with the clock. An encode is performed in 11 clock periods and a decode is instantaneous. The system can serve 16 analogue channels at a sampling rate of 8kHz when provided with a 2.048MHz clock and the appropriate channel clocks. An internal two-channel multiplexer is provided to facilitate the use of external multiplexers on both the input and output analogue channels.

The analogue inputs are differential to provide good rejection against clocks and other common mode signals. The analogue outputs are high speed operational amplifiers which are driven by the D-A converter during decode; when the Codec is in encode mode or an output is not selected it is set to zero volts. The relationship of digital information on the PCM highways and analogue samples on the two channels is shown in the timing diagrams, Figs.3a and 3b.

The encode cycle consists of two guard bits, seven encode bits and two further guard bits. When a 2.048MHz clock is used the encode sample period is 4 μ s. The aperture error is sufficiently small with this length of sample that an input sample and hold is unnecessary and provides no performance advantage.

ABSOLUTE MAXIMUM RATINGS

Electrical

SL1480

| | |
|--------------------------------|---|
| V_{IN} to Gnd | +5.5V |
| V_{EE} to Gnd | -5.5V |
| Digital inputs (pins 1-10, 12) | +5.5V to -0.5V |
| Analogue inputs (pins 18-21) | V_{CC} to V_{EE} |
| Differential input voltage | $\pm 3.0V$ $V_{18} - V_{19}$ $V_{20} - V_{21}$ |

MJ1480

| | |
|-----------------|----------------|
| V_{DD} to Gnd | +7V |
| Logical inputs | -0.3V to +7.0V |

Thermal

SL1480 and MJ1480

| | |
|---|-----------------|
| Chip-to-case thermal resistance | 15°C/Watt |
| Chip-to-case ambient thermal resistance | 60°C/Watt |
| Operating ambient temperature | 0°C to +70°C |
| Storage temperature | -55°C to +175°C |
| Maximum junction temperature | +150°C |

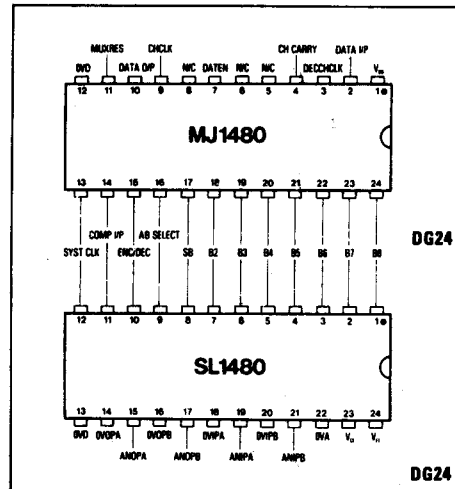


Fig.1 Pin connections SL1480 and MJ1480 (top view)

FEATURES

- Two Chip System May Be Shared Up To 16 Channels
- Includes Internal Two Channel Multiplexer
- Low Power Consumption — Equivalent to 76mW per Channel in Multiplexed Mode (8 Channels)
- Meets All Relevant CCITT Specifications
- May be Simply Designed Into a 32 Channel Security Zone Channel Bank
- Fast A-D Conversion Time, 6 μ s (With 2.048MHz Clock)
- Requires No External Components For Two Channel Application
- Highly Stable On-Chip Voltage Reference
- Supply Requirements $\pm 5V$, $\pm 5\%$
- All Digital Inputs and Outputs TTL Compatible

APPLICATIONS

- 30/32 Channel PCM Systems
- Data Acquisition
- Telemetry
- Digital Signal Processing
- Speech Synthesis
- Voice Recognition

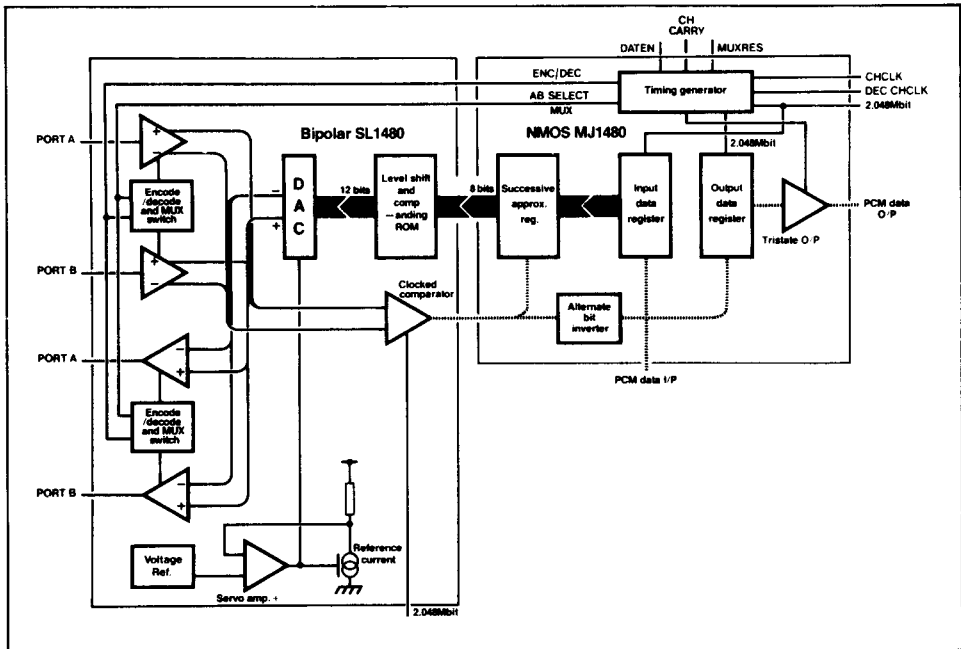


Fig. 2 Codec block diagram and partitioning

FUNCTIONAL PIN DESCRIPTION

SL1480

| Pin No. | Symbol | Description | |
|---------|-----------------|--|--------|
| 1 | B8 | Data, bit 8 (LSB) | |
| 2 | B7 | Data, bit 7 | |
| 3 | B6 | Data, bit 6 | |
| 4 | B5 | Data, bit 5 | |
| 5 | B4 | Data, bit 4 | |
| 6 | B3 | Data, bit 3 | |
| 7 | B2 | Data, bit 2 | |
| 8 | B1 | Data, sign bit (MSB) | |
| 9 | AB SELECT | Input and output multiplexer control. Normally connected to MJ1480 pin 16. A 'High' selects port B, 'Low' selects Port A. | |
| 10 | ENC/DEC | Select input or output amplifiers. 'Low' causes input to be selected. 'High' causes output to be selected. | |
| 11 | COMP O/P | Output of the successive approximation comparator, connects to pin 14, MJ1480. The comparator is a clocked master-slave circuit and compares the analogue input signal with the output of the D-A converter. The comparator samples the comparison on the positive clock transition and the result appears on pin 11 after the negative clock transition. The comparator output is high if the analogue input is greater than the decoded digital input. | |
| 12 | SYST CLK | System clock. 2.048MHz for 30/32 channel PCM channel bank. | |
| 13 | OVD | Digital earth | |
| 14 | OVOPA | Analogue earth | |
| 15 | ANOPA | Analogue output | Port A |
| 16 | OVOPB | Analogue earth | |
| 17 | ANOPB | Analogue output | Port B |
| 18 | OVIPA | Analogue earth | |
| 19 | ANIPA | Analogue input | Port A |
| 20 | OVIPB | Analogue earth | |
| 21 | ANIPB | Analogue input | Port B |
| 22 | OVA | Analogue earth | |
| 23 | V _{CC} | +5V ± 5% supply | |
| 24 | V _{EE} | -5V ± 5% supply | |

MJ1480

| Pin No. | Symbol | Description |
|---------|-----------------|---|
| 1 | V _{DD} | +5V ±5% supply |
| 2 | DATA I/P | Data input from PCM receive highway. Clocked by positive edge of clock. |
| 3 | DECCH CLK | Decode only channel clock input. Positive going edge on this pin causes a decode output. This input must be low if the channel clock (pin 9) is used. |
| 4 | CH CARRY | Channel carry will go high 8 system clock periods after the positive edge of a channel clock. This allows cascading of Codecs with no need for multiple channel clocks. |
| 5 | N/C | |
| 6 | N/C | |
| 7 | DATEN | A '0' on this input will allow data out onto the PCM transmit highway. A '1' will cause the output to be off. |
| 8 | N/C | |
| 9 | CHCLK | Channel clock input pin. A positive edge on pin 9 will start an encode cycle which lasts 11 system clocks. This is followed by a decode until the next channel clock. If the Decode channel clock (pin 3) is used pin 9 must be high. |
| 10 | DATA O/P | Data output onto PCM transmit highway. The output is an open drain allowing wired-OR connection to other devices. |
| 11 | MUXRES | A '1' resets AB SELECT output to 'High' (see Note 1 and timing diagram, Fig.3a), clocked on negative edge of system clock. |
| 12 | OVD | Digital earth. |
| 13 | SYST CLK | System clock, 2.048MHz for 30/32 channel PCM channel bank |
| 14 | COMP I/P | Comparator input; connect to pin 11, SL1480. |
| 15 | ENC/DEC | Encode/decode select output; connect to pin 10, SL1480. |
| 16 | AB SELECT | Port A/Port B select output; connect to pin 9, SL1480. |
| 17 | B8 | Data, sign bit (MSB) |
| 18 | B2 | Data, bit 2 |
| 19 | B3 | Data, bit 3 |
| 20 | B4 | Data, bit 4 |
| 21 | B5 | Data, bit 5 |
| 22 | B6 | Data, bit 6 |
| 23 | B7 | Data, bit 7 |
| 24 | B8 | Data, bit 8 (LSB) |

} Data output of successive approximation register (to SL1480)

NOTES

1. MUXRES will reset AB SELECT output to a 'High' when either a channel clock or a decode only channel clock is received, see timing diagram (Fig.3a).

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Ambient temperature T_{amb} = 0°C to +70°C

V_{CC} = +5V ± 5%, V_{EE} = -5V ± 5% (SL1480)

V_{DD} = +5V ± 5% (MJ1480)

SL1480

| Characteristic | Symbol | Value | | | Units | Conditions |
|---------------------------------------|-----------------|-------|------|-----------------------|-------|---|
| | | Min. | Typ. | Max. | | |
| Static | | | | | | |
| Positive supply current | I _{EE} | | 25 | 50 | mA | Pins 1-10, 12, 19-21 = 0V |
| Negative supply current | I _{CC} | | 25 | 50 | mA | " " |
| Logic '1' input voltage pins 1-10, 12 | V _{IH} | 2.0 | | V _{CC} + 0.5 | V | |
| Logic '1' input current pins 1-10, 12 | I _{IH} | | | 0.2 | mA | V _{IH} = V _{CC} |
| Logic '0' input voltage pins 1-10, 12 | V _{IL} | 0 | | 0.8 | V | |
| Logic '0' input current pins 1-10, 12 | I _{IL} | | | -0.36 | mA | V _{IL} = 0.4V |
| Logic '1' output voltage pin 11 | V _{OH} | 2.7 | | | V | I _{OH} = 50µA |
| Logic '0' output voltage pin 11 | V _{OL} | | | 0.5 | V | I _{OL} = -1.0mA |
| Analogue Inputs | | | | | | |
| Input impedance | R _{IN} | 2.4 | | 7.0 | kΩ | Input code X0000000 * |
| Input bias current | I _B | | | 0.15 | mA | Encode mode, port A or port B selected. |

MJ1480/SL1480

ELECTRICAL CHARACTERISTICS, SL1480 (CONTINUED)

| Characteristic | Symbol | Value | | | Units | Conditions |
|--|---------------------------|------------|------|------------|------------|---|
| | | Min. | Typ. | Max. | | |
| Encode offset voltage | V_{IN} | -32 | | +32 | mV | |
| Input offset current ratio | | 0.9 | | 1.1 | | |
| Temperature coefficient of ΔV_{IN} | $\frac{\Delta V_{IN}}{T}$ | | | | V/°C | |
| Temperature coeff. of input bias current | $\frac{I_B}{T}$ | | | | $\mu A/°C$ | |
| 'Crash level' | | 0.75 | | 0.85 | V | Comparator O/P = 1, code in = 11111111 |
| | | -0.75 | | -0.85 | V | Comparator O/P = 0, code in = 01111111 |
| Min. step size | $V_{step E}$ | | 0.4 | | mV | |
| 0dm0 level | | | 0.40 | | Vrms | |
| Analogue Outputs (pins 14-17) | | | | | | |
| Offset voltage (encode selected) | V_{offE} | -50 | | +50 | mV | Code in = X0000000* |
| Offset voltage (decode selected) | V_{offD} | -50 | | +50 | mV | |
| Minimum step size | $V_{step D}$ | | 0.5 | | mV | Code in = X1111111* |
| Output voltage (max. code in) | V_{OMAX} | ± 0.94 | | ± 1.03 | V | Code in = 10000000 |
| Output noise | V_{ON} | | | -88 | dBm | Decode selected Bandwidth = 1 MHz |
| Temp. Coeff. decode gain | $\frac{V_{OMA}}{T}$ | -200 | | +200 | ppm/°C | |
| Output rise time | t_r | | | | ns | Code in changed from 01111111 — 11111111 |
| Max. overshoot | V_{OV} | | | | V | |
| Output current | | | | | mA | |
| Crosstalk | | | | | | |
| Encode to Decode | V_{CED} | | | -75 | dB | Code in 1000000 analogue in 0.5Vrms at 850Hz. Port A or B in to Port A or B out |
| Encode interchannel crosstalk | V_{CEE} | | | -73 | dB | Port A = 0.50Vrms 850Hz. Port B = 0.05Vrms 2.4KHz Crosstalk measured A→B (or vice versa) |
| Decode interchannel crosstalk | V_{CDD} | | | -80 | dB | Port A = 850Hz, 0dBm0 measure Port B, or vice versa. |
| Decode/Encode crosstalk | V_{CDE} | | | -73 | dB | Port A or B output = 850Hz 0dBm0 Port A or B input 850Hz, 0.05Vrms |

MJ1480

*X specifies a 'don't care' condition

| | | | | | | |
|--|------------|-----|--|-----|---------|-------------------------|
| Static | | | | | | |
| Supply current | I_{DD} | | | 80 | mA | |
| High state output voltage, pin 4, 15-24 | V_{OHB} | 2.7 | | | V | $I_O = 50\mu A$ |
| Low state output voltage, pin 4, 15-24 | V_{OLB} | | | 0.5 | V | $I_O = -1\text{mA}$ |
| Low state output voltage, pin 10 | V_{OLA} | | | 0.5 | V | $I_O = -2\text{mA}$ |
| Offstate leakage current, pin 10 | I_{OO} | | | 5 | μA | $V_{OUT} = 2.7\text{V}$ |
| High state input voltage, all inputs | V_{IH} | 2.4 | | | V | |
| Low state input voltage, all inputs | V_{IL} | | | 0.8 | V | |
| High state input current | I_{IH} | | | 20 | μA | $V_I = 2.7\text{V}$ |
| Low state input current | I_{IL} | | | 20 | μA | $V_I = 0.4\text{V}$ |
| Dynamic | | | | | | |
| Propagation delay, clock to B1-B7, SB | t_{PSAR} | | | 150 | ns | |
| Propagation delay, clock to ENC/DEC | t_{PED} | | | 150 | ns | |
| Propagation delay, clock to AB SELECT | t_{PAB} | | | 150 | ns | |
| Delay, system clock to Data I/P | t_{DIP} | -11 | | | ns | |
| Propagation delay, channel clock to Bit 1 Data O/P | t_{PCDD} | 20 | | 130 | ns | |
| Propagation delay, system clock to Bit 2-8, Data O/P | t_{PCD} | 20 | | 270 | | |
| Propagation delay, system clock to channel carry | t_{PCCC} | 20 | | 120 | ns | |
| Set up time, system clock to MUX RES | t_{STSO} | 50 | | | ns | |
| Hold time, MUX RES | t_{HTSO} | 100 | | | ns | |
| Set up time, CH CLK to system clock | t_{SCC} | 200 | | | ns | |
| Delay time, system clock to CH CLK | t_{DCC} | 100 | | | ns | |

SL1480 and MJ1480 Combined Performance (see Fig.2)

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|-----------|-------|------|------|-------|---|
| | | Min. | Typ. | Max. | | |
| Quantising distortion Analogue-Digital | Q_{DN} | -15.3 | | | dB | $V_{IN} = -55\text{dBm0}$ $V_{IN} = -40\text{dBm0}$ $V_{IN} = -34\text{dBm0}$ $V_{IN} = -27\text{dBm0}$ $V_{IN} = -6\text{dBm0}$ |
| | | -30.3 | | | dB | |
| | | -34.4 | | | dB | |
| | | -35.6 | | | dB | |
| | | -35.6 | | | dB | |
| Digital-Analogue | | -15.3 | | | dB | $V_{OUT} = -55\text{dBm0}$ $V_{OUT} = -40\text{dBm0}$ $V_{OUT} = -34\text{dBm0}$ $V_{OUT} = -27\text{dBm0}$ $V_{OUT} = -6\text{dBm0}$ |
| | | -30.3 | | | dB | |
| | | -34.4 | | | dB | |
| | | -35.6 | | | dB | |
| | | -35.6 | | | dB | |
| Linearity | | | | | | |
| A-D noise signal | G_{HAD} | | | 0.25 | | $V_{IN} = -55\text{dBm0}$, see Fig.5 and note 1 |
| | | | | 0.50 | | $V_{IN} = -60\text{dBm0}$, see Fig.5 .. |
| A-D, 820Hz sine signal | G_{SAD} | | | 0.25 | | $V_{IN} = +3\text{dBm0}$, see Fig.6 |
| D-A noise signal | G_{NDA} | | | 0.25 | | $V_{IN} = -55\text{dBm0}$, see Fig.8 and note 2 |
| | | | | 0.50 | | $V_{IN} = -60\text{dBm0}$, see Fig.8 .. |
| D-A sine signal | G_{SDA} | | | 0.25 | | $V_{IN} = +3\text{dBm0}$, see Fig.9 |

NOTES

- V_{IN} is band-limited Pseudo-Random Noise in accordance with CCITT recommendation 0.131
- Input signal is a digital equivalent of V_{IN} (Note 1)

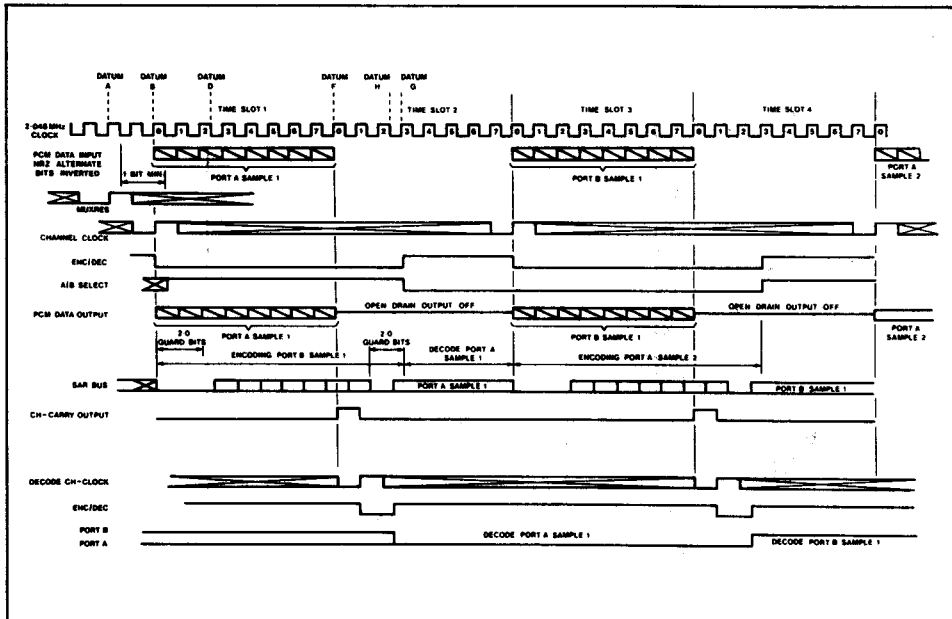


Fig.3a Codec interfacing waveforms

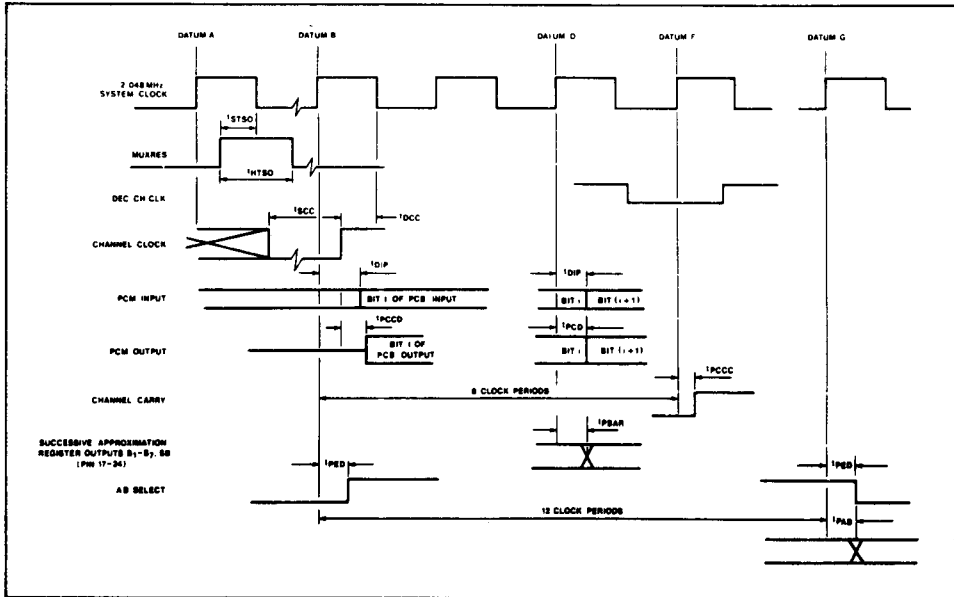


Fig.3b Codec detailed timing (all times in nanoseconds)

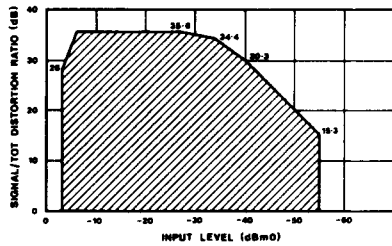


Fig.4 Quantizing distortion (encoder) as a function of input level (CCITT G712, Method 1)

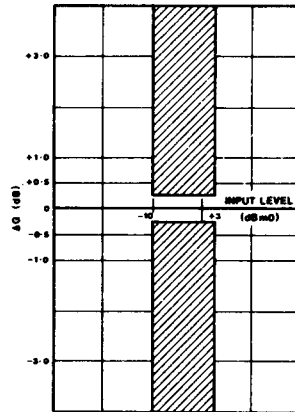


Fig.6 Variation of gain with input level (encoder) (CCITT G712, Method 1b)

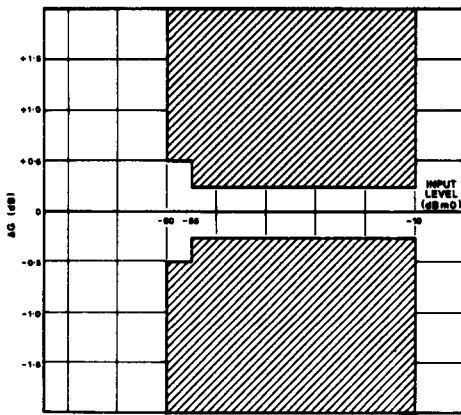


Fig.5 Variation of gain with input level (decoder) (CCITT G712, Method 1a)

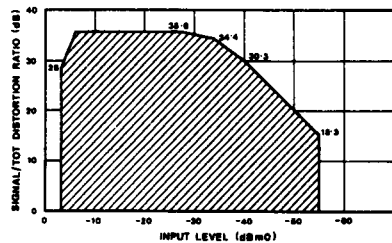


Fig.7 Quantizing distortion (decoder) as a function of output level (CCITT G712, Method 1)

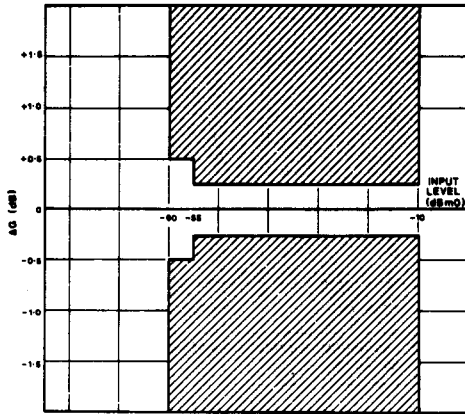


Fig.8 Variation of gain with input level (decoder) (CCITT G712, Method 1a)

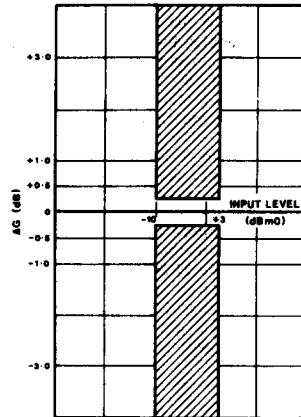


Fig.9 Variation of gain with input level (decoder) (CCITT G712, Method 1b)

APPLICATION NOTES

Input Amplifier

The input amplifier is a differential amplifier with both inputs available. Each part has a separate amplifier and input multiplexing is performed by routing the tail current to the selected input amplifier. The circuit is shown in Fig.10.

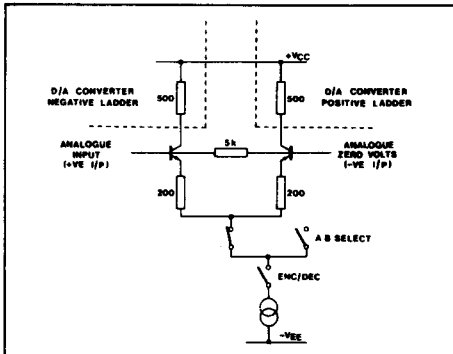


Fig.10 Input amplifier of SL1480

It is important to note that the input to the Codec is extremely broadband (Typ. 100MHz) and consequently care has to be taken to limit the noise bandwidth of the signal path leading up to the input. In addition, the impedance seen by each base of the input differential pair should be matched to reduce common mode signals (i.e. clocks etc.). Suitable configurations are shown in Figs.11a and 11b. The configuration shown in Fig.11a is only suitable for systems where each Codec input serves a single analogue channel. For applications where the signal input is derived from a multiplexer, the configuration shown in Fig.11b is more suitable as the bandwidth can be tailored for the required application.

Voltage Reference

Input and output channel gains are referenced to an internal band gap reference voltage and can be expected to be extremely stable with time and temperature. A typical regulation characteristic is shown in Fig.12.

Output Amplifier

Each output port is the output of a high performance operational amplifier selected during decode periods and

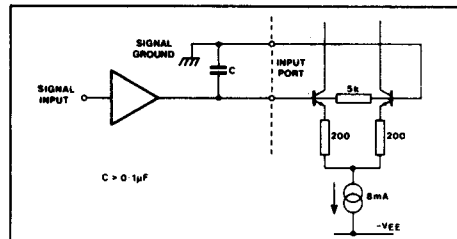


Fig.11a Input configuration for non-multiplexed applications

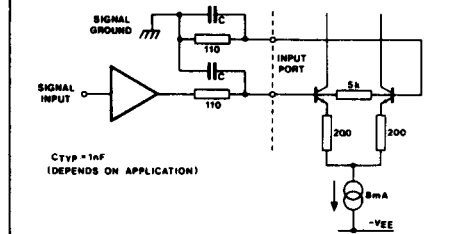


Fig.11b Input configuration for multiplexed applications

driven by the D-A converter. During encode or when the particular port is not selected the output is set to zero volts. A separate output signal earth is available for each amplifier to reduce crosstalk between channels.

Digital to Analogue Conversion

The Codec uses a successive approximation technique for encoding. The same D-A converter is used for encoding and decoding. The D-A converter is a composite structure. The 'A' law segments are selected by an R/2R resistor ladder and interpolation within each segment is performed by a group of binary weighted current sources (see Fig.13). The resistor current product formed by the converter is referenced directly to the device voltage reference ensuring excellent gain stability.

Digital Interface

The PCM interfaces to the codes are at the clock rate (2.048MHz) and are in NRZ form with alternate bits inverted. The Codec is designed to interface with a

standard 2.048M bit PCM frame and the 8 bit words associated with a particular time slot are loaded and unloaded on receipt of a channel clock. If the Codec is being used in the 'decode only' mode then the time slot immediately preceding the decode channel clock is loaded. The relationship between analogue samples and digital PCM samples is shown in Fig.3a. Encoded analogue samples are output to the PCM highway by the next channel clock and decoded analogue samples are output to the appropriate analogue port immediately following the encode cycle. The selection of ports is controlled by the MJ1480 and alternate channel clocks select port A or port B. Synchronisation of the internal multiplexer to the PCM frame is accomplished by the MUXRES input.

The PCM output is an open drain device and up to four Codecs can be connected to a PCM highway and still allow a load equivalent to two low power Schottky loads to be driven. The output of a Codec is only active when data is

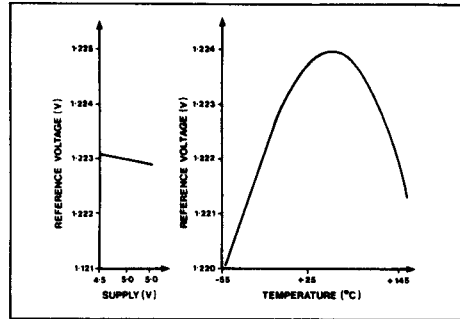


Fig.12 Regulation characteristics of the SL1480 voltage reference

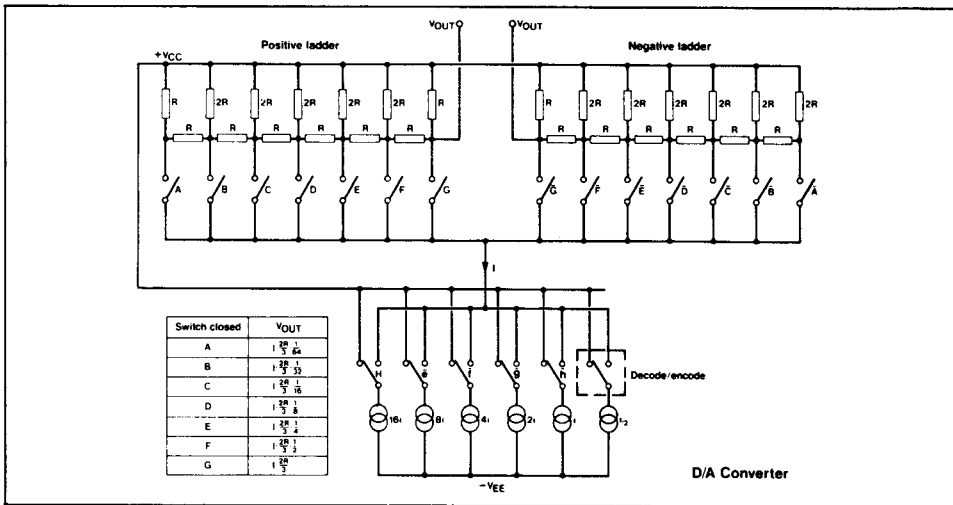


Fig.13 D-A converter for the SL1480

being output; at all other times the output is open circuit. There is a data enable (DATEN) input to the Codec which allows a particular Codec to be disabled on a static or dynamic basis thus allowing concentration on a line-by-line basis to be performed in Subscriber Line Interface Circuit (SLIC)

An Eight Line Subscriber Interface

The circuit shown in Fig.14 is an eight analogue line system using the SL1480 + MJ1480 as an 'A' law Codec.

Filtering

Three technologies are recognised for antialias filtering the analogue input signal. This circuit uses active filters although LC or switched capacitor filters could be used (with appropriate gain adjustments). A significant problem with active filters is their relatively high broadband noise level. Consequently, to improve dynamic range the signal level at the filter output has been set at approximately +15dBm0 (relative to the Codec input). Noise in the output filter is not such a severe problem as broadband noise is not a significant performance hazard.

The particular filters used are a combination of thin film substrates and gain blocks provided by Plessey TAB1042 quad programmable operational amplifiers.

A similar system using 2912 type switched capacitor PCM filter has been developed. Full information is available from Plessey Semiconductors.

Multiplexing

Industry standard 1 to 8 multiplexers are used in this application. The internal multiplexer of the Codec is not used as to do so would necessitate a more complex multiplexing scheme with four 1 to 4 multiplexers being required. The selected multiplexers have adequate switching speed to cope with the system. A further advantage of this configuration is that it could be expanded to 16 channels by duplicating the analogue path and using the other Codec port. The address waveforms required by the multiplexers are shown in Fig.15.

Offset and Gain Adjust

The variable ON resistance of the multiplexer, coupled with the 5kΩ input impedance of the Codec mean that a buffer is required to prevent gain variations outside the required specification. This buffer also allows input offset adjustment by means of a preset resistor (or an autozero circuit if preferred). The buffer is preceded by an attenuator to reduce the relatively high signal level in the filter to that suitable for the Codec.

The bandwidth of this section should be limited to the minimum possible consistent with response times required by the multiplexed input. Bandwidth is controlled by R11, C9 and in practice full advantage cannot be taken of this bandwidth as linearity at low levels deteriorates slightly for larger values of C8 and C9. A compromise between linearity and signal-to-noise ratio can be reached as the performance curves of Figs.16a and 16b show:

PARTS LIST FOR FIG. 14

| INTEGRATED CIRCUITS | | | |
|---------------------|---------------------|---------------|--------------|
| REF. NO. | FUNCTION | PART NO. | MANUFACTURER |
| IC1* IC2* IC3* IC8* | Op. Amp. | TAB 1042 | Plessey |
| IC9* IC10* IC11* | Op. Amp. | TAB 1042 | Plessey |
| IC5 IC7 | Mux | MUX08, IH6108 | PMI Intersil |
| IC6 | Op. Amp. | NE5534 | Mullard |
| IC12 | CMOS dual D-type FF | 4013 | Any |
| IC13 | CMOS 4 bit counter | 40163 | Any |
| IC14 | CMOS Quad Nor gate | 4001 | Any |
| IC4 | Transmit filter | S42026-A15-A3 | Siemens |
| IC15 | Receive filter | S42026-A15-A1 | Siemens |

| RESISTORS | | CAPACITORS | |
|-----------|-----------|------------|--------------|
| R1* 620Ω | R10 2.0kΩ | C1* | 0.01μF ± 20% |
| R2* 30kΩ | R11 110kΩ | C2* | 0.1μF ± 3% |
| R3* 30kΩ | R12 110kΩ | C3* | 0.1μF ± 3% |
| R4* 54kΩ | R13 2.0kΩ | C4* | 0.68μF ± 10% |
| R5* 54kΩ | R14 1.8kΩ | C5 | 10pF ± 20% |
| R6* 2.4kΩ | R15* 41Ω | C6 | 1μF ± 10% |
| R7* 2.2kΩ | R16* 17kΩ | C7 | 22pF ± 20% |
| R8* 9.1kΩ | R17* 33kΩ | C8 | 1nF ± 10% |
| R9 2.2kΩ | VR1 500Ω | C9 | 1nF ± 10% |

* These components are required for each analogue channel.
 TAB1042s used for IC1, 2, 3 should be biased with 7.5μA.
 TAB1042s used for IC8, 9, 10, 11 should be biased with 75μA.

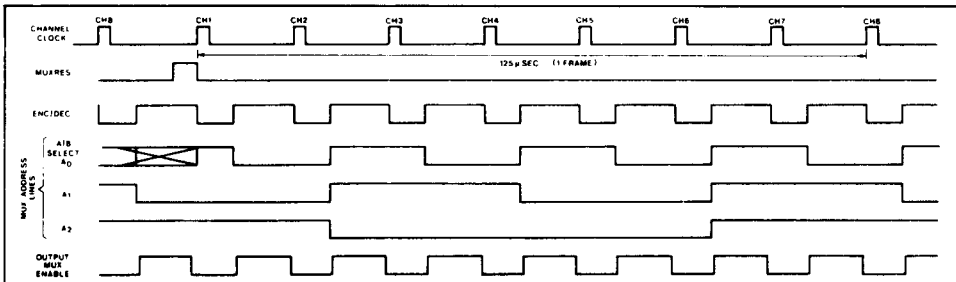


Fig.15a Multiplexer waveforms for an 8-channel multiplexed board

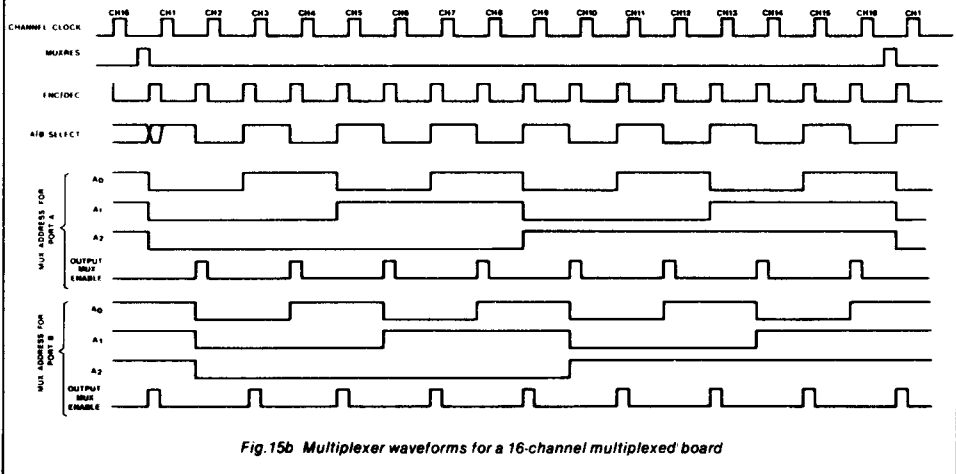


Fig.15b Multiplexer waveforms for a 16-channel multiplexed board

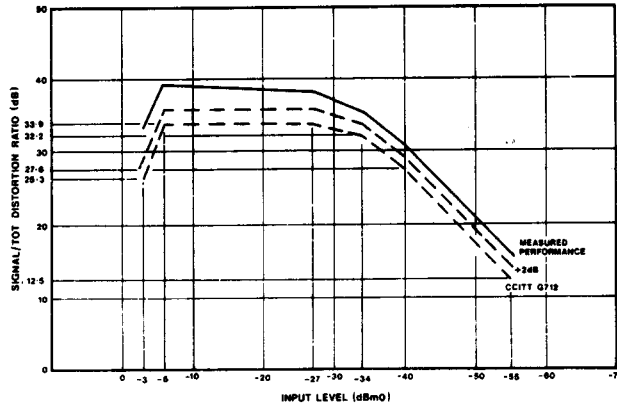


Fig.16a Encode Q_p measurements, multiplexed board (noise source)

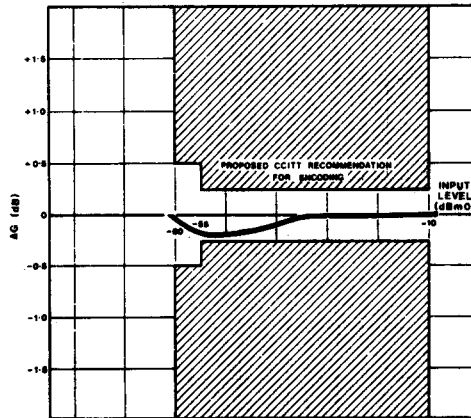


Fig.16b Encode linearity of multiplexed board (noise source)

Bandwidth Calculation

From Fig.15, the multiplexer address waveforms, we can see that the total period available to switch channels through the input multiplexer to the Codec input is 2.5 time slots (20 clock periods or 9.76µs). There is a delay to turn on the multiplexer, consisting of an address generation time, t_{add} , and a multiplexer turn on time, t_{onmux} , which must be subtracted from the 2.5 time slots before the bandwidth of input buffer can be calculated.

$$t_{add} = t_{pAB} \text{ (clock to AB sel)} + 2t_{ps} \text{ (clock to Q for IC 12)} = (150 + 2 \times 250) \text{ ns}$$

$$t_{onmux} = 2.1 \mu\text{s (PMI MUX08B)}$$

The first bit to be set during the A/D conversion process is the sign bit and the worst case deviation for this decision is from full scale to zero. For accurate sign bit determination the input must be accurate to within ½ LSB. It is assumed that the single time constant ($R_n C_s = \gamma$) controls the response time.

Full scale for an 'A' law codec = 2048 LSB steps.

$$\text{now } V = V_{in} (1 - e^{-t/\gamma}) \quad \dots (1)$$

$V =$ output voltage
 $V_{in} =$ input voltage
 $\gamma =$ time constant (i.e. $R_n \times C_s$)
 $t =$ response time
 $V = (2048 - \frac{1}{2})$ units
 $V_{in} = 2048$ units
 $t = (9.76 - 0.65 - 2.1) \mu\text{s}$ (see above)

equation (1) gives $\gamma = 843$ ns and using $R_n = 110\Omega$ gives a value for C_s of 7.67 nF. However, the use of C_s with a capacitance of this magnitude causes linearity problems and a satisfactory compromising value for C_s is 1nF.

Output Multiplexing

The output analogue signal path is considerably simpler than the input signal path and consists of the multiplexer and the output filter. Addressing for the output multiplexer

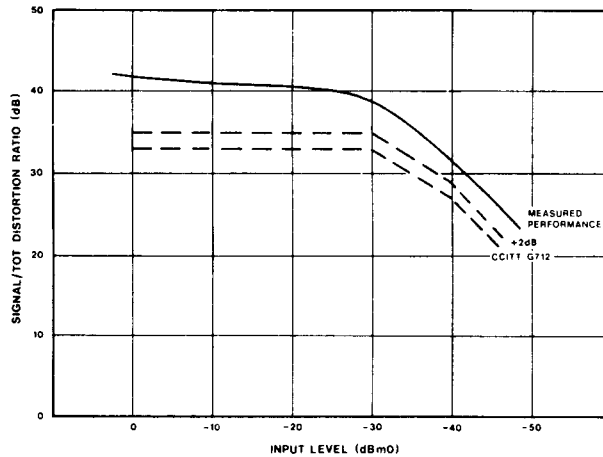


Fig. 17a Decode Q_D measurements, multiplexed board (sine wave input)

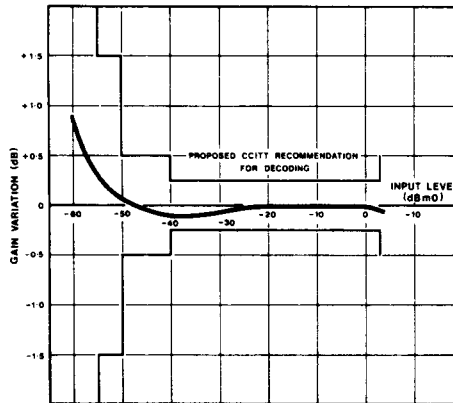


Fig. 17b Decode linearity of multiplexed board (sine wave input)

is identical with that of the input multiplexer. However, it is important that the filter only samples the Codec PAM output when it is at its decoded analogue level. To achieve this an additional enable pulse is derived by IC13 and 14. The precise length of this pulse is not important but variations in its period will cause gain variations and channel clock jitter will cause additional noise on the recovered analogue signal.

The performance of the output channel is shown in Figs. 17a and 17b.

Extension to 16 channels

This system could be extended to 16 channels merely by using both ports of the CODEC and duplicating the analogue signal paths. Multiplex addressing would be slightly more complex and the required waveforms are also shown in Fig. 16.

An Asynchronous 30 channel PCM terminal for Transmission Equipment

PCM transmission equipment differs from SLIC applications in that the digital send and receive highways are asynchronous. A block diagram of a suitable system is shown in Fig. 18. The encode part of the system consists of

two Codecs configured to serve 16 channels each, as in the SLIC example. In fact only 15 analogue channels are required as time slots zero and 16 are used for signalling.

Since the incoming and outgoing PCM streams are asynchronous a separate Codec is required for digital to analogue conversion. In this case the channel clock input (CHCLK) to the Codec is held high and the decode channel clock (DECCHCLK) is driven. This allows the Codec to decode the full 32 time slots (although only 30 would be used).

Synchronisation and data access to time slot zero and sixteen data bits can be provided by the MJ1444, MJ1445 and MJ1446 and conversion of the resulting 2.048M bit data stream to HDB3 or AML ternary codes can be accomplished by the MJ1440 or MJ1471.

Conclusion

The Codec (SL1480 + MJ1480) is a flexible system which can be incorporated into both PCM transmission equipment and digital exchange subscriber interface circuits. In both applications it can provide considerable economies in both device count and cost while satisfying all the relevant CCITT performance specifications.

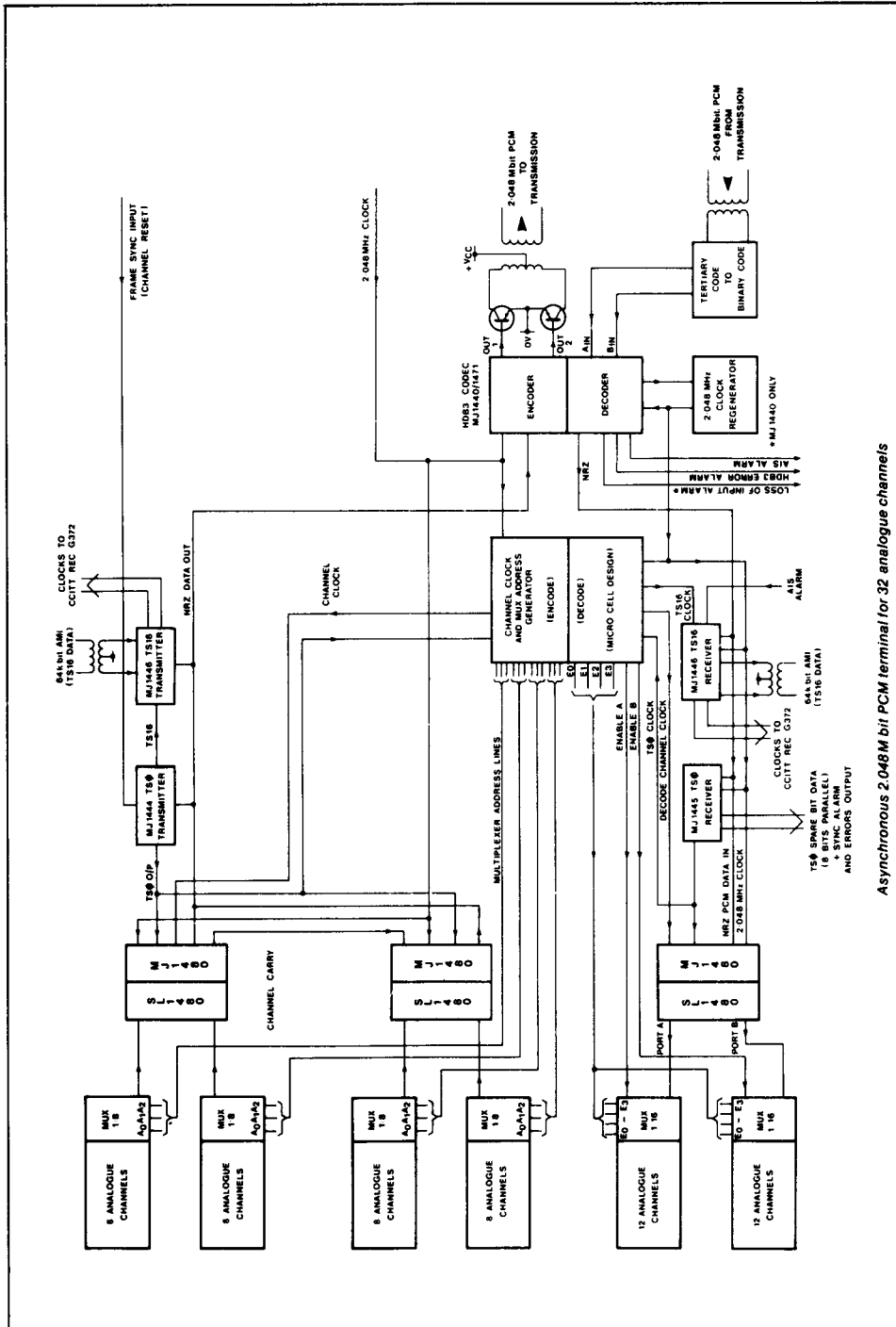


Fig. 18 Asynchronous 2.048M bit PCM terminal for 32 analogue channels

Asynchronous 2.048M bit PCM terminal for 32 analogue channels