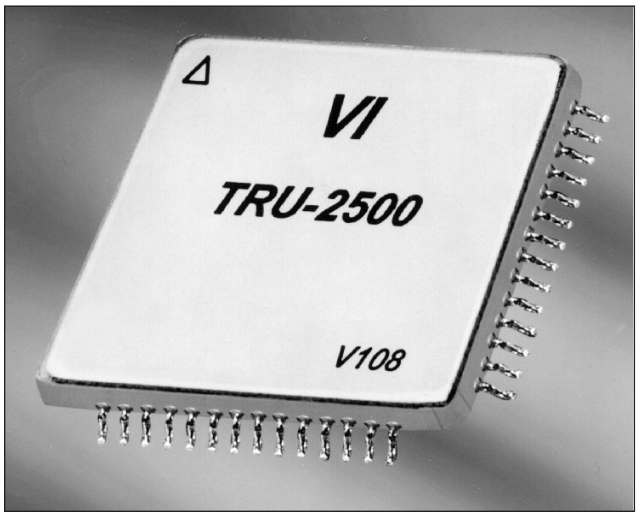
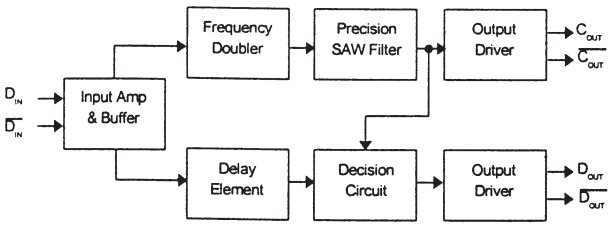
VECTRON INTERNATIONAL
A DOVER TECHNOLOGIES COMPANY

Product Data Sheet

TRU-2500

2.488 Gb/s SAW Filter Clock Recovery and Data Retiming Module





Simplified Block Diagram

Features

- **Clock Recovery and Data Retiming for 2.488 Gb/s**
- **SAW Filter Timing Recovery**
- **Commercial or Industrial Temperature Range**
- **Compliance with SONET, OC-48 / SDH, STM-16**
- **Single -5V Power Supply**
- **Differential ECL/PECL Compatible Input/Outputs**
- **50VCML Outputs**
- **<2 ps RMS Typical Output Clock Jitter**

Applications

- **SONET OC-48 / SDH STM-16**
- **DWDM Optical Networks**
- **SONET/SDH Test Equipment**
- **Submarine Transmission Links**

Description

The TRU-2500 is the latest addition to Vectron International s family of high performance timing recovery units. It extends the highly respected TRU-600 circuit topology to 2.5 Gb/s data rates with performance optimized to exceed the most stringent SONET/SDH transmission standards.

VI s TRU-2500 regenerates clean clock and data signals from an incoming 2.488 Gb/s non-return to zero (NRZ) data stream. The device utilizes SAW filter clock recovery technology for superior jitter tolerance, jitter transfer and jitter generation performance, independent of the data pattern transition density. Output clock jitter is exceptionally low at typically less than 2.0 ps RMS.

The clock is extracted from the NRZ data stream by first passing it through a frequency doubler to generate spectral energy at 2.488 GHz. A precision narrow-band SAW filter extracts the clock and eliminates unwanted jitter. The resulting clock is then precisely aligned at the decision circuit to retime the input data.

Theory of Operation

The TRU2500 combines Vectron s SAW filter expertise with custom GaAs ASIC technology for high performance timing recovery applications. The circuit is assembled on a precision ceramic hybrid and packaged in a hermetic SMD package with industry common footprint and pinout. Precision SAW filter technology assures full Bellcore compliance over all operating conditions and eliminates the need for external tuning or compensation.

High bit-rate SAW filter clock recovery was developed for and has been proven in high reliability undersea links. The timing recovery circuit must extract a clean clock signal from an input NRZ data stream and then reclock the data with the clock. A simplified block diagram of a basic timing recovery circuit is shown in Fig 1.The data retiming aspect of the design is somewhat straightforward. Recovering a clock compliant with jitter standards and maintaining acceptable clock to data alignment at the decision circuit are the most difficult aspect of the design. It is this aspect of the design which VI has mastered through many years of experience.

The clock recovery process can be viewed as a bandpass filter operation, accomplished either through a SAW filter or through the composite effect of a closed loop system (PLL). Most clock recovery devices employ a phase lock loop architecture, which employs a phase detector and loop amplifier to lock a free running VCO to the input signal. At lower data rates PLL designs provide acceptable performance, but as data rate increase, the ability to control critical loop gain parameters over environmental extremes becomes exceedingly difficult.

The accuracy and stability of the bandpass characteristic determines how effectively the process will comply with stringent SONET/SDH jitter requirements. The TRU2500 offers superior jitter transfer, jitter tolerance and jitter generation performance because its bandpass characteristic is prescribed by a precision quartz SAW filter which can be precisely controlled and accurately reproduced in volume production.

The circuit architecture of the clock recovery path is shown in Figure 2. Figure 3. illustrates the time domain waveform and its associated frequency domain spectrum at various points in the path. Since the input NRZ data stream (A) has a null at the clock frequency, non-linear processing of the signal is required to generate spectral content at the clock rate. The circuit uses a microstrip line to delay the data 1/2 of a bit period. The data and delayed data are then fed through an exclusive or-gate to produce a pulse at each data transition. This signal then has a strong spectral peak at the desired clock rate (B) and can be viewed in the time domain as a clock signal with missing pulses. The pulse train is then filtered and shaped prior to the SAW filter to provide optimum performance. The SAW filters this signal to provide a continuous sine wave (C) with compliant jitter characteristics. This signal is amplified and becomes both the output clock and the retiming signal for the decision circuit.

Due to careful attention to pre-filtering and shaping, SAW filter bandpass characteristics, and the elimination of feedback loop clock to data alignment control, the TRU2500 is able to offer output jitter performance as low as 2psRMS, a level not achieved by phase locked loop designs.

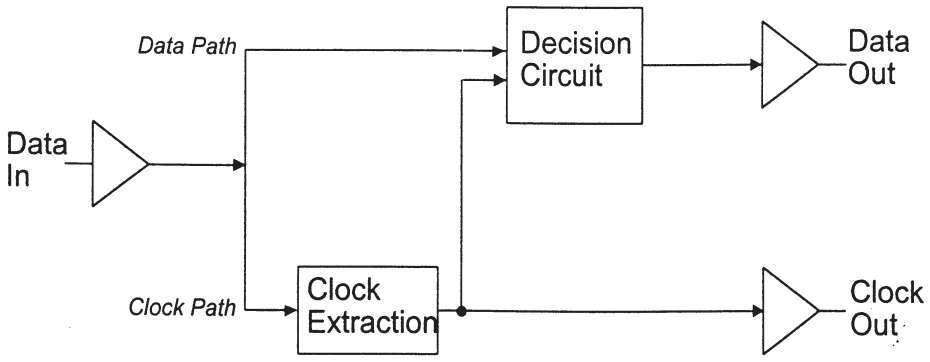


Figure 1. Simplified TRU2500 Block Diagram

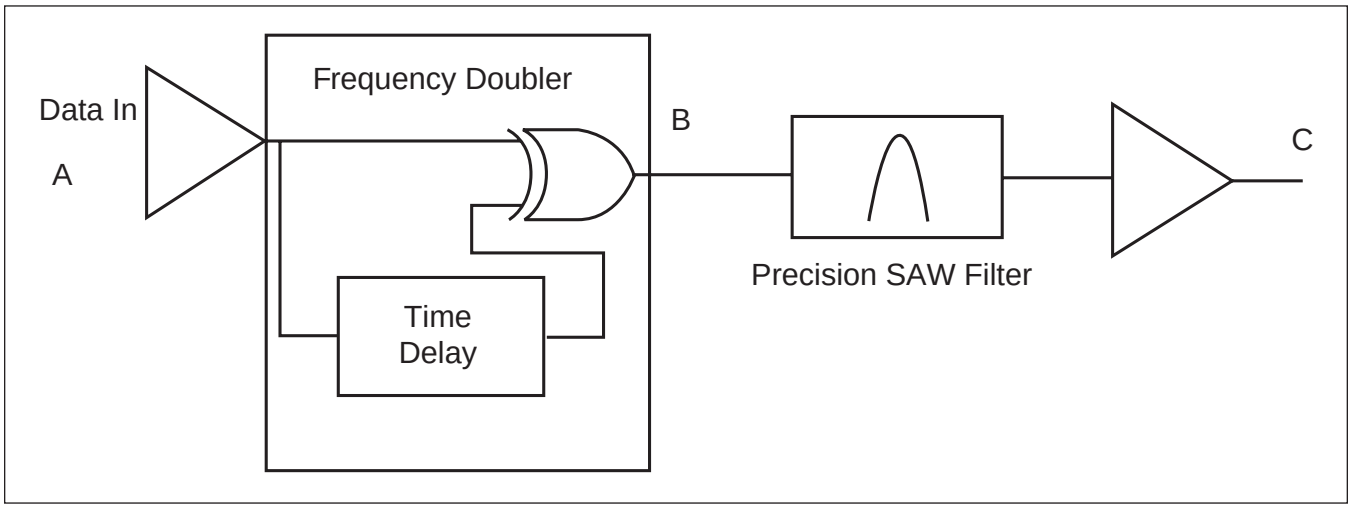


Figure 2. Clock Extraction Path

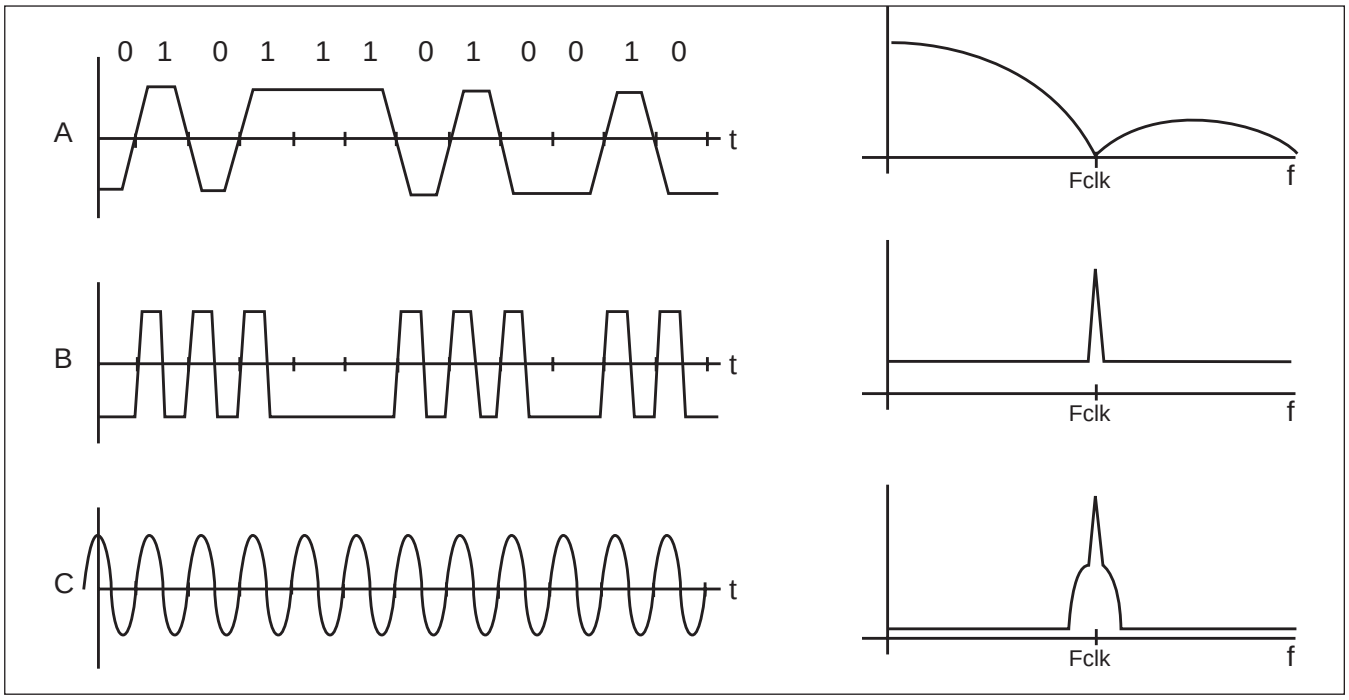


Figure 3. Signals in Clock Recovery Path

Accurate alignment of the clock within the data eye is required for error free data retiming in the presence of noise. The TRU-2500 uses a programmed delay line to achieve exceptional clock to data alignment. The delay is set at the factory to ensure generous margin for system specifications over a wide power supply and temperature range for the lifetime of the product. The decision circuit also includes CML clock and data output buffers with 50 Ohm internal matching for easy interface.

Performance Characteristics

Absolute Maximum Ratings

Absolute maximum ratings are worst case and short duration exposure conditions. Exposure to conditions more severe may result in permanent damage. Exposure for extended periods may also affect device performance or reliability. Functional operation of the device is not implied at these conditions.

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Supply Voltage Range	V_{SS}	-7	+0.5	V
Loss of Signal Bias Voltage	V_{DD}	-	7	V
Power Dissipation		-	2	W
Data Output Voltage		V_{SS}	+0.5	V
Operating Temperature Range	T_{OP}	-40	85	°C
Storage Temperature Range	T_S	-40	125	°C

Electrical Characteristics

Maximum and minimum values are testing requirements. Typical values are characteristics of the device and are result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Table 2. Electrical Characteristics (Operating Temperature Range, $\leq 10^{-9}$, 23^{23} -1 NRZ PRBW

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply Voltage	V_{SS}	-4.75	-	-5.25	V
Supply Current	I_{SS}	-	-	475	mA
Data Input Sensitivity (Differential)	DATAIN	100	-	900	mV_{pp}
Data Output Voltage	DATAOUT	625	800	-	mV_{pp}
Clock Output Voltage	CLKOUT	625	800	-	mV_{pp}
Clock/Data Output Rise/Fall Time (20/80%)	$T_{R/F}$	-	70	-	ps
LOS Output Signal, Low	V_{LOSL}	-1	-	0.5	V
LOS Output Signal, High	V_{LOSH}	V_{DD}-0.5	-	V_{DD}	V
Jitter Tolerance	J_{TOL}	Compliant with SONET/SDH Requirements			UI
Jitter Transfer Break Point	J_{BW}	-	-	2	MHz
Jitter Generation	J_{GEN}	-	2	3	ps
Output Clock Duty Cycle	D	45	50	55	%
Acquisition Time	T_{AQ}	-	350	500	ns
Clock to Data Alignment (Figure 4)	T_{CDA}	-	40	-	ps

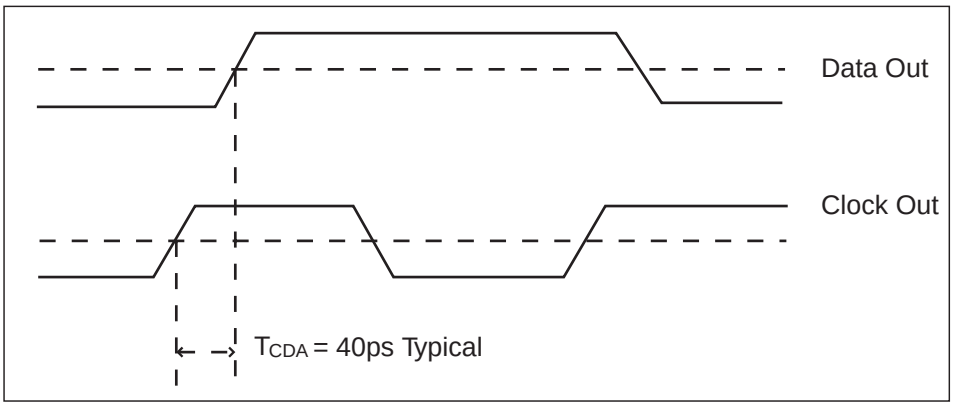
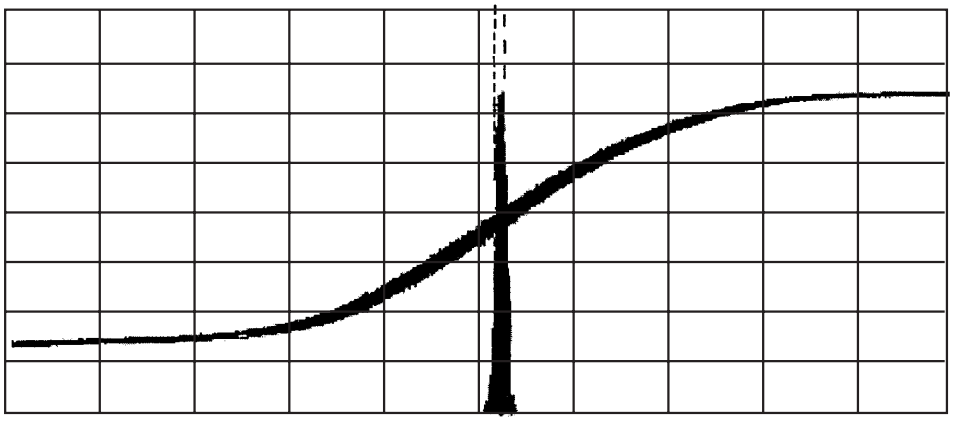


Figure 4. TRU2500 Clock to Data Alignment

Jitter Performance

SONET/ SDH standards specify jitter generation, jitter tolerance, and jitter transfer requirements for receiver and clock recovery elements. Jitter generation (see figure 5.) is minimized through careful design of the clock recovery path to minimize pattern dependent noise on the output clock. Jitter transfer and tolerance performance result from optimization of the SAW filter bandpass characteristics. The SAW filter in the TRU-2500 was specifically designed for clock recovery. It exhibits excellent control of the passband response and eliminates inband ripple. The filter is individually housed in a ceramic package and is measured for insertion loss, phase, and bandwidth. A typical response is shown in Fig 6.



Ch. 2	= 157.0 mVolts/div	Offset	= -411.3 mVolts
Timebase	= 20.0 ps/div	Delta Window	= 9.8125 mVolts
Window 1	= -441.56 mVolts	Delta T	= 2.0 ps
# Samples	= 1024	Sigma	= 1.0 ps

Figure 5. TRU2500 Jitter Generation

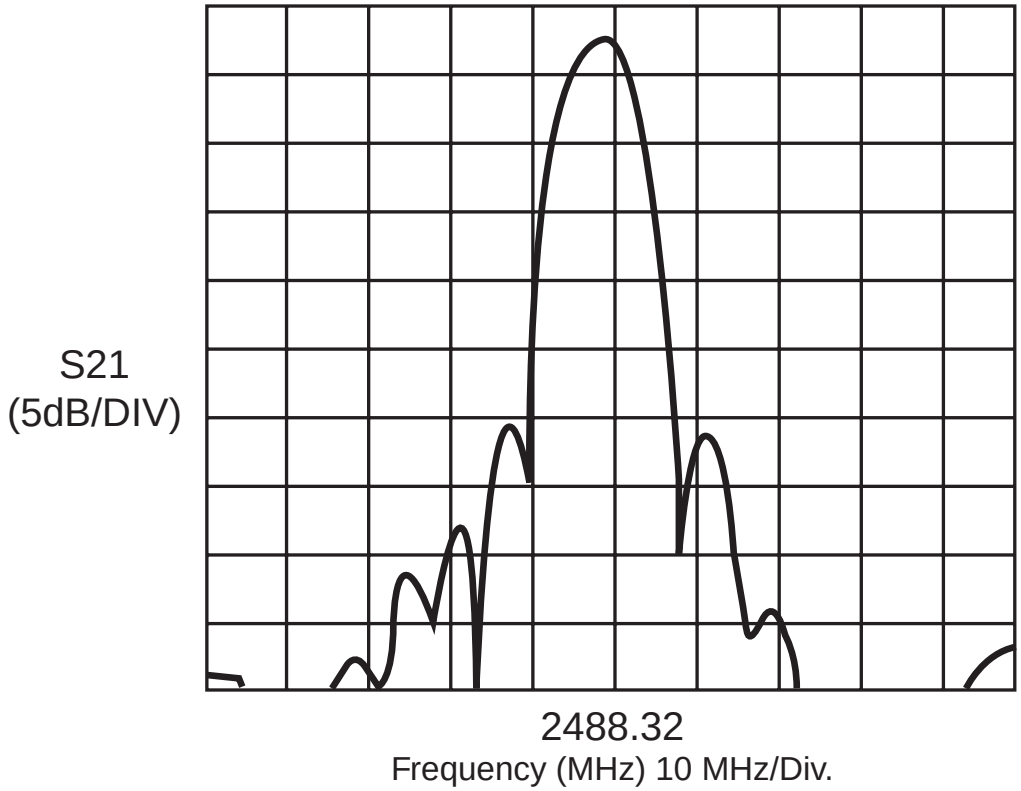


Figure 6. TRU2500 SAW Filter Response

Optimized jitter transfer and tolerance performance is dependent upon precise control of the filter bandwidth. The jitter transfer function is a baseband measurement of the SAW filter, or the loop filter bandwidth for a PLL device. The specifications form a jitter mask which limits inband jitter peaking to less than 0.01 UI and at 2MHz. The mask then rolls off at 20 dB/dec. Figure 7 shows the jitter transfer function for the TRU-2500 at 25°C, -40°C, and +85°C.The responses show a complete absence of jitter peaking and virtually optimum bandwidth with negligible temperature variation.

The jitter tolerance mask and the TRU2500 test results are shown in figure 8. At the high frequency portion of the mask, the device must run essentially error free with 0.15 UI additional sinusoidal modulation on the input data. As the modulation frequency is decreased approaching the filter bandwidth, jitter tolerance rises as the recovered clock starts to track the modulation. The breakpoint frequency for this rise in tolerance is approximately 1 MHz, this places a lower limit on the clock recovery filter bandwidth. The combined jitter tolerance and jitter transfer requirements restrict the filter bandwidth to the 1 to 2 MHz range, over all conditions. The TRU2500 typically maintains better than 0.5UI tolerance at high frequencies, due to the SAW filter response. This is virtually impossible for a PLL to meet at high data rates.

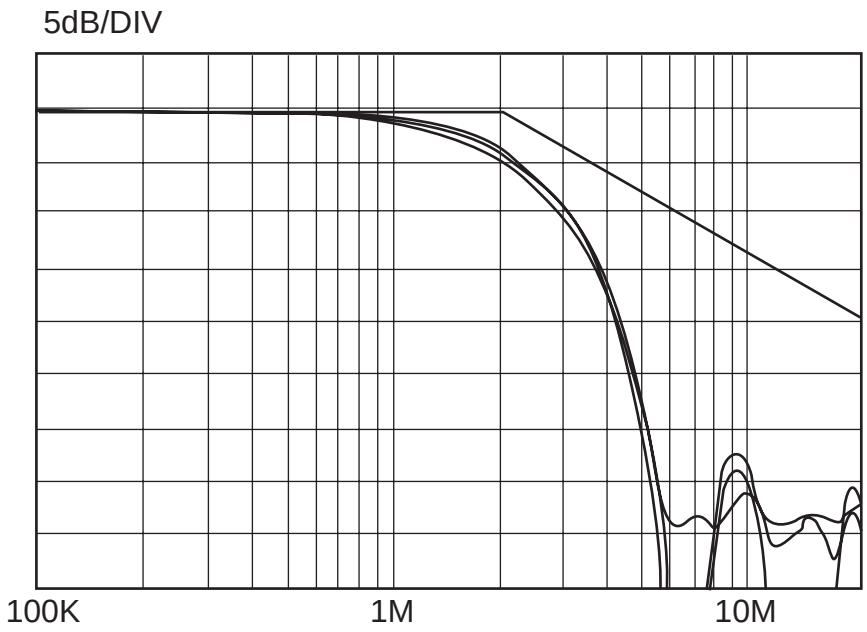


Figure 7. TRU2500 Jitter Transfer

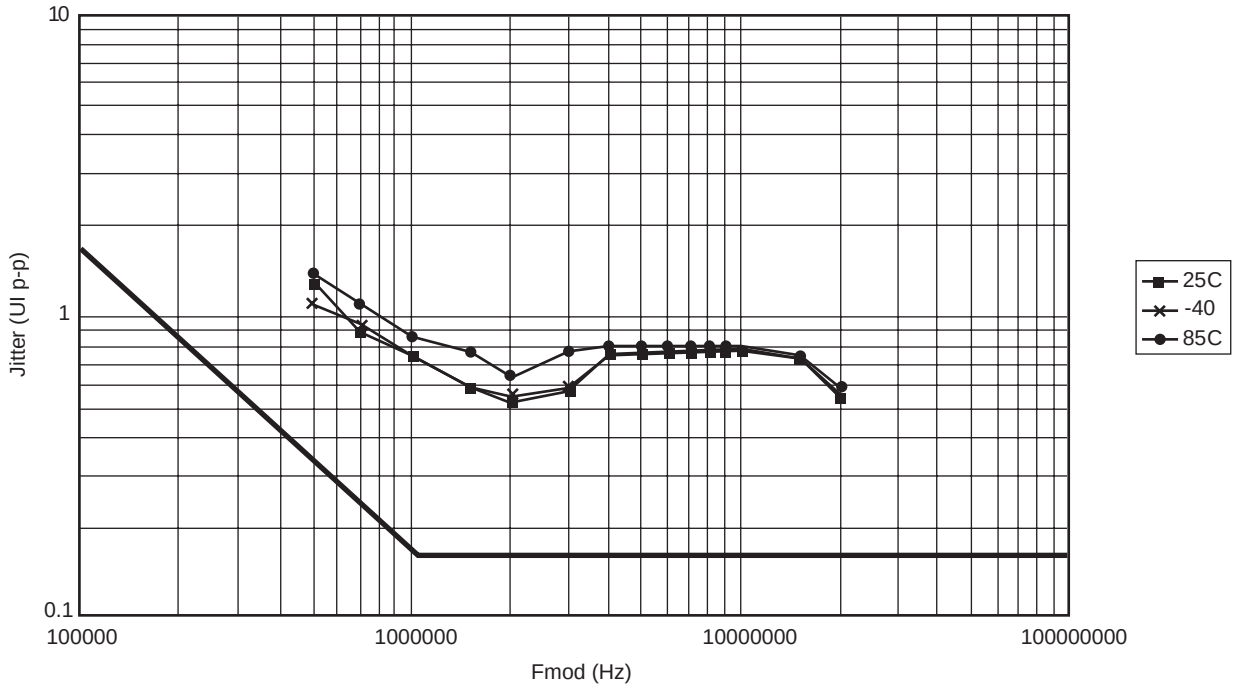


Figure 8. TRU2500 Jitter Tolerance

TRU-2500: Clock Acquisition Time ("Input Blanking")

Several parameters may be measured on a clock recovery device to characterize its response to initial start up and transient input data bursts. In conventional Phase Locked Loop designs an internal VCO functions as a clock source which must be synchronized by the loop to the input data rate. The time needed to synchronize the internal clock and provide error free data retiming after a long period without input data transitions is the acquisition time. The response time to shorter time intervals with no data transitions is sometimes referred to input blanking. A third measure of the retiming function is the maximum run length of ones or zeros with no errors.

A clock recovery device will provide error free performance up to a specified maximum number of consecutive ones or zeros. In a PLL design, synchronization is lost briefly and errors occur for a short interval until synchronization is reestablished. As the run length increases the PLL drifts further from lock and the error interval becomes longer. Eventually a limit is reached where the device is starting from a maximum frequency offset and the recovery time is the acquisition time. A PLL will output a frequency with considerable error with no data input.

Passive filter based clock recovery depends on the selectivity or Q of the filter along with the gain of associated amplifiers to build up a clock signal derived directly from the input data. Evaluation of the TRU-2500 shows that the clock signal reaches full amplitude in about 350ns with a random data input. Further evaluation shows that error free data is available at the output after a 250ns interval, less than 1000 data transitions. This interval may be shortened through the use of a preamble. This acquisition time is three orders of magnitude shorter than a comparable PLL based design. A plot comparing the recovery time for input blanking is shown in figure 9.

The SAW filter based TRU-2500 also provides a stable output clock for a comparable time period of at least 250ns after input data is stopped. 250ns correspond to 625 bit intervals at 2.5Gbit/s. Evaluation shows the typical TRU-2500 can run error free with up to 650 zeros or ones imbedded in a 2e13 random data pattern.

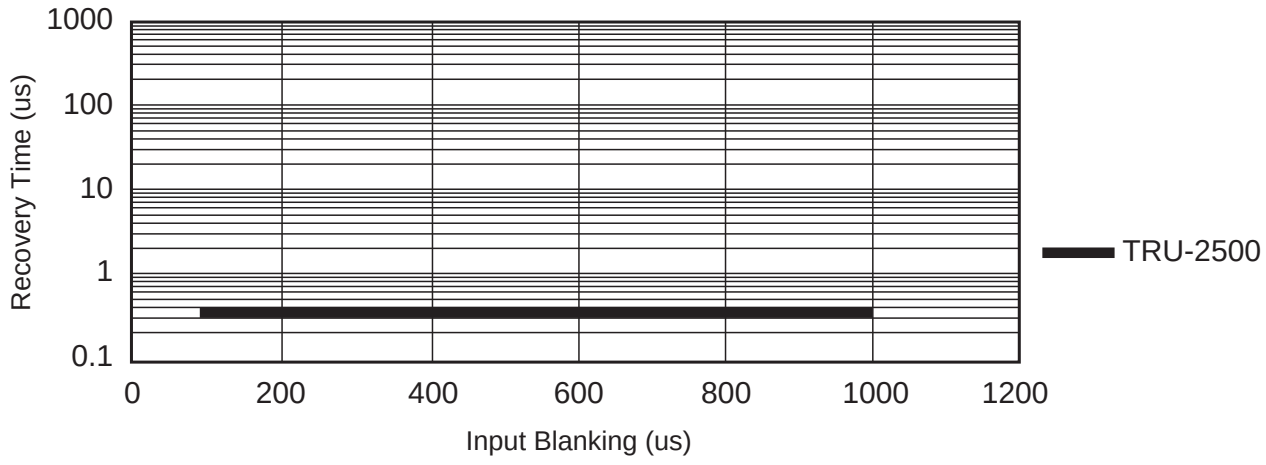


Figure 9. Error Recovery Time vs Input Blanking

Pinout Information

The Pinout for the TRU2500 is shown in figure 10

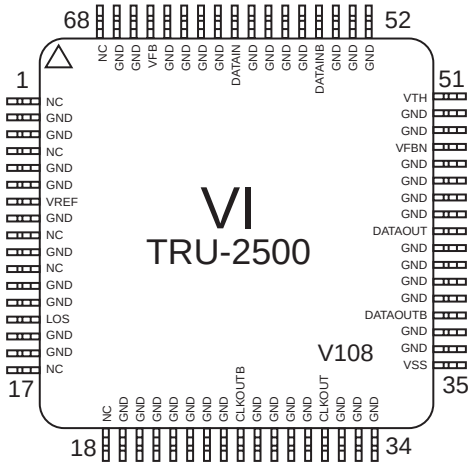


Figure 10. Pin Diagram

Table 3. Pin Description

Pin	Symbol	Name/Function
7	V_{REF}	Reference Voltage (Nominally-3.2V)
14	LOS	Loss of Signal
26	$\overline{CLKOUT}$	Recovered Clock Out (-). Terminate into 50V to GND
31	CLKOUT	Recovered Clock Out (+). Terminate into 50V to GND
35	V_{SS}	Supply Voltage (-5.0 V) Nominal
38	$\overline{DATAOUT}$	Regenerated Data Out (-) Terminate into 50V to GND
43	DATAOUT	Regenerated Data Out (+) Terminate into 50V to GND
48	$\overline{V_{FB}}$	DC Feedback Voltage (-), Not Used
51	V_{TH}	Input Threshold Voltage, (Not Typically Used)
55	$\overline{DATAIN}$	Data Input (-) Internally AC coupled
60	DATAIN	Data Input (+) Internally AC coupled
65	V_{FB}	DC Feedback Voltage (+), Use to Adjust Decision Threshold (Not Typically Used)
1,4,9,11, 17,18,68	NC	No Internal Connection
2,3,5,6,8 10,12,13,15 16,19,20,21 22,23,24,25, 27,28,29,30, 32,33,34,36, 37,39,40,41, 42,44,45,46, 47,49,50,52, 53,54,56,57, 58,59,61,62, 63,64,66,67, Case	GND	Case Ground

Circuit Layout Considerations

Power Supply and Grounding:
The TRU-2500 is designed for optimum performance with a -5 Volt supply. Good high speed grounding and layout practice should be employed to assure acceptable performance at this high a data rate. The device temperature rating is specified as the case temperature. Consequently good thermal grounding will increase the useful ambient temperature capability of the device.

Input configuration:
Data inputs are differential with internal AC coupling to a 50 Ohm termination. This allows a simple interface to a variety of drive circuits, including single ended inputs.

The TRU2500 design makes use of GaAs HBT technology to realize lower input offset levels than is achievable with other FET designs. The extremely low offset allows the device to operate without bias feedback and results in typical input sensitivities as low as 60 mV. Since feedback is not used, it is not necessary to connect $\overline{V_{TH}}$ to $\overline{V_{FB}}$. Since $\overline{V_{FB}}$ has no internal connection, $\overline{V_{TH}}$ and $\overline{V_{FB}}$ may be connected with no ill effect.

The bias point for each input is accessible through the $\overline{V_{TH}}$ and V_{FB} pins through 1kV resistors. Input offset levels can be adjusted by applying a 0V to -1V bias, to either or both of the V_{FB} and $\overline{V_{TH}}$ pins. This could be accomplished by individually tying the either or both of the inputs to -5 V through large variable (100kV) resistors. This could be used to optimize the switching threshold for a particular system or application.

Output Configuration:
The differential outputs for clock and data are 50V CML, as shown in Figure 12. This design has true 50V output impedance for optimum reflection coefficient and reduced sensitivity to variation in interconnect and downstream terminations. The CML output can interface directly to devices with CML inputs, 50 Ohm to ground, or may be AC coupled to interface with ECL, PECL.

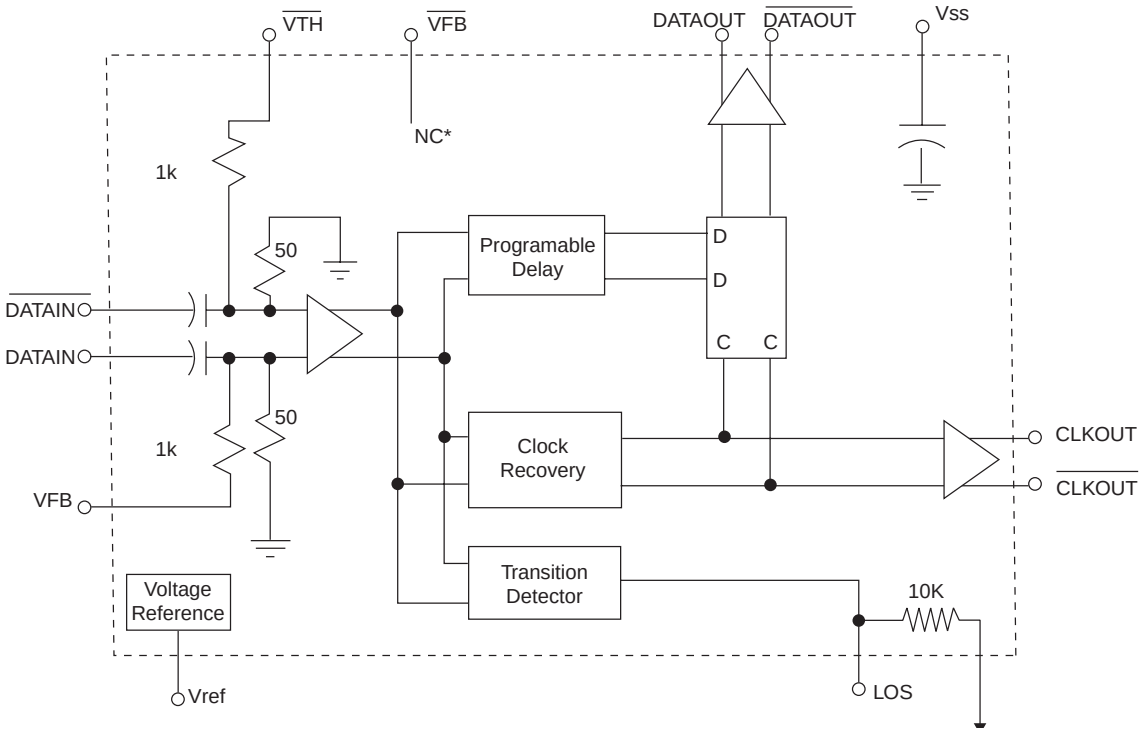


Figure 11. TRU2500 Block Diagram

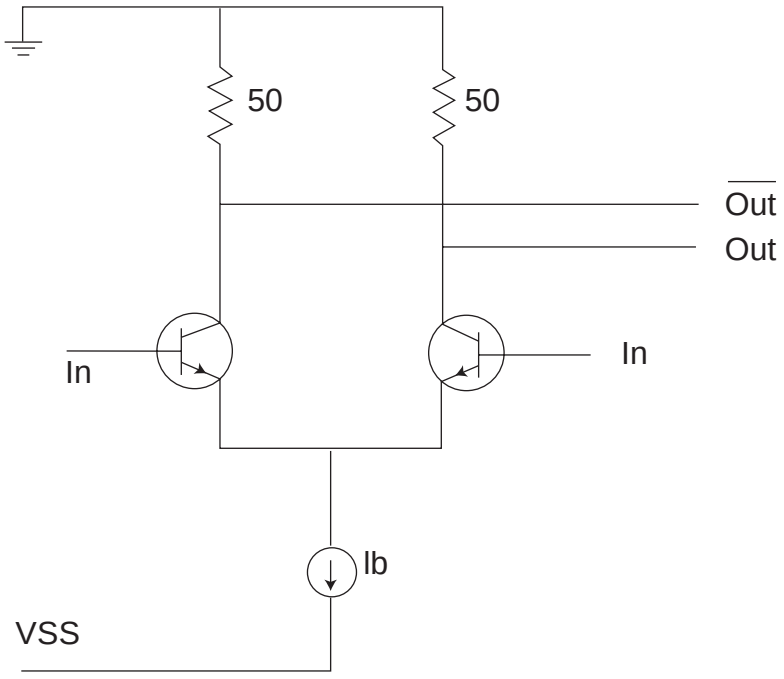


Figure 12. CML Output Configuration

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. VI employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the mode.

Although no industry-wide standard has been adopted for the CDM, a standard HBM (resistance = 1500V, capacitance = 100pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Table 4. ESD Threshold Voltage

Model	Threshold	Unit
Human-Body (HBM)	500*	V min.
Charged-Device	200	V min.

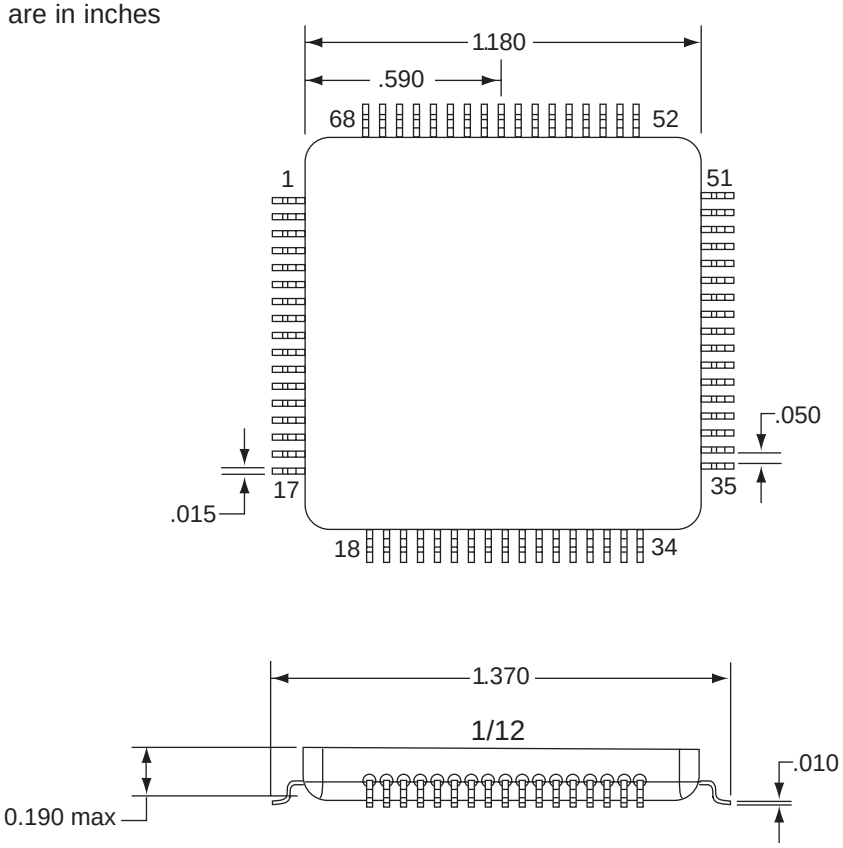
* Mil-STD-883D, Method 3015, Class 1

TRU-2500

2.488 Gb/s SAW Filter Clock Recovery and Data Retiming Module

Outline Diagram

68 Pin surface mount package
Dimmensions are in inches



Order Information

Table 5. Part Numbering Information

Part Number	Bit Rate	Operating Temperature	Comcode
TRU2500-C	2488.32 Mb/s	0°C to 70°C	330012071
TRU2500-L	2488.32 Mb/s	-40°C to+85°C	330006701

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