NEC

MOS INTEGRATED CIRCUIT

μPD44321162, 44321182, 44321322, 44321362

32M-BIT ZEROSB™ SRAM
PIPELINED OPERATION

Description

The μPD44321162 is a 2,097,152-word by 16-bit, the μPD44321182 is a 2,097,152-word by 18-bit, the μPD44321322 is a 1,048,576-word by 32-bit and the μPD44321362 is a 1,048,576-word by 36-bit ZEROSB static RAM fabricated with advanced CMOS technology using full CMOS six-transistor memory cell.

The μPD44321162, μPD44321182, μPD44321322 and μPD44321362 are optimized to eliminate dead cycles for read to write, or write to read transitions. These ZEROSB static RAMs integrate unique synchronous peripheral circuitry, 2-bit burst counter and output buffer as well as SRAM core. All input registers are controlled by a positive edge of the single clock input (CLK).

The μPD44321162, μPD44321182, μPD44321322 and μPD44321362 are suitable for applications which require synchronous operation, high speed, low voltage, high density and wide bit configuration, such as buffer memory.

ZZ has to be set LOW at the normal operation. When ZZ is set HIGH, the SRAM enters Power Down State (“Sleep”). In the “Sleep” state, the SRAM internal state is preserved. When ZZ is set LOW again, the SRAM resumes normal operation.

The μPD44321162, μPD44321182, μPD44321322 and μPD44321362 are packaged in 100-pin PLASTIC LQFP with a 1.4 mm package thickness or 165-pin PLASTIC FBGA for high density and low capacitive loading.

Features

- Low voltage core supply : V_{DD} = 3.3 ± 0.165V (-A44, -A50, -A60)
  V_{DD} = 2.5 ± 0.125V (-C50, -C60)
- Synchronous operation
- 100 percent bus utilization
- Internally self-timed write control
- Burst read / write : Interleaved burst and linear burst sequence
- Fully registered inputs and outputs for pipelined operation
- All registers triggered off positive clock edge
- 3.3V or 2.5V LVTTL Compatible : All inputs and outputs
- Fast clock access time : 2.8 ns (225 MHz), 3.2 ns (200 MHz), 3.5 ns (167 MHz)
- Asynchronous output enable : /G
- Burst sequence selectable : MODE
- Sleep mode : ZZ (ZZ = Open or Low : Normal operation)
- Separate byte write enable : /BW1 to /BW4 (μPD44321322 and μPD44321362)
  /BW1 to /BW2 (μPD44321162 and μPD44321182)
- Three chip enables for easy depth expansion
- Common I/O using three state outputs

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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Ordering Information (1/2)

Part number	Access Time ns	Clock Frequency MHz	Core Supply Voltage V	I/O Interface	Package
μPD44321162GF-A44	2.8	225	3.3 ± 0.165	3.3 V or 2.5 V LVTTL	100-pin PLASTIC LQFP (14 x 20)
μPD44321162GF-A50	3.2	200			
μPD44321162GF-A60	3.5	167			
μPD44321182GF-A44	2.8	225			
μPD44321182GF-A50	3.2	200			
μPD44321182GF-A60	3.5	167			
μPD44321322GF-A44	2.8	225			
μPD44321322GF-A50	3.2	200			
μPD44321322GF-A60	3.5	167			
μPD44321362GF-A44	2.8	225			
μPD44321362GF-A50	3.2	200			
μPD44321362GF-A60	3.5	167			
μPD44321162GF-C50	3.2	200	2.5 ± 0.125	2.5 V LVTTL	
μPD44321162GF-C60	3.5	167			
μPD44321182GF-C50	3.2	200			
μPD44321182GF-C60	3.5	167			
μPD44321322GF-C50	3.2	200			
μPD44321322GF-C60	3.5	167			
μPD44321362GF-C50	3.2	200			
μPD44321362GF-C60	3.5	167			
μPD44321162F1-A44-FQ2	2.8	225	3.3 ± 0.165	3.3 V or 2.5 V LVTTL	165-pin PLASTIC FBGA (15 x 17)
μPD44321162F1-A50-FQ2	3.2	200			
μPD44321162F1-A60-FQ2	3.5	167			
μPD44321182F1-A44-FQ2	2.8	225			
μPD44321182F1-A50-FQ2	3.2	200			
μPD44321182F1-A60-FQ2	3.5	167			
μPD44321322F1-A44-FQ2	2.8	225			
μPD44321322F1-A50-FQ2	3.2	200			
μPD44321322F1-A60-FQ2	3.5	167			
μPD44321362F1-A44-FQ2	2.8	225			
μPD44321362F1-A50-FQ2	3.2	200			
μPD44321362F1-A60-FQ2	3.5	167			

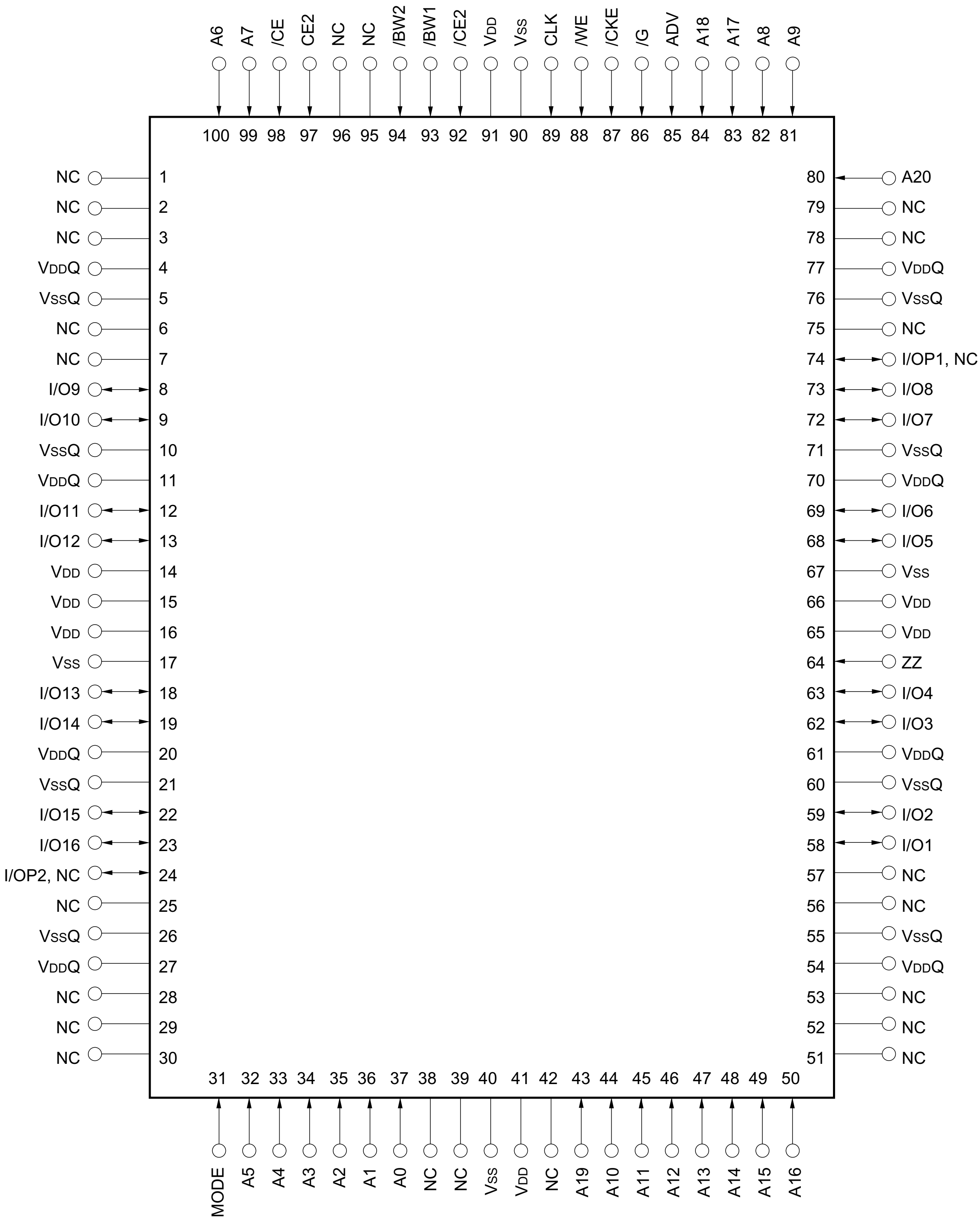
(2/2)

Part number	Access Time ns	Clock Frequency MHz	Core Supply Voltage V	I/O Interface	Package
μPD44321162F1-C50-FQ2	3.2	200	2.5 ± 0.125	2.5 V LVTTL	165-pin PLASTIC FBGA (15 x 17)
μPD44321162F1-C60-FQ2	3.5	167			
μPD44321182F1-C50-FQ2	3.2	200			
μPD44321182F1-C60-FQ2	3.5	167			
μPD44321322F1-C50-FQ2	3.2	200			
μPD44321322F1-C60-FQ2	3.5	167			
μPD44321362F1-C50-FQ2	3.2	200			
μPD44321362F1-C60-FQ2	3.5	167			

Pin Configurations (Marking Side)

/××× indicates active low signal.

100-pin PLASTIC LQFP (14 × 20)
[μPD44321162GF, μPD44321182GF]



Remark Refer to **Package Drawings** for the 1-pin index mark.

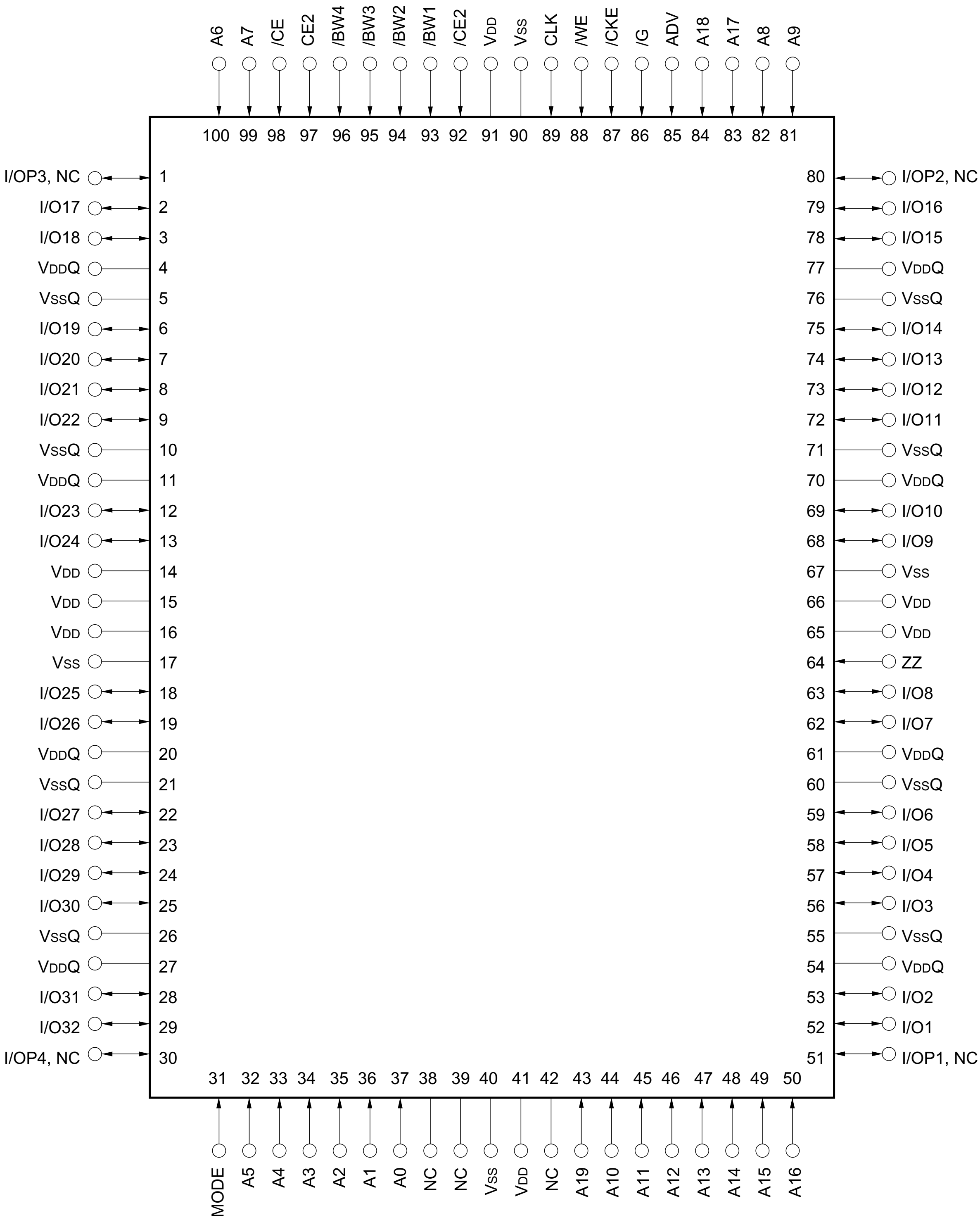
Pin Identifications

[μPD44321162GF, μPD44321182GF]

Symbol	Pin No.	Description
A0 to A20	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50, 83, 84, 43, 80	Synchronous Address Input
I/O1 to I/O16	58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	Synchronous Data In, Synchronous / Asynchronous Data Out
I/OP1, NC Note	74	Synchronous Data In (Parity), Synchronous / Asynchronous Data Out (Parity)
I/OP2, NC Note	24	
ADV	85	Synchronous Address Load / Advance Input
/CE, CE2, /CE2	98, 97, 92	Synchronous Chip Enable Input
/WE	88	Synchronous Write Enable Input
/BW1, /BW2	93, 94	Synchronous Byte Write Enable Input
/G	86	Asynchronous Output Enable Input
CLK	89	Clock Input
/CKE	87	Synchronous Clock Enable Input
MODE	31	Asynchronous Burst Sequence Select Input Have to tied to V_{DD} or V_{SS} during normal operation
ZZ	64	Asynchronous Power Down State Input
V_{DD}	14, 15, 16, 41, 65, 66, 91	Power Supply
V_{SS}	17, 40, 67, 90	Ground
$V_{DD}Q$	4, 11, 20, 27, 54, 61, 70, 77	Output Buffer Power Supply
$V_{SS}Q$	5, 10, 21, 26, 55, 60, 71, 76	Output Buffer Ground
NC	1, 2, 3, 6, 7, 25, 28, 29, 30, 38, 39, 42, 51, 52, 53, 56, 57, 75, 78, 79, 95, 96	No Connection

Note NC (No Connection) is used in the μPD44321162GF.
I/OP1 to I/OP2 are used in the μPD44321182GF.

100-pin PLASTIC LQFP (14 × 20)
[μPD44321322GF, μPD44321362GF]



Remark Refer to **Package Drawings** for the 1-pin index mark.

[μPD44321322GF, μPD44321362GF]

Symbol	Pin No.	Description
A0 to A19	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50, 83, 84, 43	Synchronous Address Input
I/O1 to I/O32	52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	Synchronous Data In, Synchronous / Asynchronous Data Out
I/OP1, NC Note	51	Synchronous Data In (Parity), Synchronous / Asynchronous Data Out (Parity)
I/OP2, NC Note	80	
I/OP3, NC Note	1	
I/OP4, NC Note	30	
ADV	85	Synchronous Address Load / Advance Input
/CE, CE2, /CE2	98, 97, 92	Synchronous Chip Enable Input
/WE	88	Synchronous Write Enable Input
/BW1 to /BW4	93, 94, 95, 96	Synchronous Byte Write Enable Input
/G	86	Asynchronous Output Enable Input
CLK	89	Clock Input
/CKE	87	Synchronous Clock Enable Input
MODE	31	Asynchronous Burst Sequence Select Input Have to tied to V_{DD} or V_{SS} during normal operation
ZZ	64	Asynchronous Power Down State Input
V_{DD}	14, 15, 16, 41, 65, 66, 91	Power Supply
V_{SS}	17, 40, 67, 90	Ground
$V_{DD}Q$	4, 11, 20, 27, 54, 61, 70, 77	Output Buffer Power Supply
$V_{SS}Q$	5, 10, 21, 26, 55, 60, 71, 76	Output Buffer Ground
NC	38, 39, 42	No Connection

Note NC (No Connection) is used in the μPD44321322GF.
I/OP1 to I/OP4 are used in the μPD44321362GF.

165-pin PLASTIC FBGA (15 x 17)

(Top View)

[μPD44321162F1, μPD44321182F1]

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A7	/CE	/BW2	NC	/CE2	/CKE	ADV	A17	A9	A20
B	NC	A6	CE2	NC	/BW1	CLK	/WE	/G	A18	A8	NC
C	NC	NC	$V_{DD}Q$	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	$V_{DD}Q$	NC	I/OP1,NC
D	NC	I/O9	$V_{DD}Q$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	$V_{DD}Q$	NC	I/O8
E	NC	I/O10	$V_{DD}Q$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	$V_{DD}Q$	NC	I/O7
F	NC	I/O11	$V_{DD}Q$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	$V_{DD}Q$	NC	I/O6
G	NC	I/O12	$V_{DD}Q$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	$V_{DD}Q$	NC	I/O5
H	NC	V_{DD}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	I/O13	NC	$V_{DD}Q$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	$V_{DD}Q$	I/O4	NC
K	I/O14	NC	$V_{DD}Q$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	$V_{DD}Q$	I/O3	NC
L	I/O15	NC	$V_{DD}Q$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	$V_{DD}Q$	I/O2	NC
M	I/O16	NC	$V_{DD}Q$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	$V_{DD}Q$	I/O1	NC
N	I/OP2,NC	NC	$V_{DD}Q$	V_{SS}	NC	NC	NC	V_{SS}	$V_{DD}Q$	NC	NC
P	NC	NC	A4	A12	TDI	A1	TDO	A19	A13	A14	NC
R	MODE	A5	A3	A2	TMS	A0	TCK	A10	A11	A15	A16

Remark Refer to **Package Drawings** for the index mark.

[μPD44321162F1, μPD44321182F1]

Symbol	Pin No.	Description
A0 to A20	6R, 6P, 4R, 3R, 3P, 2R, 2B, 2A, 10B, 10A, 8R, 9R, 4P, 9P, 10P, 10R, 11R, 9A, 9B, 8P, 11A	Synchronous Address Input
I/O1 to I/O16	10M, 10L, 10K, 10J, 11G, 11F, 11E, 11D, 2D, 2E, 2F, 2G, 1J, 1K, 1L, 1M	Synchronous Data In, Synchronous / Asynchronous Data Out
I/OP1, NC Note	11C	Synchronous Data In (Parity), Synchronous / Asynchronous Data Out (Parity)
I/OP2, NC Note	1N	
ADV	8A	Synchronous Address Load / Advance Input
/CE, CE2, /CE2	3A, 3B, 6A	Synchronous Chip Enable Input
/WE	7B	Synchronous Write Enable Input
/BW1, /BW2	5B, 4A	Synchronous Byte Write Enable Input
/G	8B	Asynchronous Output Enable Input
CLK	6B	Clock Input
/CKE	7A	Synchronous Clock Enable Input
MODE	1R	Asynchronous Burst Sequence Select Input Have to tied to V_{DD} or V_{SS} during normal operation
ZZ	11H	Asynchronous Power Down State Input
V_{DD}	2H, 4D, 4E, 4F, 4G, 4H, 4J, 4K, 4L, 4M, 8D, 8E, 8F, 8G, 8H, 8J, 8K, 8L, 8M	Power Supply
V_{SS}	4C, 4N, 5C, 5D, 5E, 5F, 5G, 5H, 5J, 5K, 5L, 5M, 6C, 6D, 6E, 6F, 6G, 6H, 6J, 6K, 6L, 6M, 7C, 7D, 7E, 7F, 7G, 7H, 7J, 7K, 7L, 7M, 8C, 8N	Ground
$V_{DD}Q$	3C, 3D, 3E, 3F, 3G, 3J, 3K, 3L, 3M, 3N, 9C, 9D, 9E, 9F, 9G, 9J, 9K, 9L, 9M, 9N	Output Buffer Power Supply
NC	1A, 1B, 1C, 1D, 1E, 1F, 1G, 1H, 1P, 2C, 2J, 2K, 2L, 2M, 2N, 2P, 3H, 4B, 5A, 5N, 6N, 7N, 9H, 10C, 10D, 10E, 10F, 10G, 10H, 10N, 11B, 11J, 11K, 11L, 11M, 11N, 11P	No Connection
TMS	5R	Test Mode Select (JTAG)
TDI	5P	Test Data Input (JTAG)
TCK	7R	Test Clock Input (JTAG)
TDO	7P	Test Data Output (JTAG)

Note NC (No Connection) is used in the μPD44321162GF.
I/OP1 to I/OP2 are used in the μPD44321182GF.

165-pin PLASTIC FBGA (15 x 17)

(Top View)

[μPD44321322F1, μPD44321362F1]

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A7	/CE	/BW3	/BW2	/CE2	/CKE	ADV	A17	A9	NC
B	NC	A6	CE2	/BW4	/BW1	CLK	/WE	/G	A18	A8	NC
C	I/OP3,NC	NC	$V_{DD}Q$	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	$V_{DD}Q$	NC	I/OP2,NC
D	I/O17	I/O21	$V_{DD}Q$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	$V_{DD}Q$	I/O16	I/O12
E	I/O18	I/O22	$V_{DD}Q$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	$V_{DD}Q$	I/O15	I/O11
F	I/O19	I/O23	$V_{DD}Q$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	$V_{DD}Q$	I/O14	I/O10
G	I/O20	I/O24	$V_{DD}Q$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	$V_{DD}Q$	I/O13	I/O9
H	NC	V_{DD}	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	I/O25	I/O29	$V_{DD}Q$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	$V_{DD}Q$	I/O8	I/O4
K	I/O26	I/O30	$V_{DD}Q$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	$V_{DD}Q$	I/O7	I/O3
L	I/O27	I/O31	$V_{DD}Q$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	$V_{DD}Q$	I/O6	I/O2
M	I/O28	I/O32	$V_{DD}Q$	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	$V_{DD}Q$	I/O5	I/O1
N	I/OP4,NC	NC	$V_{DD}Q$	V_{SS}	NC	NC	NC	V_{SS}	$V_{DD}Q$	NC	I/OP1,NC
P	NC	NC	A4	A12	TDI	A1	TDO	A19	A13	A14	NC
R	MODE	A5	A3	A2	TMS	A0	TCK	A10	A11	A15	A16

Remark Refer to **Package Drawings** for the index mark.

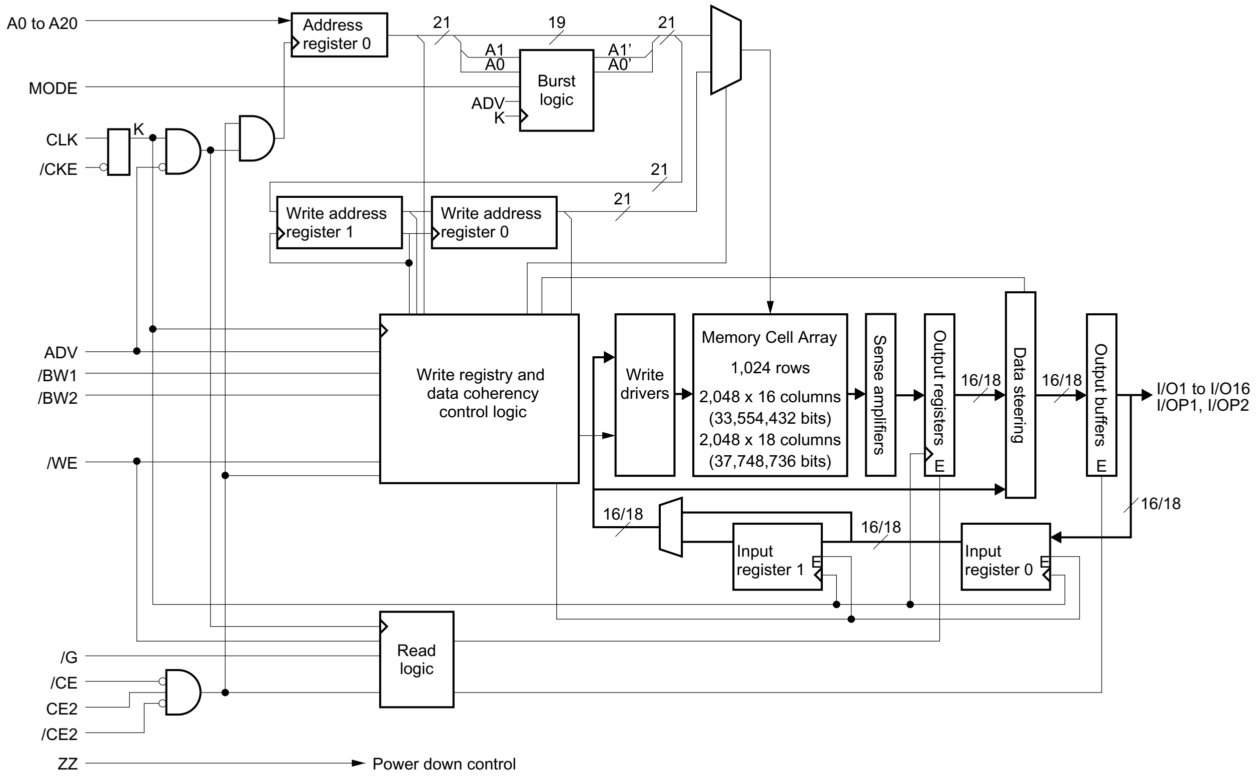
[μPD44321322GF, μPD44321362GF]

Symbol	Pin No.	Description
A0 to A19	6R, 6P, 4R, 3R, 3P, 2R, 2B, 2A, 10B, 10A, 8R, 9R, 4P, 9P, 10P, 10R, 11R, 9A, 9B, 8P	Synchronous Address Input
I/O1 to I/O32	11M, 11L, 11K, 11J, 10M, 10L, 10K, 10J, 11G, 11F, 11E, 11D, 10G, 10F, 10E, 10D, 1D, 1E, 1F, 1G, 2D, 2E, 2F, 2G,1J, 1K, 1L, 1M, 2J, 2K, 2L, 2M	Synchronous Data In, Synchronous / Asynchronous Data Out
I/OP1, NC Note	11N	Synchronous Data In (Parity), Synchronous / Asynchronous Data Out (Parity)
I/OP2, NC Note	11C	
I/OP3, NC Note	1C	
I/OP4, NC Note	1N	
ADV	8A	Synchronous Address Load / Advance Input
/CE, CE2, /CE2	3A, 3B, 6A	Synchronous Chip Enable Input
/WE	7B	Synchronous Write Enable Input
/BW1 to /BW4	5B, 5A, 4A, 4B	Synchronous Byte Write Enable Input
/G	8B	Asynchronous Output Enable Input
CLK	6B	Clock Input
/CKE	7A	Synchronous Clock Enable Input
MODE	1R	Asynchronous Burst Sequence Select Input Have to tied to V_{DD} or V_{SS} during normal operation
ZZ	11H	Asynchronous Power Down State Input
V_{DD}	2H, 4D, 4E, 4F, 4G, 4H, 4J, 4K, 4L, 4M, 8D, 8E, 8F, 8G, 8H, 8J, 8K, 8L, 8M	Power Supply
V_{SS}	4C, 4N, 5C, 5D, 5E, 5F, 5G, 5H, 5J, 5K, 5L, 5M, 6C, 6D, 6E, 6F, 6G, 6H, 6J, 6K, 6L, 6M, 7C, 7D, 7E, 7F, 7G, 7H, 7J, 7K, 7L, 7M, 8C, 8N	Ground
$V_{DD}Q$	3C, 3D, 3E, 3F, 3G, 3J, 3K, 3L, 3M, 3N, 9C, 9D, 9E, 9F, 9G, 9J, 9K, 9L, 9M, 9N	Output Buffer Power Supply
NC	1A, 1B, 1H, 1P, 2C, 2N, 2P, 3H, 5N, 6N, 7N, 9H, 10C, 10H, 10N, 11A, 11B, 11P	No Connection
TMS	5R	Test Mode Select (JTAG)
TDI	5P	Test Data Input (JTAG)
TCK	7R	Test Clock Input (JTAG)
TDO	7P	Test Data Output (JTAG)

Note NC (No Connection) is used in the μPD44321322GF.
I/OP1 to I/OP4 are used in the μPD44321362GF.

Block Diagrams

[μPD44321162, μPD44321182]



Burst Sequence

[μPD44321162, μPD44321182]

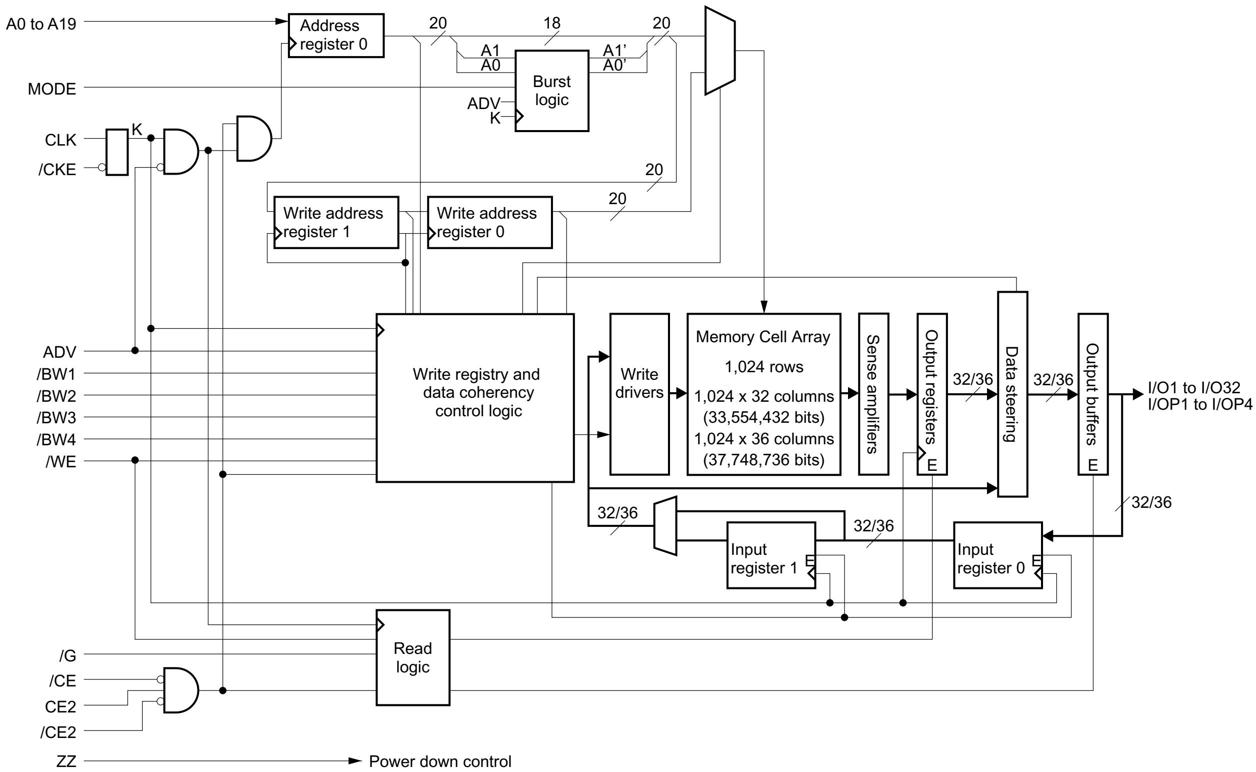
Interleaved Burst Sequence Table (MODE = V_{DD})

External Address	A20 to A2, A1, A0
1st Burst Address	A20 to A2, A1, /A0
2nd Burst Address	A20 to A2, /A1, A0
3rd Burst Address	A20 to A2, /A1, /A0

Linear Burst Sequence Table (MODE = V_{SS})

External Address	A20 to A2, 0, 0	A20 to A2, 0, 1	A20 to A2, 1, 0	A20 to A2, 1, 1
1st Burst Address	A20 to A2, 0, 1	A20 to A2, 1, 0	A20 to A2, 1, 1	A20 to A2, 0, 0
2nd Burst Address	A20 to A2, 1, 0	A20 to A2, 1, 1	A20 to A2, 0, 0	A20 to A2, 0, 1
3rd Burst Address	A20 to A2, 1, 1	A20 to A2, 0, 0	A20 to A2, 0, 1	A20 to A2, 1, 0

[μPD44321322, μPD44321362]



[μPD44321322, μPD44321362]

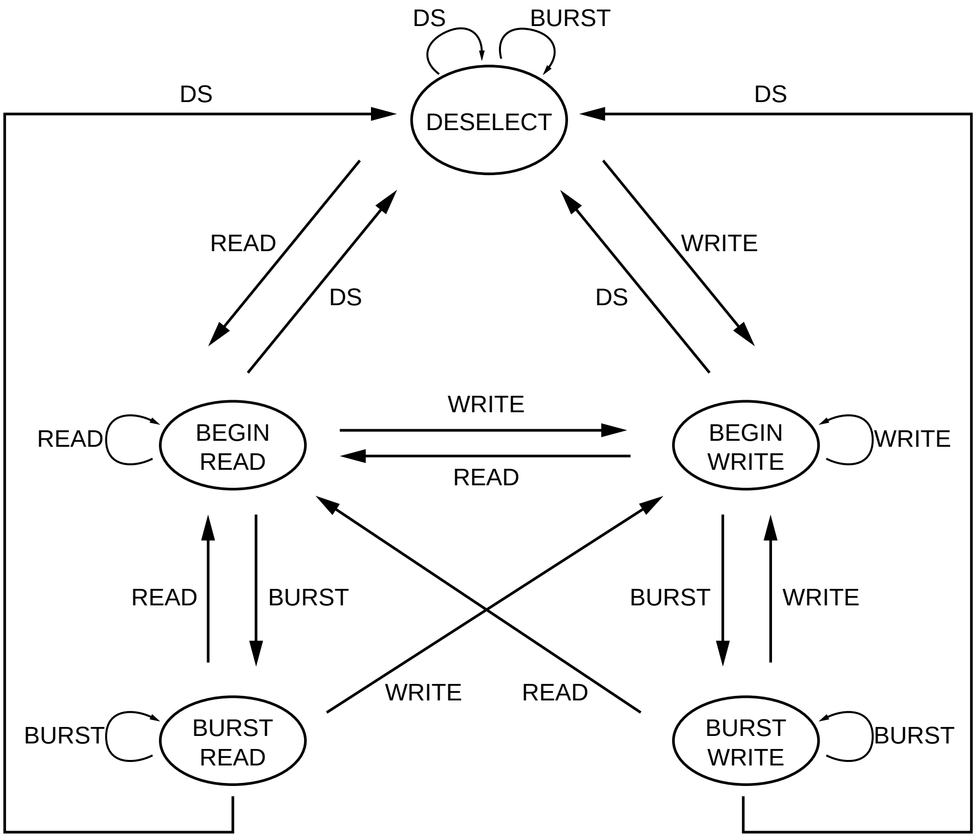
Interleaved Burst Sequence Table (MODE = V_{DD})

External Address	A19 to A2, A1, A0
1st Burst Address	A19 to A2, A1, /A0
2nd Burst Address	A19 to A2, /A1, A0
3rd Burst Address	A19 to A2, /A1, /A0

Linear Burst Sequence Table (MODE = V_{SS})

External Address	A19 to A2, 0, 0	A19 to A2, 0, 1	A19 to A2, 1, 0	A19 to A2, 1, 1
1st Burst Address	A19 to A2, 0, 1	A19 to A2, 1, 0	A19 to A2, 1, 1	A19 to A2, 0, 0
2nd Burst Address	A19 to A2, 1, 0	A19 to A2, 1, 1	A19 to A2, 0, 0	A19 to A2, 0, 1
3rd Burst Address	A19 to A2, 1, 1	A19 to A2, 0, 0	A19 to A2, 0, 1	A19 to A2, 1, 0

State Diagram



Command	Operation
DS	Deselect
Read	New Read
Write	New Write
Burst	Burst Read, Burst Write or Continue Deselect

Remarks **1.** States change on the rising edge of the clock.

2. A Stall or Ignore Clock Edge cycle is not shown in the above diagram. This is because /CKE HIGH only blocks the clock (CLK) input and does not change the state of the device.

Asynchronous Truth Table

Operation	/G	I/O
Read Cycle	L	Data-Out
Read Cycle	H	High-Z
Write Cycle	×	High-Z, Data-In
Deselected	×	High-Z

Remark × : don't care

Synchronous Truth Table

Operation	/CE	CE2	/CE2	ADV	/WE	/BWs	/CKE	CLK	I/O	Address	Note
Deselected	H	×	×	L	×	×	L	L → H	High-Z	None	1
Deselected	×	L	×	L	×	×	L	L → H	High-Z	None	1
Deselected	×	×	H	L	×	×	L	L → H	High-Z	None	1
Continue Deselected	×	×	×	H	×	×	L	L → H	High-Z	None	1
Read Cycle / Begin Burst	L	H	L	L	H	×	L	L → H	Data-Out	External	
Read Cycle / Continue Burst	×	×	×	H	×	×	L	L → H	Data-Out	Next	
Write Cycle / Begin Burst	L	H	L	L	L	L	L	L → H	Data-In	External	
Write Cycle / Continue Burst	×	×	×	H	×	L	L	L → H	Data-In	Next	
Write Cycle / Write Abort	L	H	L	L	L	H	L	L → H	High-Z	External	
Write Cycle / Write Abort	×	×	×	H	×	H	L	L → H	High-Z	Next	
Stall / Ignore Clock Edge	×	×	×	×	×	×	H	L → H	–	Current	2

Notes **1.** Deselect status is held until new "Begin Burst" entry.

2. If an Ignore Clock Edge command occurs during a read operation, the I/O bus will remain active (Low-impedance). If it occurs during a write cycle, the bus will remain High impedance. No write operation will be performed during the Ignore Clock Edge cycle.

Remarks **1.** × : don't care

2. /BWs = L means any one or more byte write enables (/BW1, /BW2, /BW3 or /BW4) are LOW.
/BWs = H means all byte write enables (/BW1, /BW2, /BW3 or /BW4) are HIGH.

Partial Truth Table for Write Enables

[μPD44321162, μPD44321182]

Operation	/WE	/BW1	/BW2
Read Cycle	H	×	×
Write Cycle / Byte 1 (I/O [1:8], I/OP1)	L	L	H
Write Cycle / Byte 2 (I/O [9:16], I/OP2)	L	H	L
Write Cycle / All Bytes	L	L	L
Write Abort / NOP	L	H	H

Remark × : don't care

[μPD44321322, μPD44321362]

Operation	/WE	/BW1	/BW2	/BW3	/BW4
Read Cycle	H	×	×	×	×
Write Cycle / Byte 1 (I/O [1:8], I/OP1)	L	L	H	H	H
Write Cycle / Byte 2 (I/O [9:16], I/OP2)	L	H	L	H	H
Write Cycle / Byte 3 (I/O [17:24], I/OP3)	L	H	H	L	H
Write Cycle / Byte 4 (I/O [25:32], I/OP4)	L	H	H	H	L
Write Cycle / All Bytes	L	L	L	L	L
Write Abort / NOP	L	H	H	H	H

Remark × : don't care

ZZ (Sleep) Truth Table

ZZ	Chip Status
≤ 0.2 V	Active
Open	Active
≥ V_{DD} – 0.2 V	Sleep

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		-A44, -A50, -A60	–0.5		+4.0	V
			-C50, -C60	–0.5		+3.0	
Output supply voltage	$V_{DD}Q$			–0.5		V_{DD}	V
Input voltage	V_{IN}			–0.5 Note		V_{DD} + 0.5	V
Input / Output voltage	$V_{I/O}$			–0.5 Note		$V_{DD}Q$ + 0.5	V
Operating ambient temperature	T_A			0		70	°C
Storage temperature	T_{stg}			–55		+125	°C

Note –2.0 V (MIN.) (Pulse width : 2 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70 °C) (1/2)

Parameter	Symbol	Conditions	-A44, -A50, -A60			Unit
			MIN.	TYP.	MAX.	
Supply voltage	V_{DD}		3.135	3.3	3.465	V
2.5 V LVTTL Interface						
Output supply voltage	$V_{DD}Q$		2.375	2.5	2.9	V
High level input voltage	V_{IH}		1.7		$V_{DD}Q$ + 0.3	V
Low level input voltage	V_{IL}		–0.3 Note		+0.7	V
3.3 V LVTTL Interface						
Output supply voltage	$V_{DD}Q$		3.135	3.3	3.465	V
High level input voltage	V_{IH}		2.0		$V_{DD}Q$ + 0.3	V
Low level input voltage	V_{IL}		–0.3 Note		+0.8	V

Note –0.8 V (MIN.) (Pulse width : 2 ns)

Recommended DC Operating Conditions (T_A = 0 to 70 °C) (2/2)

Parameter	Symbol	Conditions	-C50, -C60			Unit
			MIN.	TYP.	MAX.	
Supply voltage	V_{DD}		2.375	2.5	2.625	V
Output supply voltage	$V_{DD}Q$		2.375	2.5	2.625	V
High level input voltage	V_{IH}		1.7		$V_{DD}Q$ + 0.3	V
Low level input voltage	V_{IL}		–0.3 Note		+0.7	V

Note –0.8 V (MIN.) (Pulse width : 2 ns)

DC Characteristics (T_A = 0 to 70°C, V_{DD} = 3.3 ± 0.165 V or 2.5 ± 0.125 V)

Parameter	Symbol	Test condition		MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	V_{IN} (except ZZ, MODE) = 0 V to V_{DD}		–2		+2	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{DD}Q, Outputs are disabled.		–2		+2	μA
Operating supply current	I_{DD}	Device selected, Cycle = MAX.	-A44			440	mA
		$V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$,	-A50, -C50			410	
		$I_{I/O}$ = 0 mA	-A60, -C60			360	
Standby supply current	I_{SB}	Device deselected, Cycle = 0 MHz, $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, All inputs are static.				70	mA
	I_{SB1}	Device deselected, Cycle = 0 MHz, $V_{IN} \leq$ 0.2 V or $V_{IN} \geq V_{DD}$ – 0.2 V, $V_{I/O} \leq$ 0.2 V, All inputs are static.				60	
	I_{SB2}	Device deselected, Cycle = MAX. $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$				130	
Power down supply current	I_{SBZZ}	ZZ ≥ V_{DD} – 0.2 V, $V_{I/O} \leq V_{DD}$Q + 0.2 V				60	mA
2.5 V LVTTL Interface							
High level output voltage	V_{OH}	I_{OH} = –2.0 mA		1.7			V
		I_{OL} = –1.0 mA		2.1			
Low level output voltage	V_{OL}	I_{OH} = +2.0 mA				0.7	V
		I_{OL} = +1.0 mA				0.4	
3.3 V LVTTL Interface							
High level output voltage	V_{OH}	I_{OH} = –4.0 mA		2.4			V
Low level output voltage	V_{OL}	I_{OL} = +8.0 mA				0.4	V

Capacitance (T_A = 25 °C, f = 1MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			6.0	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			8.0	pF
Clock input capacitance	C_{clk}	V_{clk} = 0 V			6.0	pF

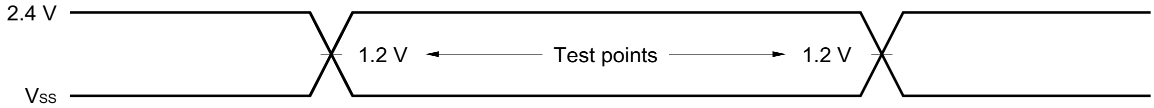
Remark These parameters are periodically sampled and not 100% tested.

AC Characteristics (T_A = 0 to 70°C, V_{DD} = 3.3 ± 0.165 V or 2.5 ± 0.125 V)

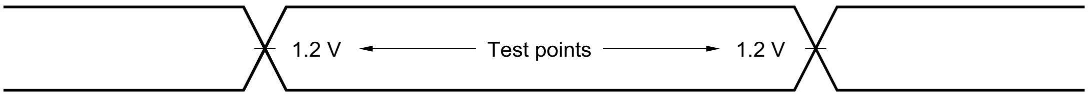
AC Test Conditions

2.5 V LVTTL Interface

Input waveform (Rise / Fall time ≤ 2.4 ns)

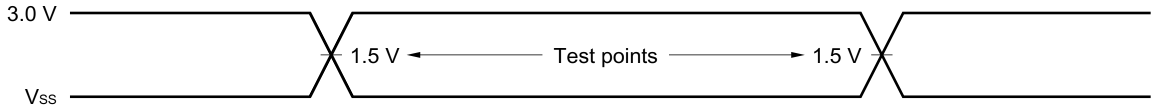


Output waveform

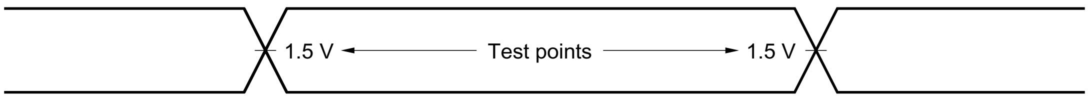


3.3 V LVTTL Interface

Input waveform (Rise / Fall time ≤ 3.0 ns)



Output waveform

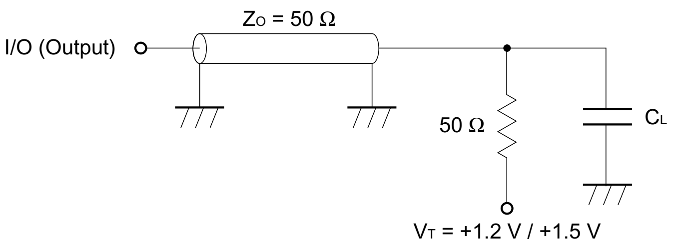


Output load condition

C_L : 30 pF

5 pF (TKHQX1, TKHQX2, TGLQX, TGHQZ, TKHQZ)

Figure External load at test



Remark C_L includes capacitances of the probe and jig, and stray capacitances.

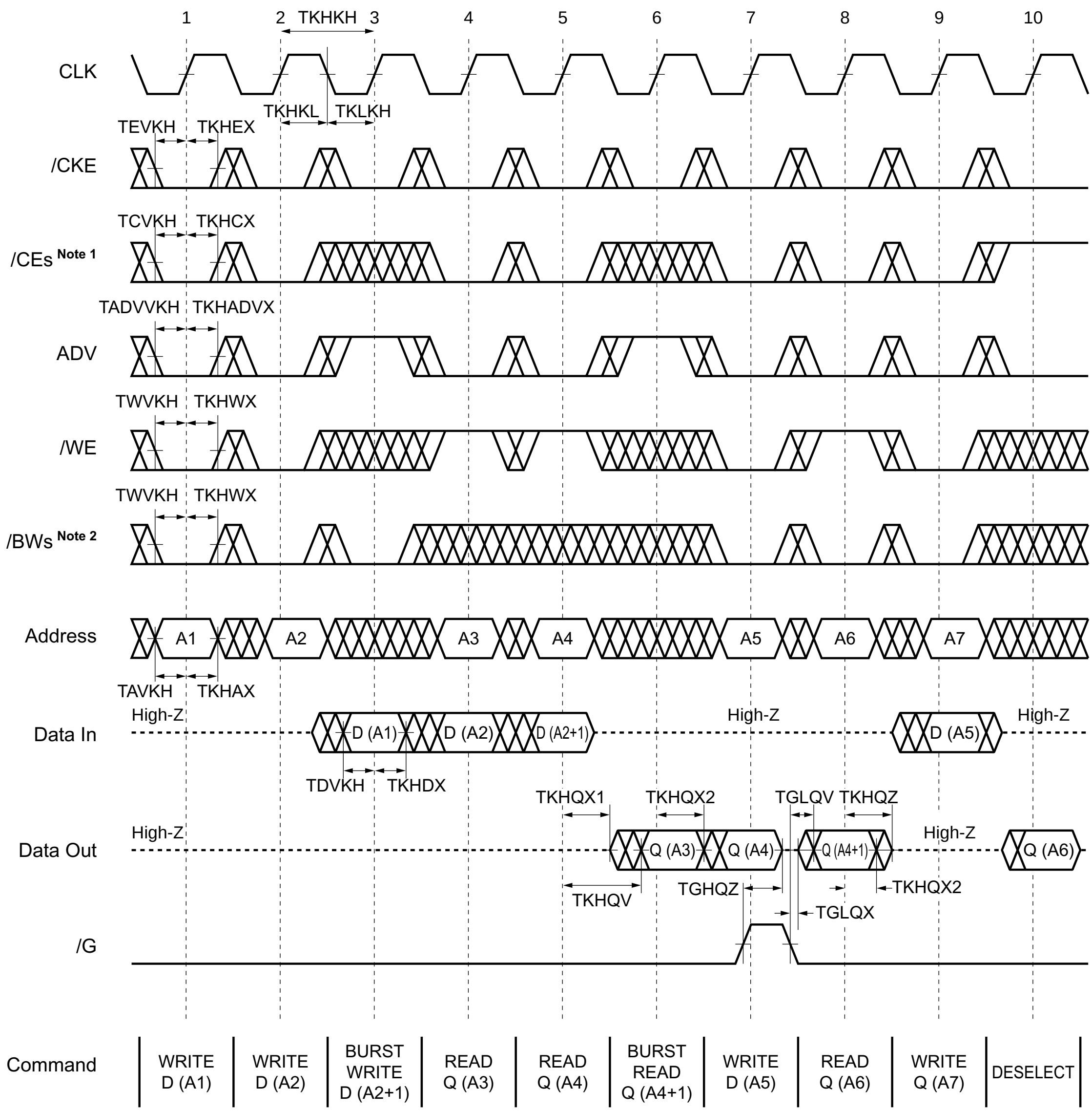
Read and Write Cycle

Parameter		Symbol Standard	Symbol Alias	-A44 (225 MHz) MIN.	-A44 (225 MHz) MAX.	-A50, -C50 (200 MHz) MIN.	-A50, -C50 (200 MHz) MAX.	-A60, -C60 (167 MHz) MIN.	-A60, -C60 (167 MHz) MAX.	Unit	Notes
Cycle time		TKHKH	TCYC	4.4	–	5	–	6	–	ns	
Clock access time		TKHQV	TCD	–	2.8	–	3.2	–	3.5	ns	
Output enable access time		TGLQV	TOE	–	2.8	–	3.2	–	3.5	ns	
Clock high to output active		TKHQX1	TDC1	1.5	–	1.5	–	1.5	–	ns	1, 2
Clock high to output change		TKHQX2	TDC2	1.5	–	1.5	–	1.5	–	ns	
Output enable to output active		TGLQX	TOLZ	0	–	0	–	0	–	ns	1
Output disable to output High-Z		TGHQZ	TOHZ	0	2.8	0	3.2	0	3.5	ns	1
Clock high to output High-Z		TKHQZ	TCZ	1.5	2.8	1.5	3.2	1.5	3.5	ns	1, 2
Clock high pulse width		TKHKL	TCH	1.8	–	1.8	–	1.8	–	ns	
Clock low pulse width		TKLKH	TCL	1.8	–	1.8	–	1.8	–	ns	
Setup times	Address	TAVKH	TAS	1.4	–	1.5	–	1.5	–	ns	
	Address status	TADSVKH	TSS								
	Data in	TDVKH	TDS								
	Write enable	TWVKH	TWS								
	Address advance	TADVVKH	–								
	Chip enable	TEVKH	–								
Hold times	Address	TKHAX	TAH	0.4	–	0.5	–	0.5	–	ns	
	Address status	TKHADSX	TSH								
	Data in	TKHDX	TDH								
	Write enable	TKHWX	TWH								
	Address advance	TKHADVX	–								
	Chip enable	TKHEX	–								
Power down entry time		TZZE	TZZE	8.8	–	10	–	12	–	ns	
Power down recovery time		TZZR	TZZR	8.8	–	10	–	12	–	ns	

Notes 1. Transition is measured ±200 mV from steady state.

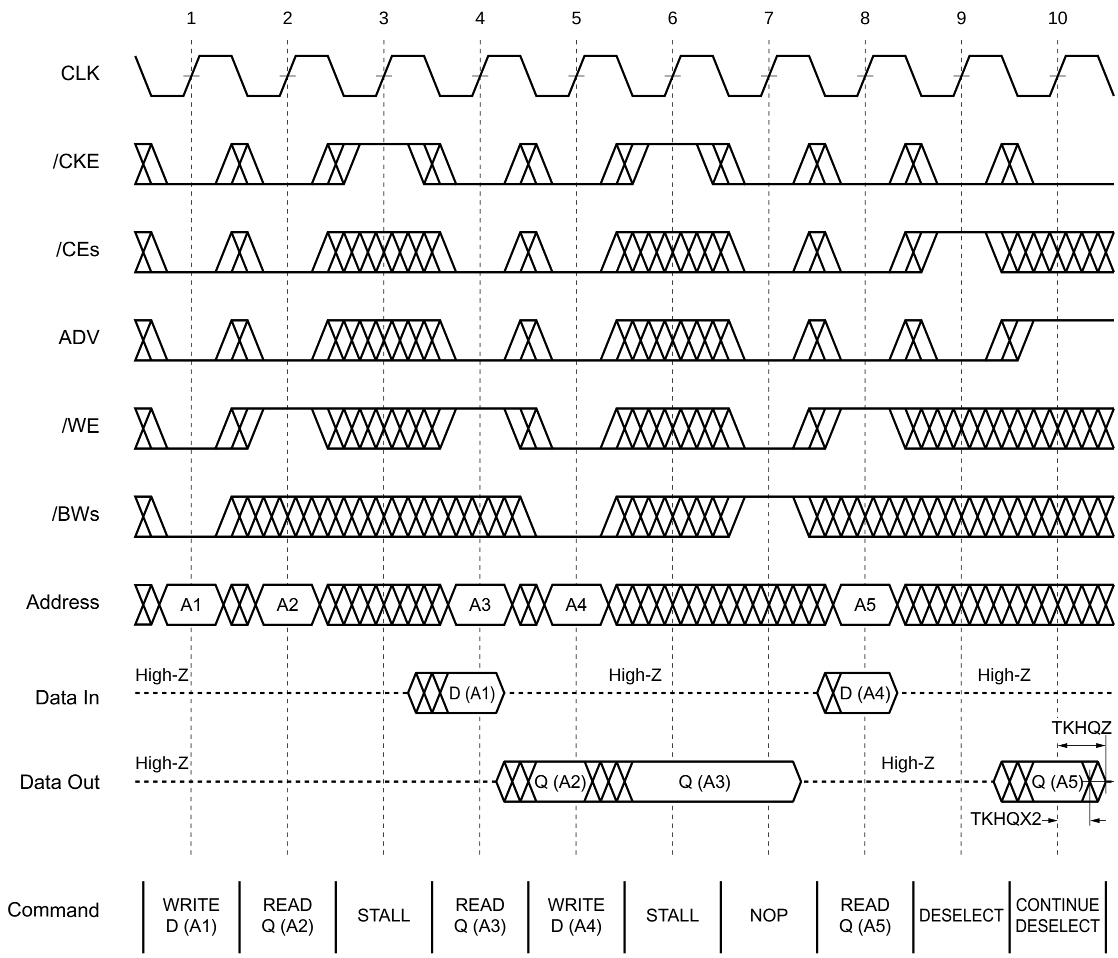
2. To avoid bus contention, the output buffers are designed such that TKHQZ (device turn-off) is faster than TKHQX1 (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because TKHQX1 is a min. parameter that is worse case at totally different conditions (0 °C, V_{DD} max.) than TKHQZ, which is a max. parameter (worse case at 70 °C, V_{DD} min.).

READ / WRITE CYCLE

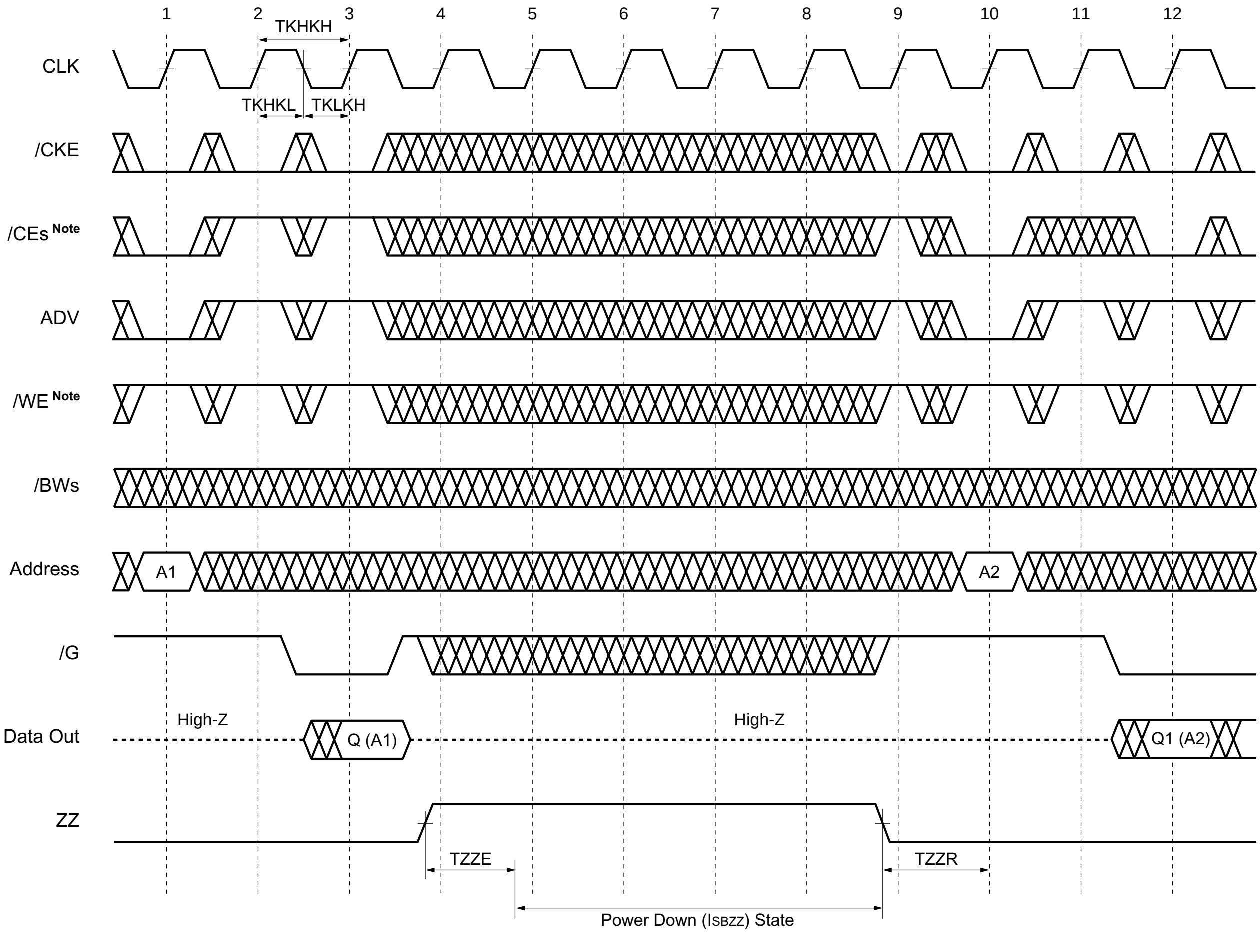


Notes
1. /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.
2. /BWs refers to /BW1, /BW2, /BW3 and /BW4. When /BWs is LOW, any one or more byte write enables (/BW1, /BW2, /BW3 or /BW4) are LOW.

NOP, STALL AND DESELECT CYCLE



POWER DOWN (ZZ) CYCLE



Note /WE or /CEs must be held HIGH at CLK rising edge (clock edge No.2 and No.3 in this figure) prior to power down state entry.

JTAG Specifications

Only the 165-pin PLASTIC FBGA package of μPD44321162, μPD44321182, μPD44321322 and μPD44321362 support a limited set of JTAG functions as in IEEE standard 1149.1.

Test Access Port (TAP) Pins

Pin Name	Description
TCK	Test Clock Input. All input are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select. This is the command input for the TAP controller state machine.
TDI	Test Data Input. This is the input side of the serial registers placed between TDI and TDO.The register placed between TDI and TDO is deter-mined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction.
TDO	Test Data Output. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Remark The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held high for five rising edges of TCK. The TAP controller state is also reset on the SRAM POWER-UP.

JTAG DC Characteristics (T_A = 0 to 70 °C, V_{DD} = 3.3 ± 0.165 V) (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
JTAG Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ V_{DD}	–5.0	–	+5.0	μA	
JTAG I/O leakage current	I_{LO}	0 V ≤ V_{IN} ≤ V_{DD}Q , Outputs disabled	–5.0	–	+5.0	μA	
JTAG input high voltage	V_{IH}		2.0	–	V_{DD}+0.3	V	
JTAG input low voltage	V_{IL}		–0.3	–	+0.5	V	
JTAG output high voltage	V_{OH}	I_{OH} = –4 mA	2.4	–	–	V	
JTAG output low voltage	V_{OL}	I_{OL} = 8 mA	–	–	0.4	V	

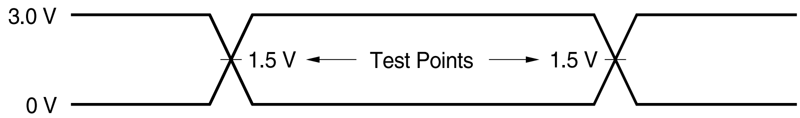
JTAG DC Characteristics (T_A = 0 to 70°C, V_{DD} = 2.5 ± 0.125 V) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
JTAG Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ V_{DD}	–5.0	–	+5.0	μA	
JTAG I/O leakage current	I_{LO}	0 V ≤ V_{IN} ≤ V_{DD}Q , Outputs disabled	–5.0	–	+5.0	μA	
JTAG input high voltage	V_{IH}		1.7	–	V_{DD}+0.3	V	
JTAG input low voltage	V_{IL}		–0.3	–	+0.5	V	
JTAG output high voltage	V_{OH}	I_{OH} = –2 mA	1.7			V	
		I_{OL} = –1 mA	2.1				
JTAG output low voltage	V_{OL}	I_{OH} = 2 mA			0.7	V	
		I_{OL} = 1 mA			0.4		

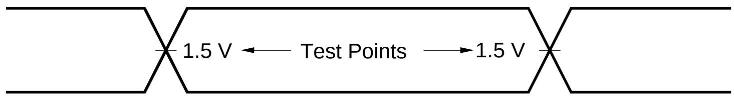
JTAG AC Test Conditions (T_A = 0 to 70 °C)

[-A44, -A50, -A60]

Input waveform (rise / fall time ≤ 1 ns)

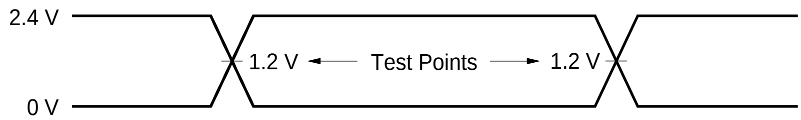


Output waveform

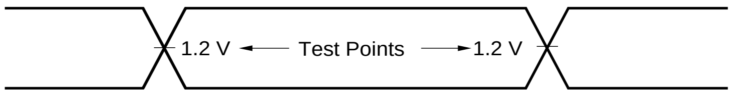


[-C50, -C60]

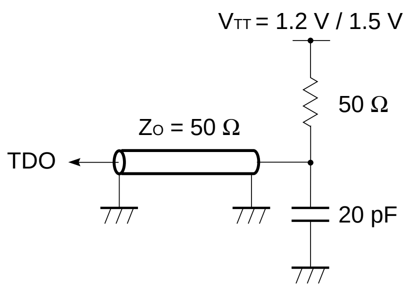
Input waveform (rise / fall time ≤ 1 ns)



Output waveform



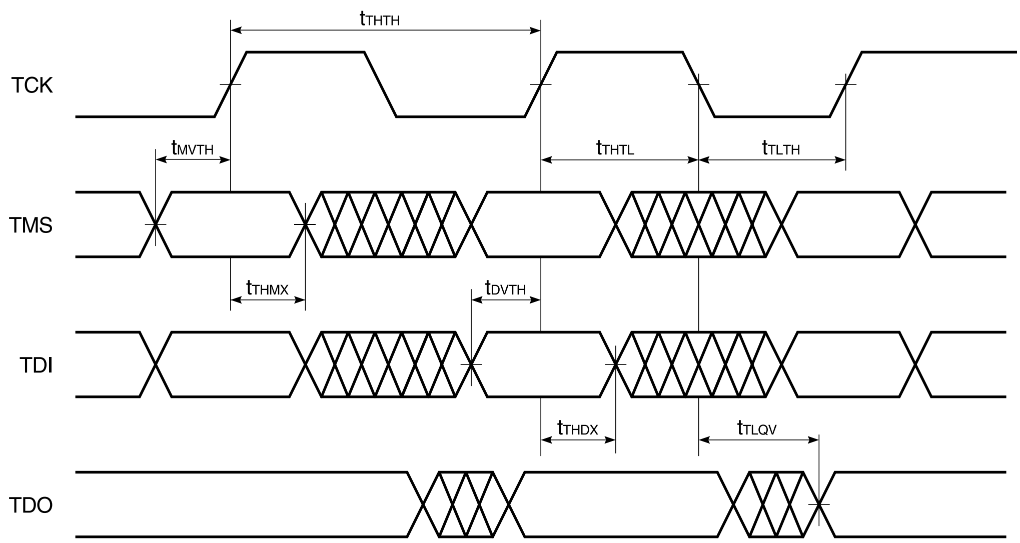
Output load



JTAG AC Characteristics (T_A = 0 to 70 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Clock Cycle Time (TCK)	t_{THTH}		100		–	ns	
Clock Phase Time (TCK)	t_{THTL} / t_{TLTH}		40		–	ns	
Setup Time (TMS / TDI)	t_{MVTH} / t_{DVTH}		10		–	ns	
Hold Time (TMS / TDI)	t_{THMX} / t_{THDX}		10		–	ns	
TCK Low to TDO Valid (TDO)	t_{TLQV}		–		20	ns	

JTAG Timing Diagram



Scan Register Definition (1)

Register name	Description
Instruction register	The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run-test/idle or the various data register state. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power-up whenever the controller is placed in test-logic-reset state.
Bypass register	The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.
ID register	The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into shift-DR state.
Boundary register	The boundary register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to shift-DR state. Several TAP instructions can be used to activate the boundary register. The Scan Exit Order tables describe which device bump connects to each boundary register location. The first column defines the bit's position in the boundary register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 1. The second column is the name of the input or I/O at the bump and the third column is the bump number.

Scan Register Definition (2)

Register name		Unit
Instruction register	3	bit
Bypass register	1	bit
ID register	32	bit
Boundary register	77	bit

ID Register Definition

Part number	Organization	ID [31:28] vendor revision no.	ID [27:12] part no.	ID [11:1] vendor ID no.	ID [0] fix bit
μPD44321162	2M x 16	XXXX	XXXX XXXX XXXX XXXX	00000010000	1
μPD44321182	2M x 18	XXXX	XXXX XXXX XXXX XXXX	00000010000	1
μPD44321322	1M x 32	XXXX	XXXX XXXX XXXX XXXX	00000010000	1
μPD44321362	1M x 36	XXXX	XXXX XXXX XXXX XXXX	00000010000	1

SCAN Exit Order

[μPD44321162 (2M words by 16 bits)]

Bit no.	Signal name	Bump ID
1	NC	6N
2	A19	8P
3	A10	8R
4	A11	9R
5	A13	9P
6	A14	10P
7	A15	10R
8	A16	11R
9	NC	11P
10	ZZ	11H
11	NC	11N
12	NC	11M
13	NC	11L
14	NC	11K
15	NC	11J
16	I/O1	10M
17	I/O2	10L
18	I/O3	10K
19	I/O4	10J
20	I/O5	11G
21	I/O6	11F
22	I/O7	11E
23	I/O8	11D
24	NC	11C
25	NC	10F
26	NC	10E
27	NC	10D
28	NC	10G
29	A20	11A
30	NC	11B
31	A9	10A
32	A8	10B
33	A17	9A
34	A18	9B
35	ADV	8A
36	/G	8B
37	/CKE	7A
38	/WE	7B
39	CLK	6B

Bit no.	Signal name	Bump ID
40	/CE2	6A
41	/BW1	5B
42	NC	5A
43	/BW2	4A
44	NC	4B
45	CE2	3B
46	/CE	3A
47	A7	2A
48	A6	2B
49	NC	1B
50	NC	1A
51	NC	1C
52	NC	1D
53	NC	1E
54	NC	1F
55	NC	1G
56	I/O9	2D
57	I/O10	2E
58	I/O11	2F
59	I/O12	2G
60	I/O13	1J
61	I/O14	1K
62	I/O15	1L
63	I/O16	1M
64	NC	1N
65	NC	2K
66	NC	2L
67	NC	2M
68	NC	2J
69	A5	2R
70	MODE	1R
71	A4	3P
72	A3	3R
73	A2	4R
74	A12	4P
75	A1	6P
76	A0	6R

[μPD44321182 (2M words by 18 bits)]

Bit no.	Signal name	Bump ID
1	NC	6N
2	A19	8P
3	A10	8R
4	A11	9R
5	A13	9P
6	A14	10P
7	A15	10R
8	A16	11R
9	NC	11P
10	ZZ	11H
11	NC	11N
12	NC	11M
13	NC	11L
14	NC	11K
15	NC	11J
16	I/O1	10M
17	I/O2	10L
18	I/O3	10K
19	I/O4	10J
20	I/O5	11G
21	I/O6	11F
22	I/O7	11E
23	I/O8	11D
24	I/OP1	11C
25	NC	10F
26	NC	10E
27	NC	10D
28	NC	10G
29	A20	11A
30	NC	11B
31	A9	10A
32	A8	10B
33	A17	9A
34	A18	9B
35	ADV	8A
36	/G	8B
37	/CKE	7A
38	/WE	7B
39	CLK	6B

Bit no.	Signal name	Bump ID
40	/CE2	6A
41	/BW1	5B
42	NC	5A
43	/BW2	4A
44	NC	4B
45	CE2	3B
46	/CE	3A
47	A7	2A
48	A6	2B
49	NC	1B
50	NC	1A
51	NC	1C
52	NC	1D
53	NC	1E
54	NC	1F
55	NC	1G
56	I/O9	2D
57	I/O10	2E
58	I/O11	2F
59	I/O12	2G
60	I/O13	1J
61	I/O14	1K
62	I/O15	1L
63	I/O16	1M
64	I/OP2	1N
65	NC	2K
66	NC	2L
67	NC	2M
68	NC	2J
69	A5	2R
70	MODE	1R
71	A4	3P
72	A3	3R
73	A2	4R
74	A12	4P
75	A1	6P
76	A0	6R

[μPD44321322 (1M words by 32 bits)]

Bit no.	Signal name	Bump ID	Bit no.	Signal name	Bump ID
1	NC	6N	40	/CE2	6A
2	A19	8P	41	/BW1	5B
3	A10	8R	42	/BW2	5A
4	A11	9R	43	/BW3	4A
5	A13	9P	44	/BW4	4B
6	A14	10P	45	CE2	3B
7	A15	10R	46	/CE1	3A
8	A16	11R	47	A7	2A
9	NC	11P	48	A6	2B
10	ZZ	11H	49	NC	1B
11	NC	11N	50	NC	1A
12	I/O1	11M	51	NC	1C
13	I/O2	11L	52	I/O17	1D
14	I/O3	11K	53	I/O18	1E
15	I/O4	11J	54	I/O19	1F
16	I/O5	10M	55	I/O20	1G
17	I/O6	10L	56	I/O21	2D
18	I/O7	10K	57	I/O22	2E
19	I/O8	10J	58	I/O23	2F
20	I/O9	11G	59	I/O24	2G
21	I/O10	11F	60	I/O25	1J
22	I/O11	11E	61	I/O26	1K
23	I/O12	11D	62	I/O27	1L
24	I/O13	10G	63	I/O28	1M
25	I/O14	10F	64	I/O29	2J
26	I/O15	10E	65	I/O30	2K
27	I/O16	10D	66	I/O31	2L
28	NC	11C	67	I/O32	2M
29	NC	11A	68	NC	1N
30	NC	11B	69	A5	2R
31	A9	10A	70	MODE	1R
32	A8	10B	71	A4	3P
33	A17	9A	72	A3	3R
34	A18	9B	73	A2	4R
35	ADV	8A	74	A12	4P
36	/G	8B	75	A1	6P
37	/CKE	7A	76	A0	6R
38	/WE	7B			
39	CLK	6B			

[μPD44321362 (1M words by 36 bits)]

Bit no.	Signal name	Bump ID	Bit no.	Signal name	Bump ID
1	NC	6N	40	/CE2	6A
2	A19	8P	41	/BW1	5B
3	A10	8R	42	/BW2	5A
4	A11	9R	43	/BW3	4A
5	A13	9P	44	/BW4	4B
6	A14	10P	45	CE2	3B
7	A15	10R	46	/CE1	3A
8	A16	11R	47	A7	2A
9	NC	11P	48	A6	2B
10	ZZ	11H	49	NC	1B
11	I/OP1	11N	50	NC	1A
12	I/O1	11M	51	I/OP3	1C
13	I/O2	11L	52	I/O17	1D
14	I/O3	11K	53	I/O18	1E
15	I/O4	11J	54	I/O19	1F
16	I/O5	10M	55	I/O20	1G
17	I/O6	10L	56	I/O21	2D
18	I/O7	10K	57	I/O22	2E
19	I/O8	10J	58	I/O23	2F
20	I/O9	11G	59	I/O24	2G
21	I/O10	11F	60	I/O25	1J
22	I/O11	11E	61	I/O26	1K
23	I/O12	11D	62	I/O27	1L
24	I/O13	10G	63	I/O28	1M
25	I/O14	10F	64	I/O29	2J
26	I/O15	10E	65	I/O30	2K
27	I/O16	10D	66	I/O31	2L
28	I/OP2	11C	67	I/O32	2M
29	NC	11A	68	I/OP4	1N
30	NC	11B	69	A5	2R
31	A9	10A	70	MODE	1R
32	A8	10B	71	A4	3P
33	A17	9A	72	A3	3R
34	A18	9B	73	A2	4R
35	ADV	8A	74	A12	4P
36	/G	8B	75	A1	6P
37	/CKE	7A	76	A0	6R
38	/WE	7B			
39	CLK	6B			

JTAG Instructions

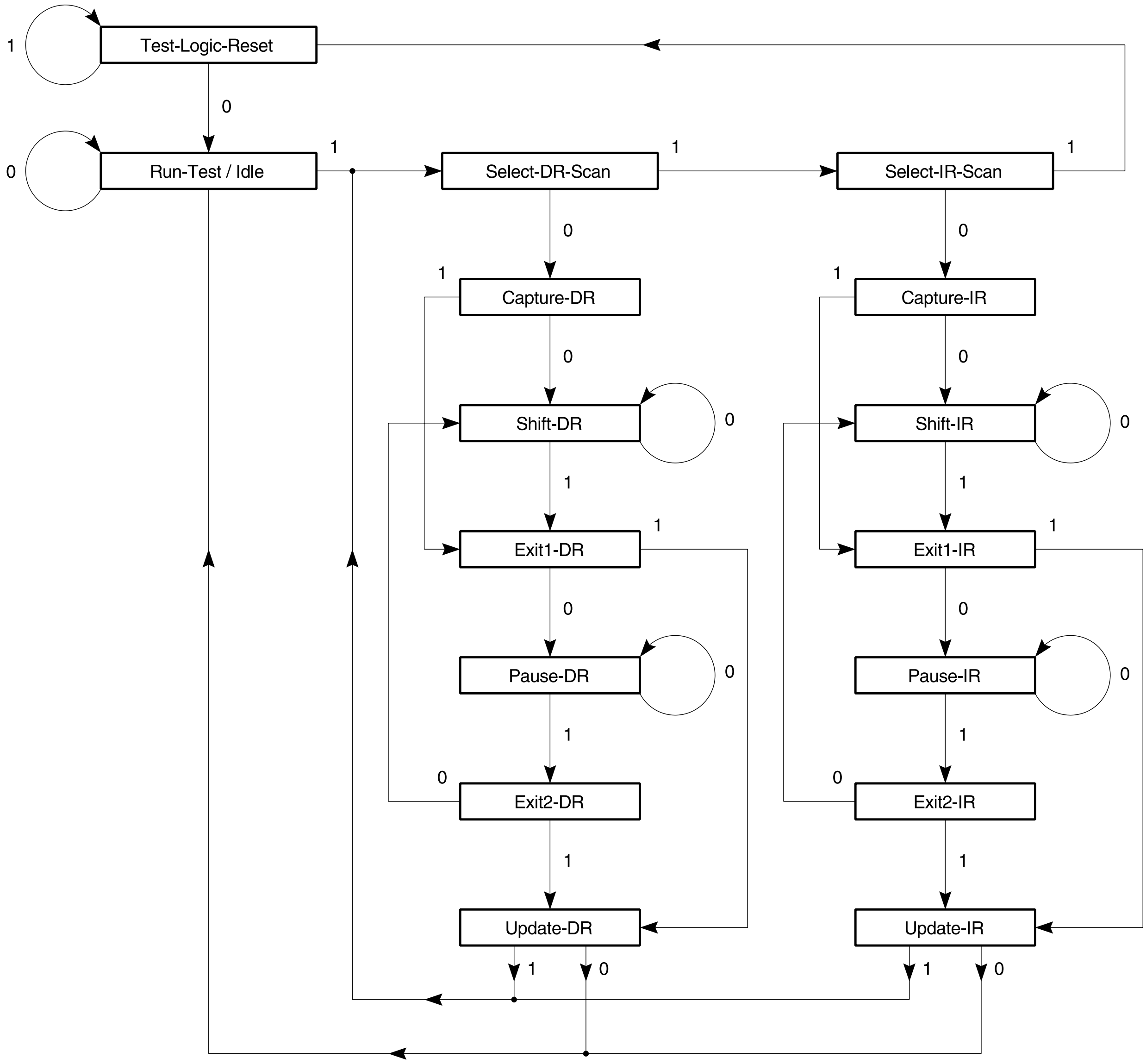
Instructions	Description
EXTEST	EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register, whatever length it may be in the device, is loaded with all logic 0s. EXTEST is not implemented in this device. Therefore this device is not 1149.1 compliant. Nevertheless, this RAMs TAP does respond to an all zeros instruction, as follows. With the EXTEST (000) instruction loaded in the instruction register the RAM responds just as it does in response to the SAMPLE instruction, except the RAM output are forced to high impedance any time the instruction is loaded.
IDCODE	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO pins in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test-logic-reset state.
BYPASS	The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.
SAMPLE	Sample is a Standard 1149.1 mandatory public instruction. When the sample instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable input will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO pins. This functionality is not Standard 1149.1 compliant.
SAMPLE-Z	If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (High impedance) and the boundary register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.

JTAG Instruction Cording

IR2	IR1	IR0	Instruction	Note
0	0	0	EXTEST	1
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	1
0	1	1	BYPASS	
1	0	0	SAMPLE	
1	0	1	BYPASS	
1	1	0	BYPASS	
1	1	1	BYPASS	

Note 1. TRISTATE all data drivers and CAPTURE the pad values into a SERIAL SCAN LATCH.

TAP Controller State Diagram



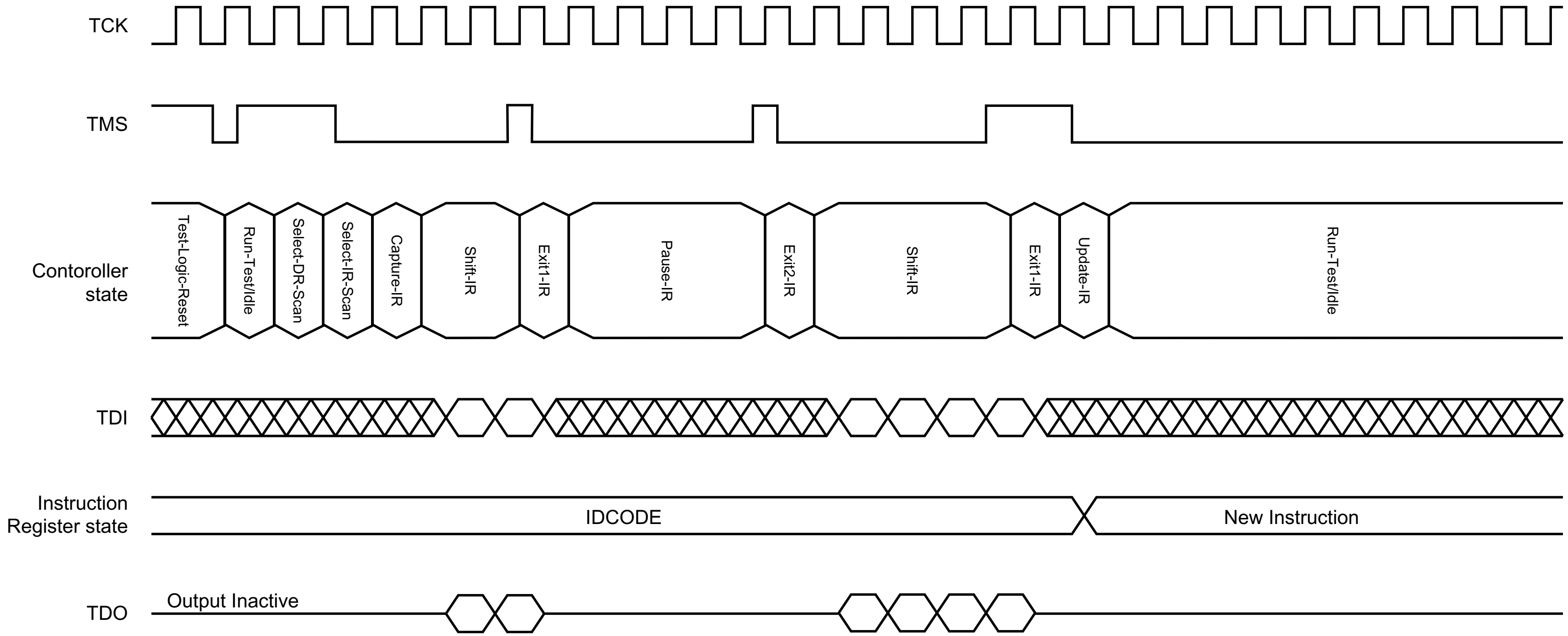
Disabling The Test Access Port

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs.

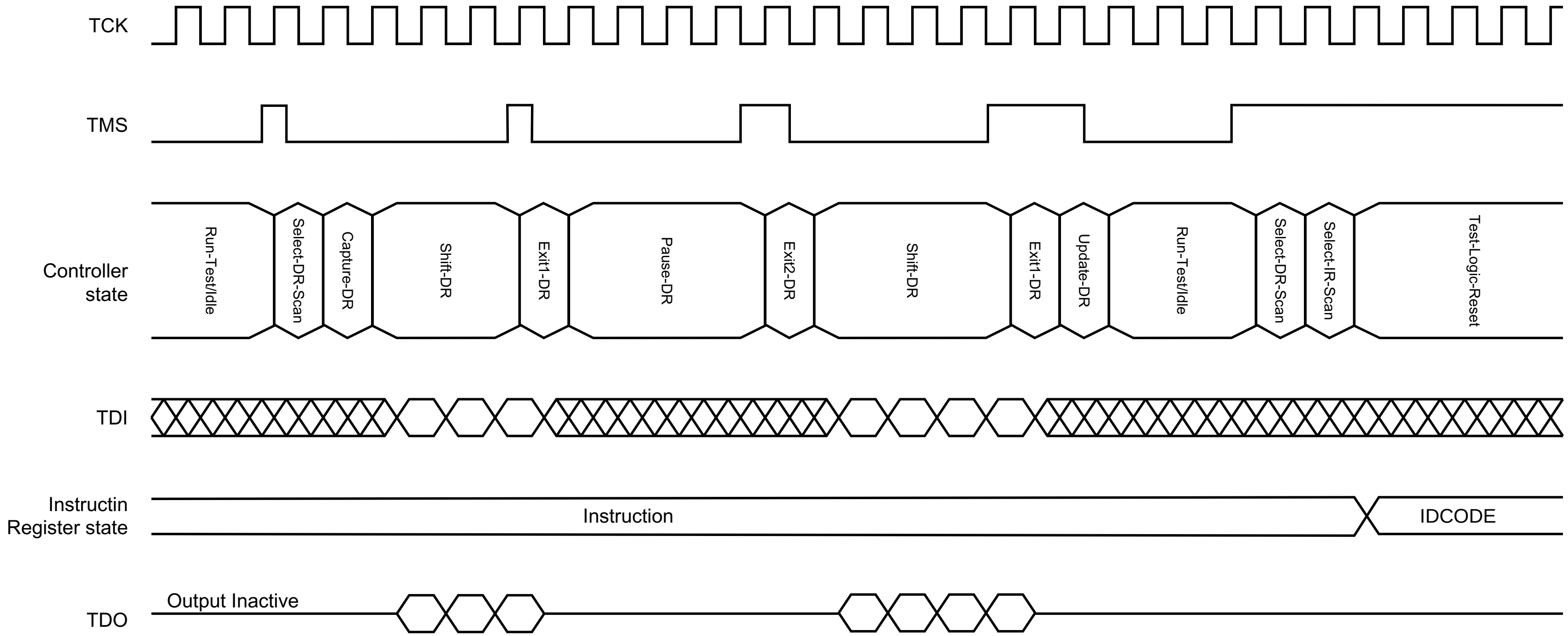
TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1 kΩ resistor.

TDO should be left unconnected.

Test Logic Operation (Instruction Scan)

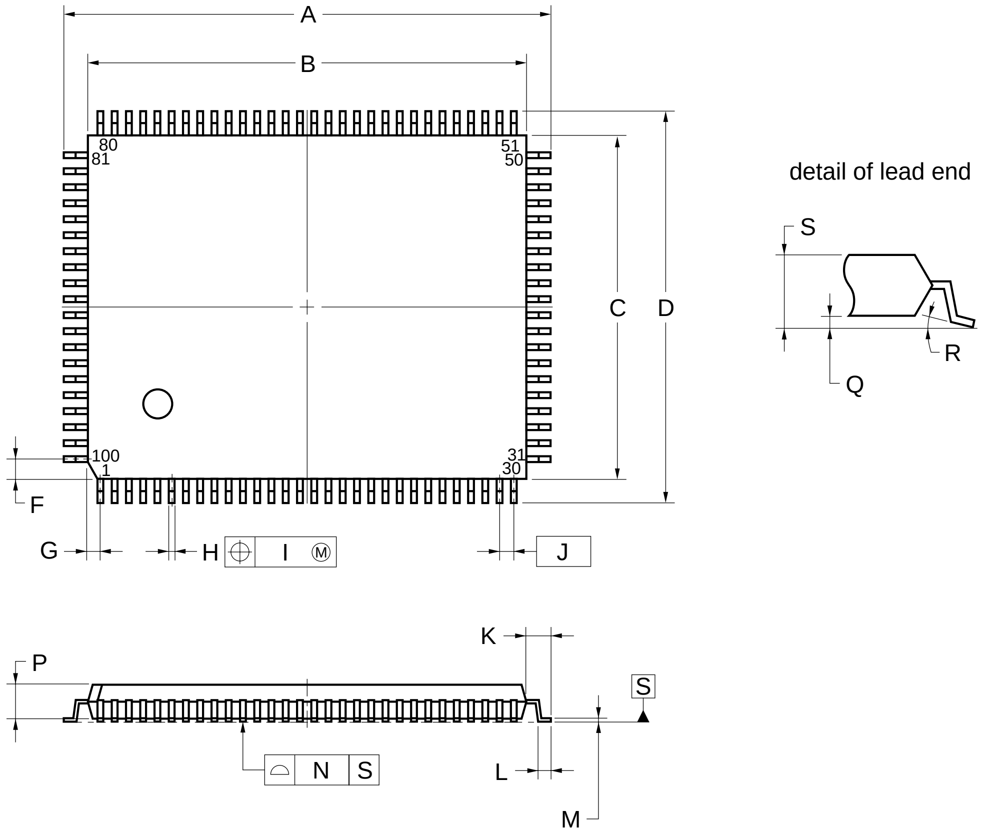


Test Logic (Data Scan)



Package Drawings

100-PIN PLASTIC LQFP (14x20)



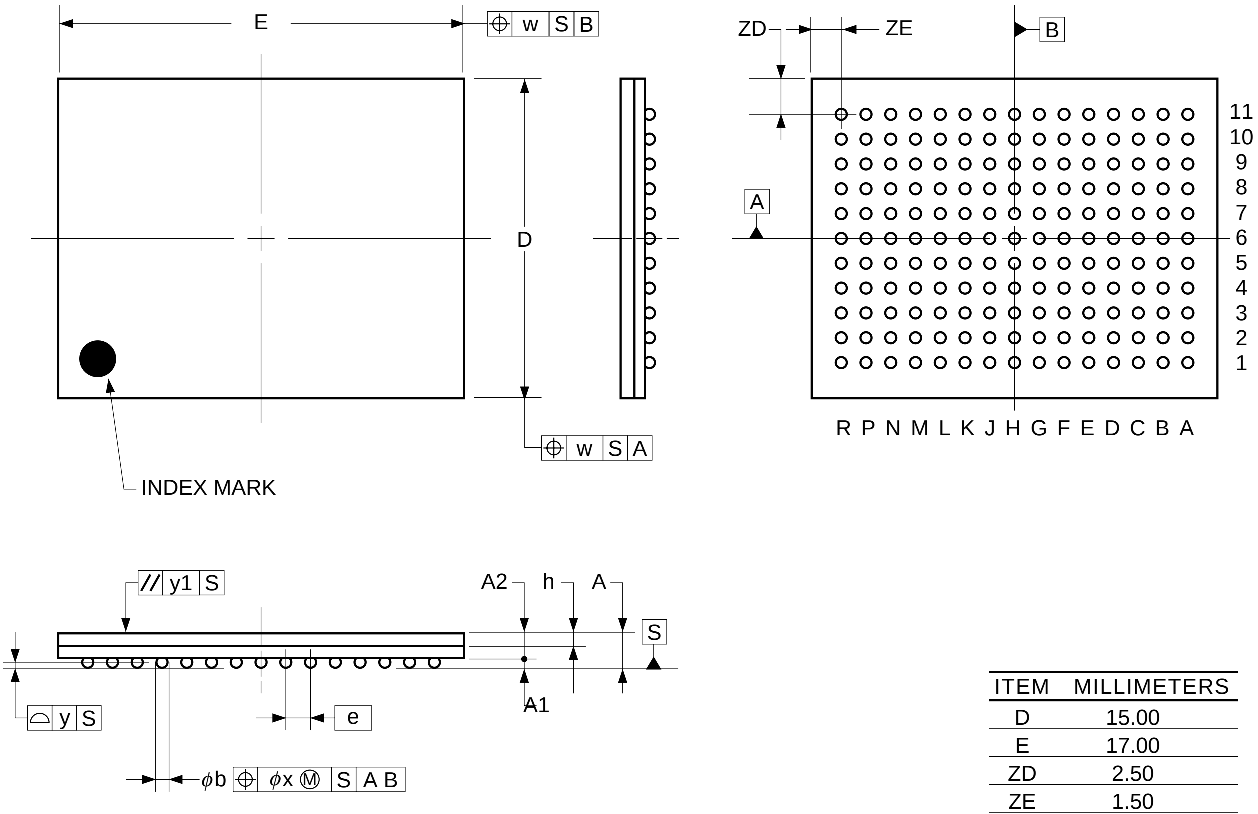
NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	14.0±0.2
D	16.0±0.2
F	0.825
G	0.575
H	$0.32^{+0.08}_{-0.07}$
I	0.13
J	0.65 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.17^{+0.06}_{-0.05}$
N	0.10
P	1.4
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.7 MAX.

S100GF-65-8ET-1

165-PIN PLASTIC FBGA (15x17)



ITEM	MILLIMETERS
D	15.00
E	17.00
ZD	2.50
ZE	1.50
e	1.00
h	0.60
A	1.40
A1	0.40
A2	1.00
b	0.45
y	0.08
x	0.08
w	0.15
y1	0.20

This package drawing is a preliminary version. It may be changed in the future.

Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of the μPD44321162, μPD44321182, μPD44321322 and μPD44321362.

Types of Surface Mount Devices

μPD44321162GF	: 100-pin PLASTIC LQFP (14 x 20)
μPD44321182GF	: 100-pin PLASTIC LQFP (14 x 20)
μPD44321322GF	: 100-pin PLASTIC LQFP (14 x 20)
μPD44321362GF	: 100-pin PLASTIC LQFP (14 x 20)
μPD44321162F1-FQ2	: 165-pin PLASTIC FBGA (15 x 17)
μPD44321182F1-FQ2	: 165-pin PLASTIC FBGA (15 x 17)
μPD44321322F1-FQ2	: 165-pin PLASTIC FBGA (15 x 17)
μPD44321362F1-FQ2	: 165-pin PLASTIC FBGA (15 x 17)

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.