DENSE-PAC MICROSYSTEMS

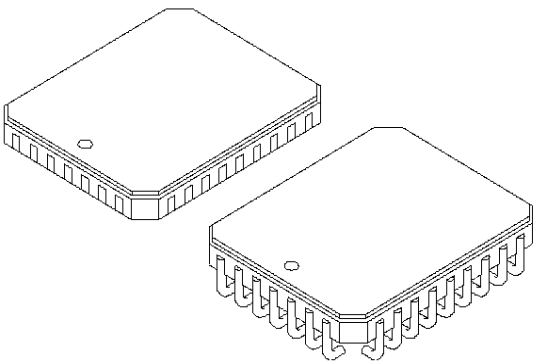
1 Megabit High Speed CMOS SRAM

DPS128M8En

DESCRIPTION:

The DPS128M8En is a very high speed 128K x 8 Static Random Access Memory (SRAM) fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5V power supply is required.

The DPS128M8En is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation and very high speed.



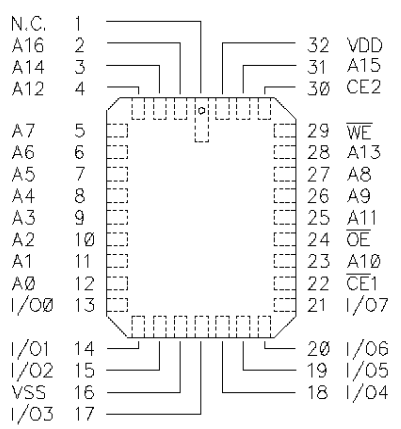
FEATURES:

- 131,072 Words by 8-Bits Organization
- Access Times: 15*, 17, 20, 25, 35ns (max.)
- Fully Static Operation;
  No Clock or Refresh Required
- TTL Compatible Input and Output
- Common Data Input and Output
- Single +5V Power Supply, ±10% Tolerance
- Three State Output
- Standard Packages:
  32-Pad Ceramic LCC
  32-Pin "J" Leaded Ceramic LCC

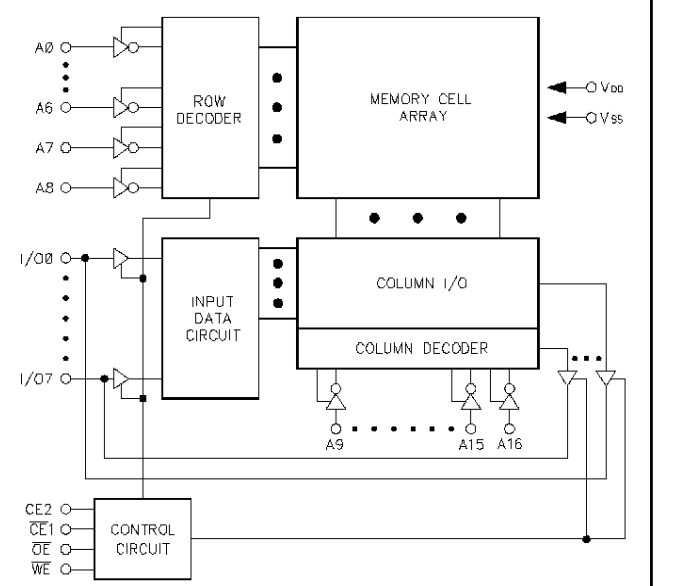
* Commercial Only

PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O7	Data In/Out
$\overline{CE}$1, CE2	Chip Enables
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

PIN-OUT DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING RANGE [3]						
Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage		2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage		-0.3[2]		0.8	V
T_A	Operating Temperature	M/B	-55	+25	+125	°C
		I	-40	+25	+85	
		C	0	+25	+70	

TRUTH TABLE						
Mode	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	H	X	X	X	High-Z	Standby
Not Selected	X	L	X	X	High-Z	Standby
D_{OUT} Disable	L	H	H	H	High-Z	Active
Read	L	H	H	L	D_{OUT}	Active
Write	L	H	L	X	D_{IN}	Active

H = HIGH L = LOW X = Don't Care

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH} = -4.0mA	2.4		V
V_{OL}	LOW Voltage	I_{OL} = 8.0mA		0.4	V

ABSOLUTE MAXIMUM RATINGS [3]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [1]	-0.5 to +7.0	°C
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD}+0.5	V

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	8	pF	V_{IN}[2] = 0V
C_{CE1}	Chip Enable	8		
C_{CE2}	Active High Chip Select	8		
C_{WE}	Write Enable	8		
C_{OE}	Output Enable	8		
$C_{I/O}$	Data Input/Output	10		

DC OPERATING CHARACTERISTICS: Over operating ranges										
Symbol	Characteristics	Test Conditions	Typ. (†)	C		I		M/B		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-	-5	+5	-5	+5	-5	+5	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE1}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-	-5	+5	-5	+5	-5	+5	µA
I_{CC}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA	180		200		220		220	mA
I_{SB1}	Full Standby Supply Current	$V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ +0.2V	0.4		5		5		10	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE1}$ = V_{IH}, or CE2 = V_{IL}, f = f max.	30		35		40		40	mA
I_{DR3}	Data Retention Supply Current (3.0V)	V_{DR} = 3.0V, $\overline{CE1} \geq V_{DR}$ -0.2V, CE2 ≤ 0.2V, $V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq$ +0.2V	100		150		350		1200	µA
I_{DR2}	Data Retention Supply Current (2.0V)	V_{DR} = 2.0V, $\overline{CE1} \geq V_{DR}$ -0.2V, CE2 ≤ 0.2V, $V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq$ +0.2V	70		150		250		1000	µA
V_{OL}	Output Low Voltage	I_{OUT} = 8.0mA	-		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -4.0mA	-	2.4		2.4		2.4		V

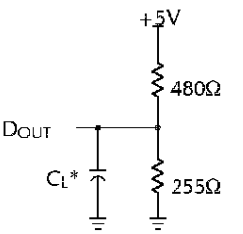
† Typical measurements made at +25°C, Cycle = min., V_{DD} = 5.0V.

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD		
Load	**C_L**	**Parameters Measured**
1	30pF	except t_{LZ1}, t_{LZ2}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OLZ}, and t_{WHZ}
2	5pF	t_{LZ1}, t_{LZ2}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OLZ}, and t_{WHZ}

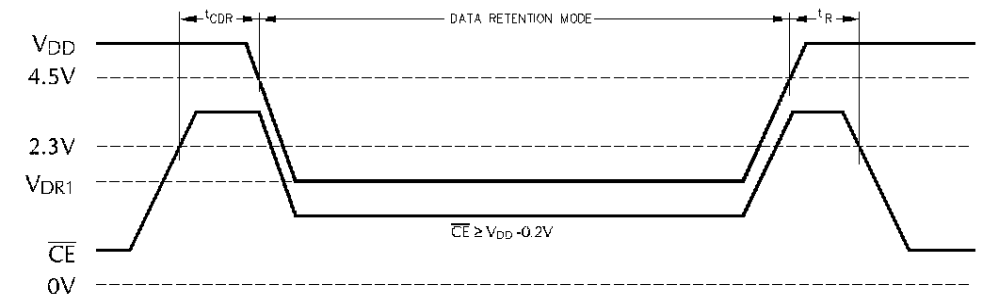
Figure 1. Output Load

* Including Probe and Jig Capacitance.

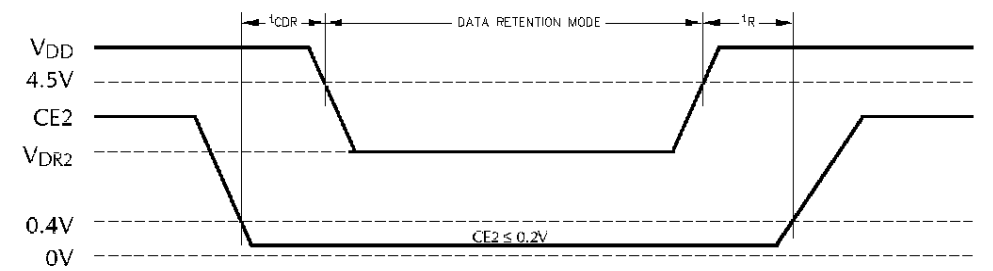


Data Retention AC Characteristics [8]						
Symbol	**Parameter**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{DR}	V_{DD} for Data Retention	$\overline{CE} \geq V_{DR}$ -0.2V, CE2 ≤ 0.2V, $V_{IN} \geq V_{DR}$ -0.2V or $V_{IN} \leq 0.2V$	2.0	-	-	V
V_{CDR}	Chip Disable to Data Retention Time	See Data Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time	See Data Retention Waveform	5	-	-	ms

DATA RETENTION WAVEFORM: $\overline{CE}$1 Controlled.



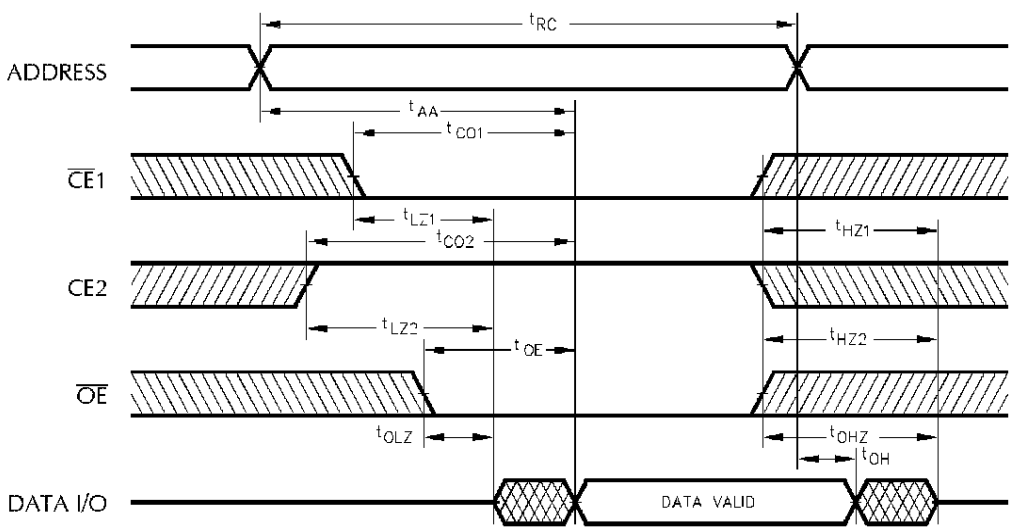
DATA RETENTION WAVEFORM: CE2 Controlled.



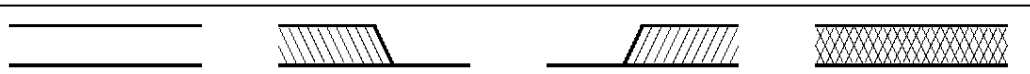
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	15ns*		17ns		20ns		25ns		35ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	15		17		20		25		35		ns
2	t_{AA}	Address Access Time		15		17		20		25		35	ns
3	t_{CO1}	$\overline{CE}1$ to Output Valid		15		17		20		25		35	ns
4	t_{CO2}	CE2 to Output Valid		15		17		20		25		35	ns
5	t_{OE}	Output Enable to Output Valid		6		6		8		10		12	ns
6	t_{LZ1}	$\overline{CE}1$ to Output in LOW-Z [4, 5]	3		3		3		3		3		ns
7	t_{LZ2}	CE2 to Output in LOW-Z [4, 5]	3		3		3		3		3		ns
8	t_{OLZ}	Output Enable to Output in LOW-Z [4, 5]	3		3		3		3		3		ns
9	t_{HZ1}	$\overline{CE}1$ to Output in HIGH-Z [4, 5]		8		8		10		12		15	ns
10	t_{HZ2}	CE2 to Output in HIGH-Z [4, 5]		8		8		10		12		15	ns
11	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 5]		6		6		8		10		12	ns
12	t_{OH}	Output Hold from Address Change	3		3		3		3		3		ns

* Available in Commercial Only.

READ CYCLE



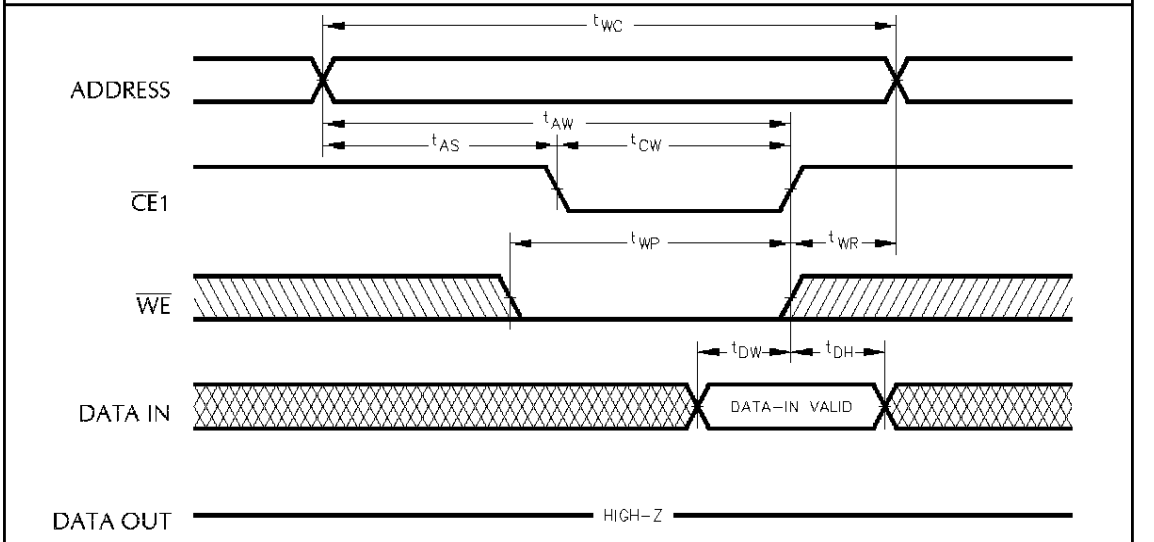
WAVEFORM KEY



AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE [6, 7]: Over operating ranges													
No.	Symbol	Parameter	15ns*		17ns		20ns		25ns		35ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
13	t_{WC}	Write Cycle Time	15		17		20		25		35		ns
14	t_{AW}	Address Valid to End of Write	12		12		15		20		30		ns
15	t_{CW}	Chip Enable to End of Write	12		12		15		20		30		ns
16	t_{AS}	Address Set-Up Time **	0		0		0		0		0		ns
17	t_{WP}	Write Pulse Width	12		12		15		20		35		ns
18	t_{WR}	Write Recovery Time, $\overline{CE1}$, CE2, $\overline{WE}$	0		0		0		0		0		ns
19	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 5]		8		8		10		12		15	ns
20	t_{DW}	Data to Write Time Overlap	7		7		8		10		12		ns
21	t_{DH}	Data Hold from Write Time	0		0		0		0		0		ns
22	t_{OW}	Output Active from End of Write	3		3		3		3		3		ns

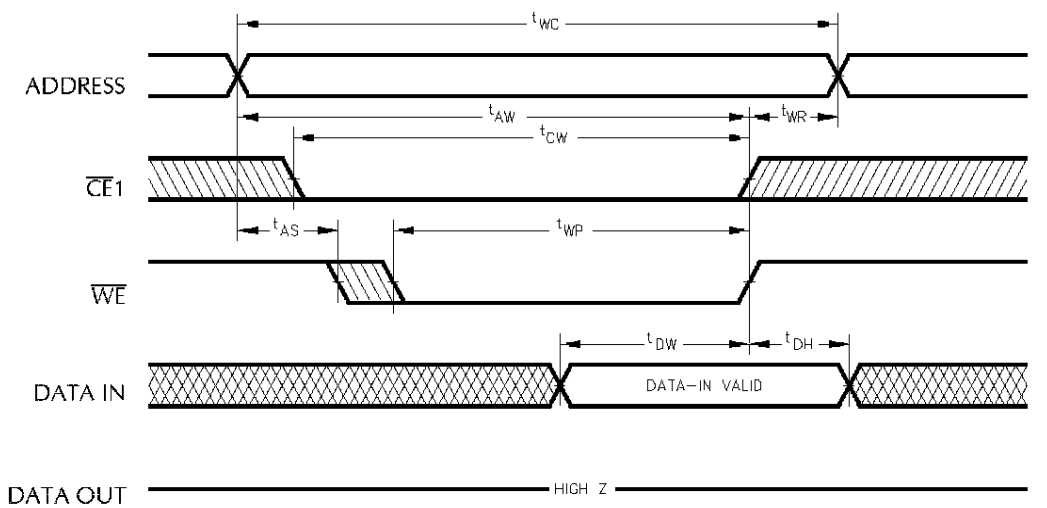
* Available in Commercial Only.
** Valid for both Read and Write Cycles.

WRITE CYCLE 1: $\overline{CE}$ Controlled. [8]

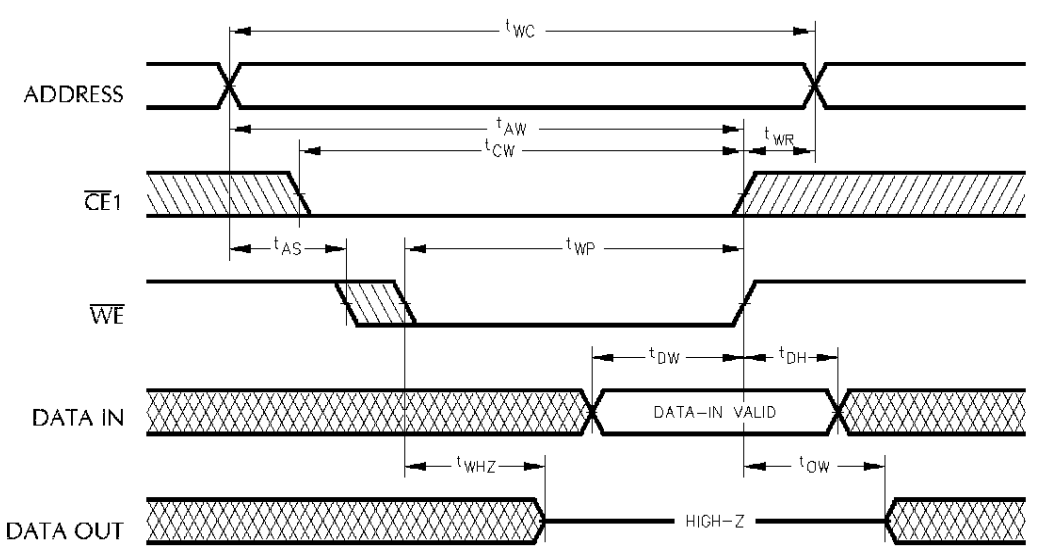


NOTES:
1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE1}$ are LOW and CE2 and $\overline{WE}$ are HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.
8. CE2 timing is the same as $\overline{CE1}$ timing. The Waveform is inverted.
9. Chip Enable and Write Enable can initiate and terminate WRITE Cycle.

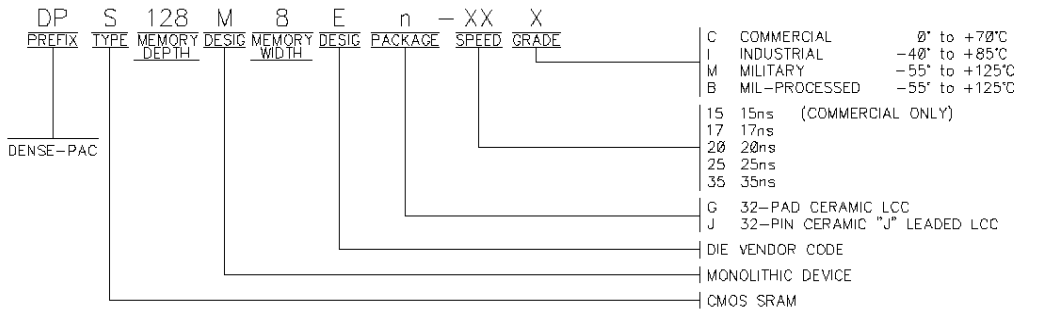
WRITE CYCLE 2: $\overline{WE}$ Controlled. $\overline{OE}$ is HIGH. [8, 9]



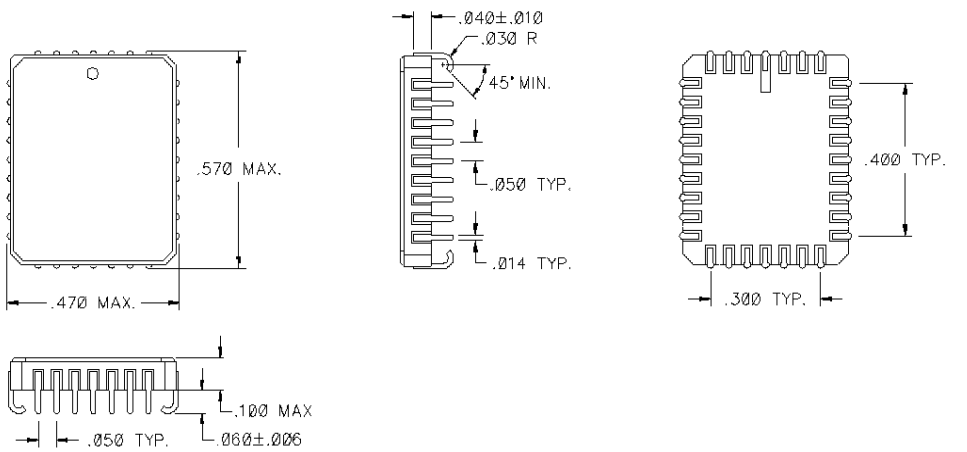
WRITE CYCLE 3: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW. [8, 9]



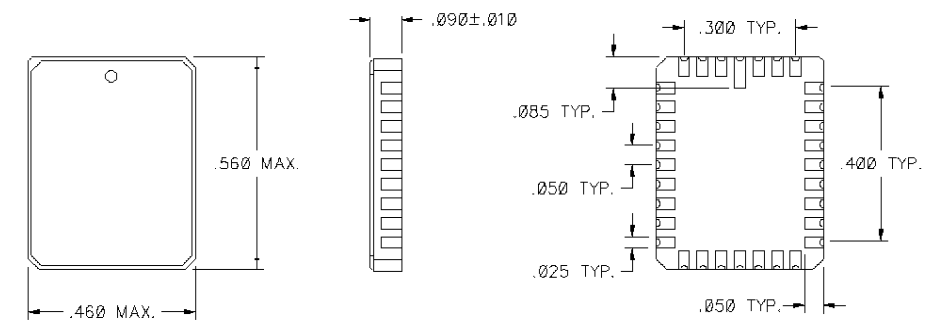
ORDERING INFORMATION



"J" LEADED LCC MECHANICAL DRAWING



LCC MECHANICAL DRAWING



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