HM66WP18100/HM66WP36512

18M Pipelined Zero Bus Latency (ZBL) SRAM
(HM66WP18100) 1-Mword × 18-bit
(HM66WP36512) 512-Kword × 36-bit

HITACHI

ADE-203-1298C (Z)
Preliminary
Rev. 0.3
Mar. 29, 2002

Description

The HM66WP18100 is a synchronous fast static RAM organized as 1-Mword × 18-bit. The HM66WP36512 is a synchronous fast static RAM organized as 512-Kword × 36-bit. It has realized high speed access time by employing the most advanced CMOS process and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. It is packaged in standard 100-pin LQFP and 119-pin BGA.

Note : All power supply(V_{DD},V_{DDQ}) and ground(V_{SS}) pins must be connected for proper operation of the device.

ZBL : Zero Bus Latency and compatible ZBT™ SRAM. ZBT™ is trademark of Integrated Device Technology, Inc.,

Features

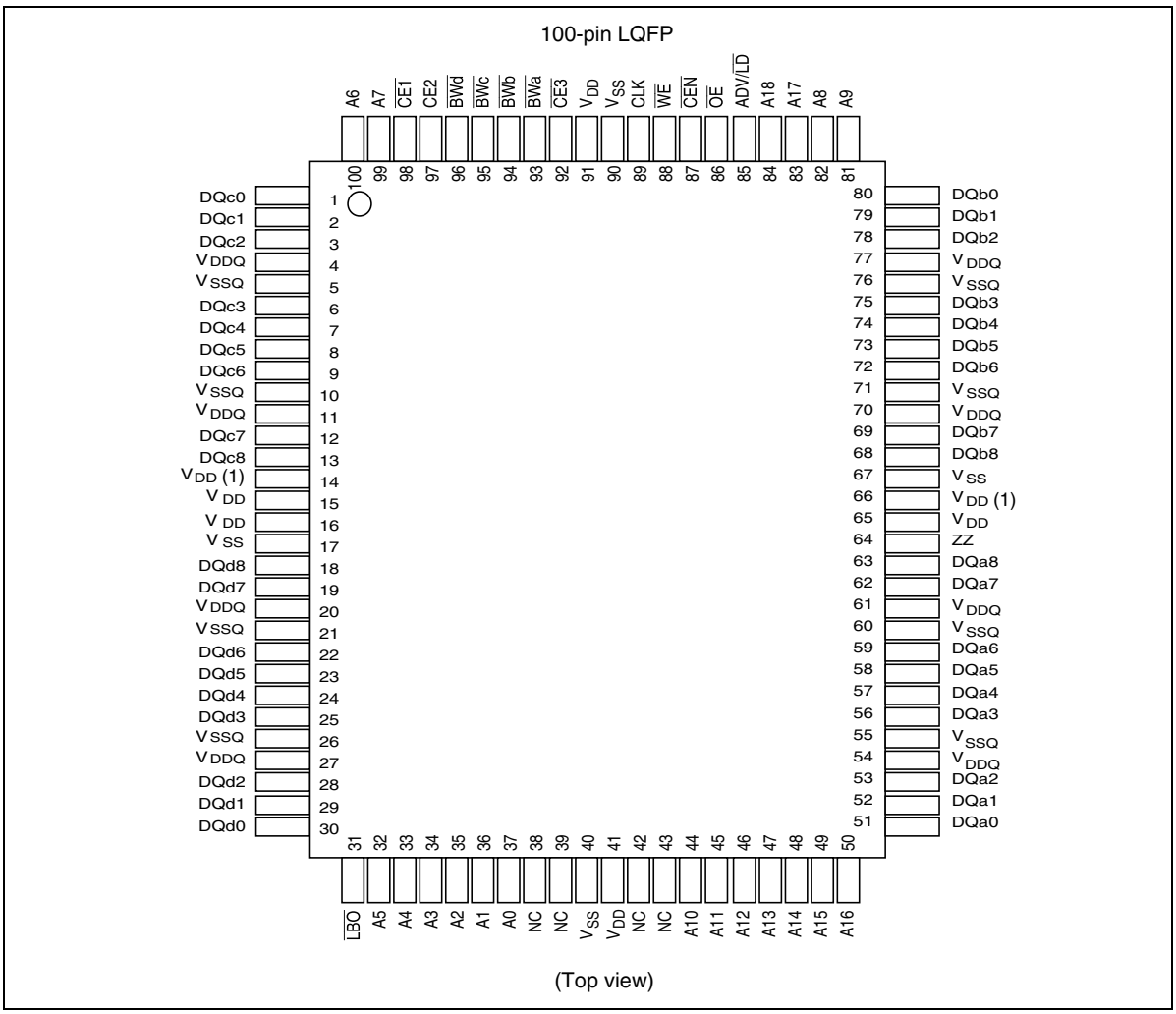
- 3.3 V or 2.5V power supply, 3.3 V or 2.5 V I/O supply voltage
- Clock frequency: 250/200/166 MHz
- Fast clock access time: 2.6/3.0/3.5 ns (max)
- Low operating current: 300/250/220 mA (max)
- Address data pipeline capability
- Internal input registers (Address, Data, Control)
- Internal self-timed write cycle
- ADV/$\overline{LD}$ burst control pins
- Internally synchronized registered outputs eliminate the need to control $\overline{OE}$
- Individual byte write control
- Power down state via ZZ
- Common data inputs and data outputs
- High board density 100-pin LQFP package and 119-pin BGA package
- Burst contorol selected pin $\overline{LBO}$ (Interleave or linear burst oder)

Hitachi semiconductor

Ordering Information

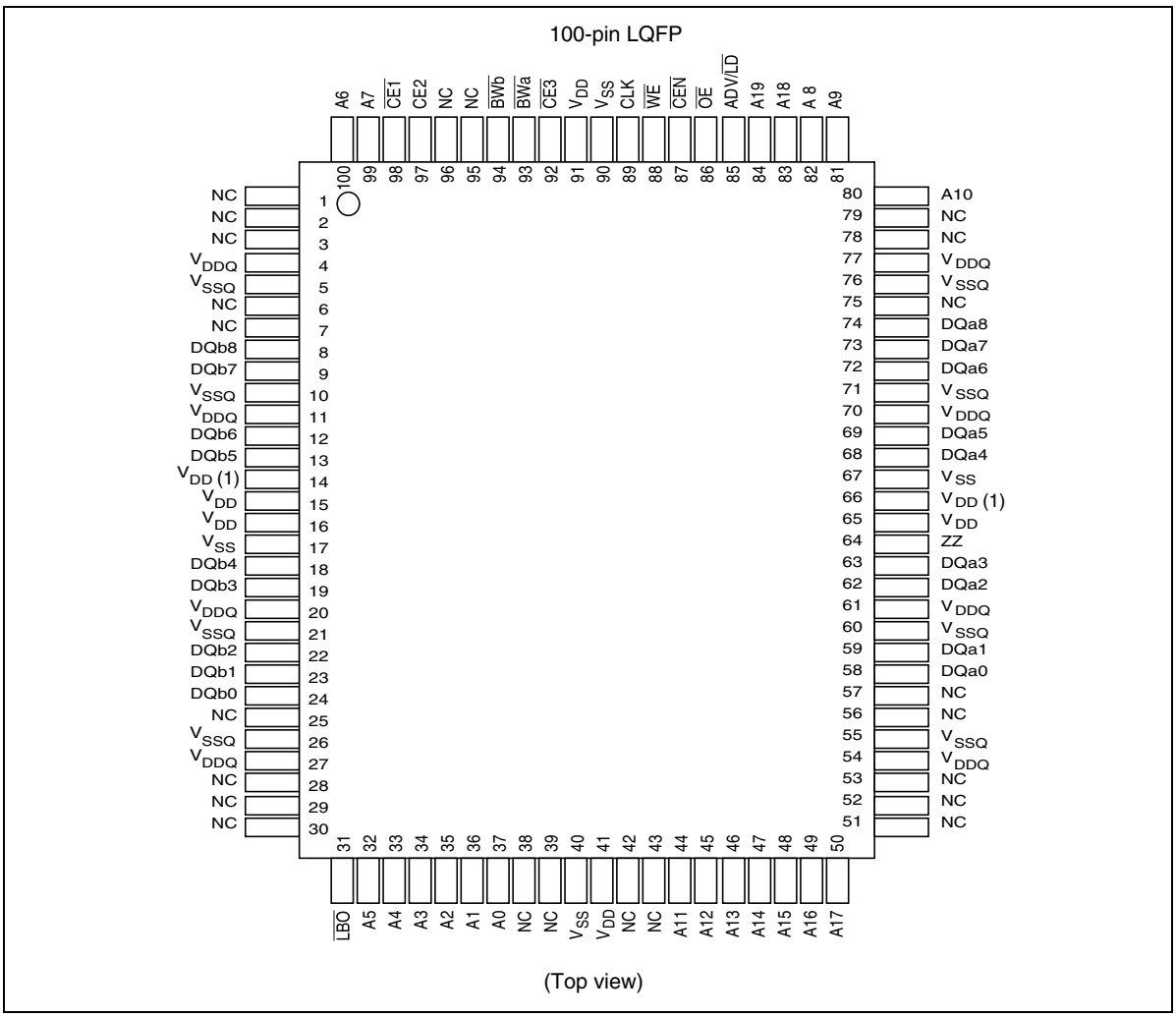
Type No.	Access time	CPU clock rate	Package
HM66WP18100FP-40	2.6 ns	250 MHz	LQFP 100-pin (FP-100H)
HM66WP18100FP-50	3.0 ns	200 MHz	
HM66WP18100FP-60	3.5 ns	166 MHz	
HM66WP36512FP-40	2.6 ns	250 MHz	
HM66WP36512FP-50	3.0 ns	200 MHz	
HM66WP36512FP-60	3.5 ns	166 MHz	
HM66WP18100BP-40	2.6 ns	250 MHz	BGA 119-pin (BP-119A)
HM66WP18100BP-50	3.0 ns	200 MHz	
HM66WP18100BP-60	3.5 ns	166 MHz	
HM66WP36512BP-40	2.6 ns	250 MHz	
HM66WP36512BP-50	3.0 ns	200 MHz	
HM66WP36512BP-60	3.5 ns	166 MHz	

Pin Arrangement (HM66WP36512) 100PIN-LQFP



Note : Pins 14 and 66 are not V_{DD} Supply ,but have to be connected V_{DD} or > V_{IH}.

Pin Arrangement (HM66WP18100) 100PIN-LQFP



Note : Pins 14 and 66 are not V_{DD} Supply ,but have to be connected V_{DD} or > V_{IH}.

Pin Arrangement (HM66WP36512) 119PIN-BGA

	1	2	3	4	5	6	7
A	V_{DDQ}	A6	A4	A18	A8	A16	V_{DDQ}
B	NC	CE2	A3	ADV/$\overline{LD}$	A9	$\overline{CE3}$	NC
C	NC	A7	A2	V_{DD}	A12	A15	NC
D	DQc1	DQc0	V_{SS}	NC	V_{SS}	DQb0	DQb1
E	DQc3	DQc2	V_{SS}	$\overline{CE1}$	V_{SS}	DQb2	DQb3
F	V_{DDQ}	DQc4	V_{SS}	$\overline{OE}$	V_{SS}	DQb4	V_{DDQ}
G	DQc6	DQc5	$\overline{BWc}$	A17	$\overline{BWb}$	DQb5	DQb6
H	DQc8	DQc7	V_{SS}	$\overline{WE}$	V_{SS}	DQb7	DQb8
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd8	DQd7	V_{SS}	CLK	V_{SS}	DQa7	DQa8
L	DQd6	DQd5	$\overline{BWd}$	NC	$\overline{BWa}$	DQa5	DQa6
M	V_{DDQ}	DQd4	V_{SS}	$\overline{CEN}$	V_{SS}	DQa4	V_{DDQ}
N	DQd3	DQd2	V_{SS}	A1	V_{SS}	DQa2	DQa3
P	DQd1	DQd0	V_{SS}	A0	V_{SS}	DQa0	DQa1
R	NC	A5	$\overline{LBO}$	V_{DD}	NC	A13	NC
T	NC	NC	A10	A11	A14	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

(Top view)

Pin Arrangement (HM66WP18100) 119PIN-BGA

	1	2	3	4	5	6	7
A	V_{DDQ}	A6	A4	A19	A8	A16	V_{DDQ}
B	NC	CE2	A3	ADV/$\overline{LD}$	A9	$\overline{CE3}$	NC
C	NC	A7	A2	V_{DD}	A13	A17	NC
D	DQb8	NC	V_{SS}	NC	V_{SS}	DQa8	NC
E	NC	DQb7	V_{SS}	$\overline{CE1}$	V_{SS}	NC	DQa7
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQa6	V_{DDQ}
G	NC	DQb6	$\overline{BWb}$	A18	V_{SS}	NC	DQa5
H	DQb5	NC	V_{SS}	$\overline{WE}$	V_{SS}	DQa4	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQb4	V_{SS}	CLK	V_{SS}	NC	DQa3
L	DQb3	NC	V_{SS}	NC	$\overline{BWa}$	DQa2	NC
M	V_{DDQ}	DQb2	V_{SS}	$\overline{CEN}$	V_{SS}	NC	V_{DDQ}
N	DQb1	NC	V_{SS}	A1	V_{SS}	DQa1	NC
P	NC	DQb0	V_{SS}	A0	V_{SS}	NC	DQa0
R	NC	A5	$\overline{LBO}$	V_{DD}	NC	A12	NC
T	NC	A10	A15	NC	A14	A11	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

(Top view)

Note: Pin 3L and 5G are not V_{ss} Supply, but have to be connected V_{ss} or have to be NC.

Pin Description (See Detailed Pin Description)

Name	I/O type	Description	Notes
A0 ,A1 and A2-18 (HM66WP36512)	Input	19 address inputs	
A0 ,A1 and A2-19 (HM66WP18100)	Input	20 address inputs	
$\overline{BWm}$	Input	Byte write enables $\overline{BWa}$ controls DQa0 to DQa8 $\overline{BWb}$ controls DQb0 to DQb8 $\overline{BWc}$ controls DQc0 to DQc8 $\overline{BWd}$ controls DQd0 to DQd8	m = a, b, c, d (HM66WP36512) m = a, b (HM66WP18100)
$\overline{WE}$	Input	Write enable	
CLK	Input	Clock	
$\overline{CE1}$, $\overline{CE3}$, CE2	Input	Chip enable	
$\overline{OE}$	Input	Output enable	
ADV/$\overline{LD}$	Input	Address load control	
$\overline{CEN}$	Input	Clock enable control	
ZZ	Input	Power down	
$\overline{LBO}$	Input	Burst mode control	
NC	—	No connection	
DQmn n = 0 – 8	Input/Output	Data input/output	m = a, b, c, d (HM66WP36512) m = a, b (HM66WP18100)
V_{DD}	Supply	Power supply	
V_{DDQ}	Supply	I/O power supply	
V_{SS}	Supply	Ground	

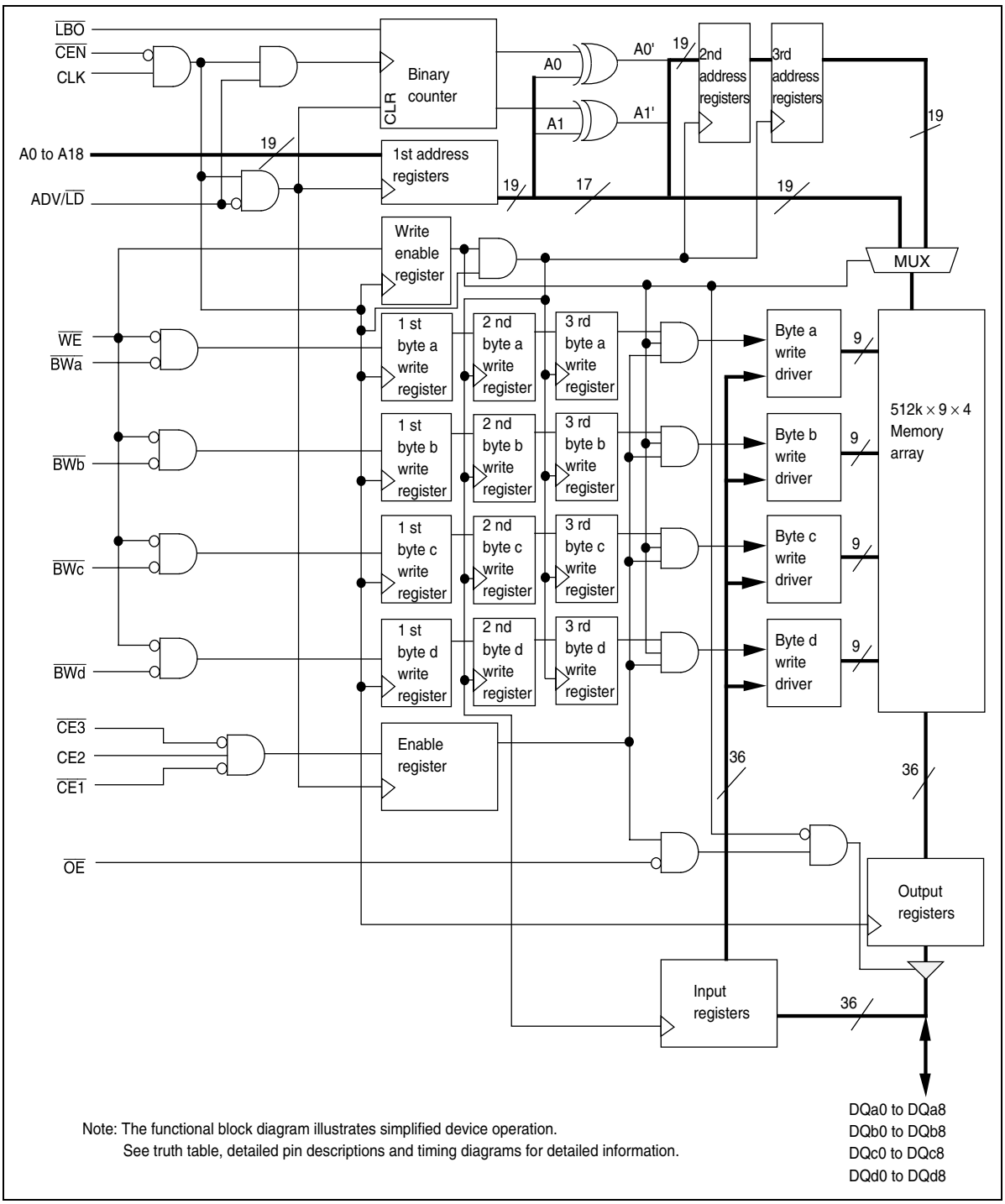
Detailed Pin Description

Pin number(s)		Symbol	Type	Description
LQFP	**BGA**			
35, 34, 33, 32, 44, 45, 46, 47, 48,49,50,81,82, 83,84,99, 100	2A, 2C, 2R, 3A, 3B, 3C, 3T, 4G, 5A, 5B, 5C, 5T, 6A, 6C, 6R, 4A	A (× 36-bit × 18-bit common)	Input	Synchronous address inputs: These inputs are registered and must meet setup and hold times around the rising edge of CLK.
37, 36	4P, 4N	A0,A1		Burst address inputs
80	2T, 6T 4T	A (× 18-bit)A (× 36-bit)		
93, 94, 95, 96	5L, 5G, 3G, 3L	$\overline{BWa}$, $\overline{BWb}$ $\overline{BWc}$, $\overline{BWd}$ (× 36-bit)	Input	Synchronous byte write enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BWa}$ controls DQa0 to DQa8. $\overline{BWb}$ controls DQb0 to DQb8. $\overline{BWc}$ controls DQc0 to DQc8. $\overline{BWd}$ controls DQd0 to DQd8. Data I/O are tristated if any of these four inputs are LOW.
93, 94	5L, 3G	$\overline{BWa}$, $\overline{BWb}$ (× 18-bit)		
87	4M	$\overline{CEN}$	Input	Synchronous clock enable: This active LOW internal clock signal is active.
88	4H	$\overline{WE}$	Input	Synchronous write enable: This active LOW input permits write operations and must meet the setup and hold times around the rising edge of CLK.
89	4K	CLK	Input	Clock: This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	4E	$\overline{CE1}$	Input	Synchronous chip enable: This active LOW input is used to enable the device. This input is sampled only when a external address is loaded. This input can be used for memory depth expansion.
92	6B	$\overline{CE3}$	Input	
97	2B	CE2	Input	Synchronous chip enable: This active HIGH input is used to enable the device. This input sampled only when a new external address is load. This input can be used for memory depth expansion.
86	4F	$\overline{OE}$	Input	Output enable: This active LOW asynchronous input enables the data I/O output drivers.
85	4B	ADV/$\overline{LD}$	Input	Synchronous address advance or load control: This active HIGH input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A LOW input is caused a new external address to be latched.

Detailed Pin Description (cont)

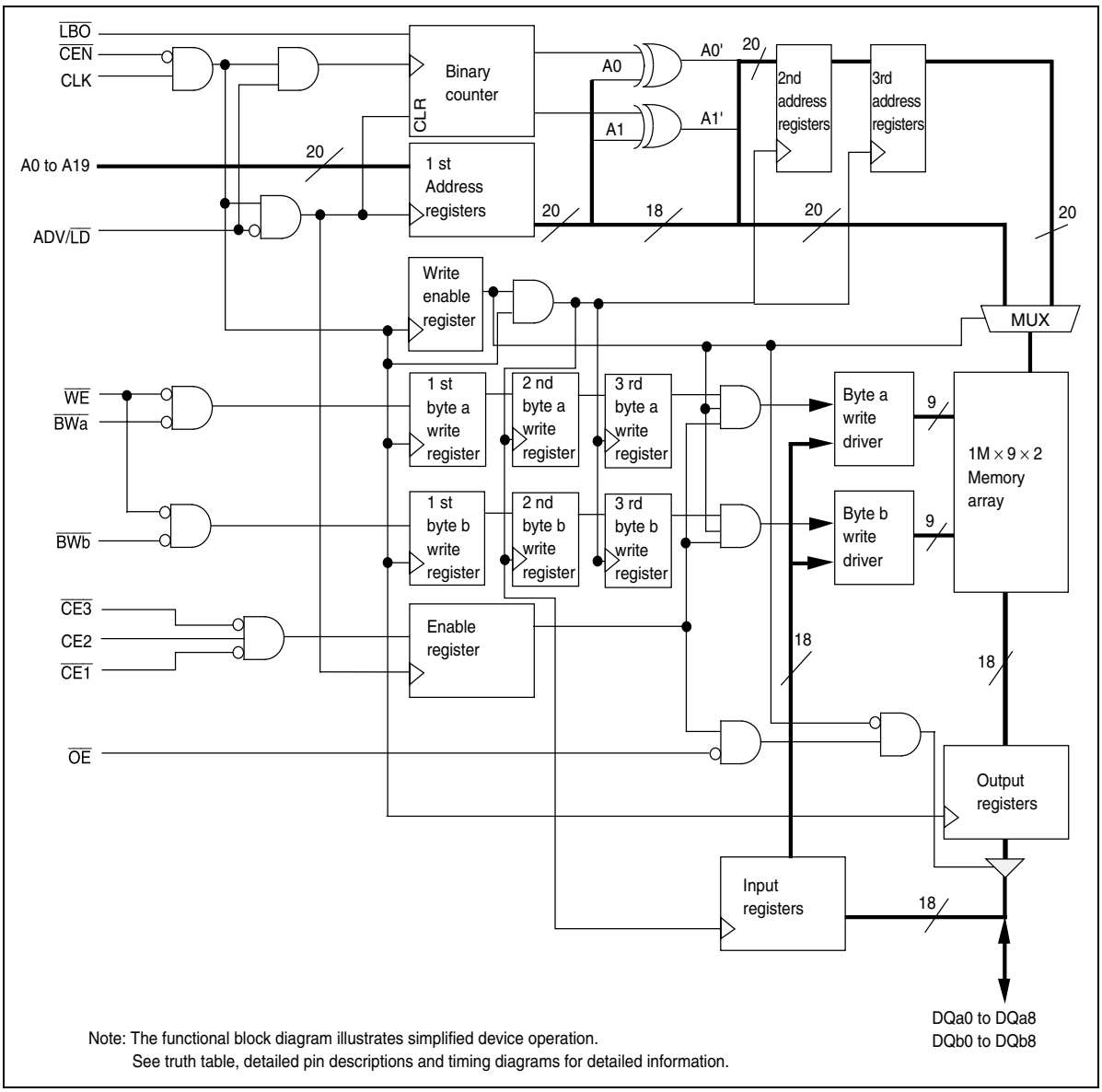
Pin number(s)		Symbol	Type	Description
LQFP	BGA			
38, 39, 42, 43,	1B, 1C, 1R, 1T, 3J, 4D, 4L,5J,5R,6T,6U,7B,7C,7R	NC (× 36-bit)	—	No Connect: These signals are internally not connected.
1, 2, 3, 6, 7, 25, 28, 29, 30, 38, 39, 42, 43, 51, 52, 53, 56, 57, 75, 78, 79, 95, 96	1B, 1C, 1E, 1G, 1K, 1P, 1R, 1T,2D,2F,2H,2L,2N,4L, 4T,5J,5R,6E,6G,6K,6M,6P, 6U,7B,7C,7D,7H,7L,7N,7R	NC (× 18-bit)	—	No Connect: These signals are internally not connected.
51, 52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 80, 1, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29, 30	6K, 6L, 6M, 6N, 6P, 7K, 7L, 7N, 7P, 6D, 6E, 6F, 6G, 6H, 7D, 7E, 7G, 7H, 1D, 1E, 1G, 1H, 2D, 2E 2F, 2G, 2H, 1K, 1L, 1N 1P,2K , 2L, 2M, 2N, 2P	DQmn m = a, b, c, d n = 0 – 8 (× 36-bit)	Input/ Output	SRAM data I/O: Byte a is DQa0 to DQa8; Byte b is DQb0 to DQb8; Byte c is DQc0 to DQc8; Byte d is DQd0 to DQd8. Input data must meet setup and hold times around the rising edge of CLK.
58, 59, 62, 63, 68, 69, 72, 73, 74, 8, 9, 12, 13, 18, 19, 22, 23, 24	6D, 6F, 6H, 6L, 6N, 7E, 7G, 7K, 7P, 1D, 1H, 1L, 1N, 1E, 1G, 1K, 1M, 1P	DQmn m = a, b n = 0 – 8 (× 18-bit)	Input/ Output	SRAM data I/O: Byte a is DQa0 to DQa8; Byte b is DQb0 to DQb8. Input data must meet setup and hold times around the rising edge of CLK.
14, 15, 16, 41, 65, 66, 91	2J, 4C, 4J, 4R, 6J,	V_{DD}	Supply	Power supply: 3.3 V (+5%/–5%) or 2.5 V (+5%/–5%)
4, 11, 20, 27, 54 61, 70, 77	1A, 1F, 1J, 1M, 1U, 7A, 7F, 7J, 7M, 7U	V_{DDQ}	Supply	I/O power supply: 3.3 V (+5%/–5%) or 2.5 V (+5%/–5%)
17, 40, 67, 90, 5, 10, 21, 26, 55, 60, 71, 76	3D,3E,3F,3H,3K,3M,3N,3P, 5D,5E,5F,5H,5K,5M,5N,5P	V_{SS}	Supply	Ground: GND
	3L, 5G	V_{SS} (× 18-bit)	Supply	Ground: GND
64	7T	ZZ	Input	Asynchronous power-down (Snooze): This active HIGH input enables SRAM to enter a power-down (Snooze) state with data retention. During Snooze state, data retention is guaranteed. At this time, internal state of the SRAM is not preserved. After Snooze state, SRAM must be initiated with $\overline{CEN}$ or ADV/$\overline{LD}$ using a new external address. This pin must be connected to V_{SS} in systems that do not use ZZ feature.
31	3R	$\overline{LBO}$	Input	Burst order (Interleave burst or linear burst) select pin (DC) This pin must connect V_{DD} or V_{DDQ} or V_{SS}.

Block Diagram (HM66WP36512)



Note: The functional block diagram illustrates simplified device operation.
See truth table, detailed pin descriptions and timing diagrams for detailed information.

Block Diagram (HM66WP18100)



Note: The functional block diagram illustrates simplified device operation.
See truth table, detailed pin descriptions and timing diagrams for detailed information.

Synchronous Truth Table

Operation	Address	$\overline{CE1}$	$\overline{CE3}$	CE2	ADV/$\overline{LD}$	$\overline{CEN}$	$\overline{WE}$	$B\overline{Wm}$	$\overline{OE}$	CLK	DQ
Deselected cycle, power-down	None	H	×	×	L	L	×	×	×	L-H	High-Z
Deselected cycle, power-down	None	×	H	×	L	L	×	×	×	L-H	High-Z
Deselected cycle, power-down	None	×	×	L	L	L	×	×	×	L-H	High-Z
WRITE cycle, begin burst	External	L	L	H	L	L	L	L	×	L-H	D
NOP/WRITE Abort, begin burst	External	L	L	H	L	L	L	H	×	L-H	High-Z
READ cycle, begin burst	External	L	L	H	L	L	H	×	L	L-H	Q
Dummy READ cycle, begin burst	External	L	L	H	L	L	H	×	H	L-H	High-Z
WRITE cycle, continue burst	Next	×	×	×	H	L	×	L	×	L-H	D
WRITE Abort, continue burst	Next	×	×	×	H	L	×	H	×	L-H	High-Z
READ cycle, continue burst	Next	×	×	×	H	L	×	×	L	L-H	Q
Dummy READ cycle, continue burst	Next	×	×	×	H	L	×	×	H	L-H	High-Z
WRITE cycle, suspend	Current	×	×	×	×	H	×	×	×	L-H	-
READ cycle, suspend	Current	×	×	×	×	H	×	×	L	L-H	Q
Dummy READ cycle, suspend	Current	×	×	×	×	H	×	×	H	L-H	High-Z

Notes: 1. H means logic HIGH, L means logic LOW. × means H or L. $\overline{WE}$ = L means any one or more byte write enable signals ($\overline{BWa}$, $\overline{BWb}$, $\overline{BWc}$ or $\overline{BWd}$) are LOW. $\overline{WE}$ = H means all byte write enable signals are HIGH.

2. $\overline{BWa}$ enables write to Bytea (DQa0 to DQa8). $\overline{BWb}$ enables write to Byteb (DQb0 to DQb8). $\overline{BWc}$ enables write to Byte2 (DQc0 to DQc8). $\overline{BWd}$ enables write to Byted (DQd0 to DQd8).
3. All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. A WRITE is performed by setting one or more byte write enable signals and $\overline{WE}$ LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.
5. The status for DQ described in this synchronous truth table appears two clocks after the cycle in which the Read or Write command is asserted.
6. If ADV/$\overline{LD}$ is sampled High that it is continue burst cycle follows before the operation cycle.
7. Wait states are inserted by $\overline{CEN}$ = High. When $\overline{CEN}$ is sampled High after Read cycle, the Read data is maintain as output data. When $\overline{CEN}$ is sampled High after Write cycle, the Write Input Data is ignored and is maintained High-Z. Refer to Timing diagram for clarification.

Asynchronous Truth Table

Operation	ZZ	$\overline{OE}$	I/O status
Read	L	L	Data out
Read	L	H	High-Z
Write	L	×	High-Z, Data in
Deselect	L	×	High-Z
Power down (Snooze)	H	×	High-Z

Note: H means logic HIGH. L means logic LOW. × means H or L.

Partial Truth Table for Writes

Operation	$\overline{WE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
Read	H	×	×	×	×
No write	L	H	H	H	H
Write byte a	L	L	H	H	H
Write all bytes	L	L	L	L	L

Note: H means logic HIGH. L means logic LOW. × means H or L.

Interleave Sequence Table ($\overline{LBO} = V_{DD}$ or V_{DDQ})

Parameter	Sequence 1 (A1, A0)	Sequence 2 (A1, A0)	Sequence 3 (A1, A0)	Sequence 4 (A1, A0)
External address	0 0	0 1	1 0	1 1
1st internal address	0 1	0 0	1 1	1 0
2nd internal address	1 0	1 1	0 0	0 1
3rd internal address	1 1	1 0	0 1	0 0

Note: Each sequence wraps around to its initial state upon completion.

Linear Sequence Table ($\overline{LBO} = V_{SS}$)

Parameter	Sequence 1 (A1, A0)	Sequence 2 (A1, A0)	Sequence 3 (A1, A0)	Sequence 4 (A1, A0)
External address	0 0	0 1	1 0	1 1
1st internal address	0 1	1 0	1 1	0 0
2nd internal address	1 0	1 1	0 0	0 1
3rd internal address	1 1	0 0	0 1	1 0

Note: Each sequence wraps around to its initial state upon completion.

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Supply voltage		V_{DD}	–0.5 to +4.6	V
Voltage on any pins relative to V_{SS}	(DQ)	V_T	–0.5 to V_{DDQ} + 0.5	V
Except V_{DD}	(Others)	V_T	–0.5 to V_{DD} + 0.5	V
Power dissipation		P_T	1.6	W
Operating temperature		Topr	0 to +70	°C
Storage temperature range (with bias)		Tstg (bias)	–10 to +85	°C
Storage temperature range		Tstg	–55 to +125	°C

Recommended DC Operating Conditions (3.3V Power supply)

(Ta = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply voltage (Operating voltage range)		V_{DD}	3.135	3.3	3.465	V	
Supply I/O voltage (3.3 V I/O)		V_{DDQ}	3.135	3.3	3.465	V	
Supply I/O voltage (2.5 V I/O)		V_{DDQ}	2.375	2.5	2.625	V	
Supply voltage to V_{SS}		V_{SS}	0.0	0.0	0.0	V	
Input high voltage (3.3 V I/O)	(DQ)	V_{IH}	2.0	-	V_{DDQ} + 0.3	V	
	(Others)	V_{IH}	2.0	-	V_{DD} + 0.3	V	
Input high voltage (2.5 V I/O)	(DQ)	V_{IH}	1.7	-	V_{DDQ} + 0.3	V	
	(Others)	V_{IH}	1.7	-	V_{DD} + 0.3	V	
Input low voltage (3.3 V I/O)		V_{IL}	–0.3	-	0.8	V	1
Input low voltage (2.5 V I/O)		V_{IL}	–0.3	-	0.7	V	1

Note: 1. –2.0 V for undershoot pulse width ≤ 20% t_{CYC}.

Recommended DC Operating Conditions (2.5V Power supply)

(Ta = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply voltage (Operating voltage range)		V_{DD}	2.375	2.5	2.625	V	
Supply I/O voltage (2.5 V I/O)		V_{DDQ}	2.375	2.5	2.625	V	
Supply voltage to V_{SS}		V_{SS}	0.0	0.0	0.0	V	
Input high voltage (2.5 V I/O)	(DQ)	V_{IH}	1.7	-	V_{DDQ} + 0.3	V	
	(Others)	V_{IH}	1.7	-	V_{DD} + 0.3	V	
Input low voltage (2.5 V I/O)		V_{IL}	–0.3	-	0.7	V	1

Note: 1. –2.0 V for undershoot pulse width ≤ 20% t_{CYC}.

DC Characteristics

(Ta = 0 to +70°C, V_{DD} = 3.3 V +5%/–5% or 2.5 V +5%/–5%)

		HM66WP18100/HM66WP36512							
		-40		-50		-60			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Input leakage current	I_{LI}	–2	2	–2	2	–2	2	µA	All inputs Vin = V_{SS} to V_{DD}
Output leakage current	I_{LO}	–5	5	–5	5	–5	5	µA	$\overline{OE}$ = V_{IH}, Vout = V_{SS} to V_{DDQ}
Operating current	I_{DD}	—	300	—	250	—	220	mA	Device selected, Iout = 0 mA, all inputs = V_{IH} or V_{IL}, cycle time = t_{CYC} min.
Standby current	I_{SB}	—	100	—	90	—	80	mA	Device deselected all inputs = fixed and all inputs ≥ V_{DD} – 0.2 V or ≤ 0.2 V, cycle time = t_{CYC} min.
	I_{SB1}	—	30	—	30	—	30	mA	Device deselected all inputs = fixed and all inputs ≥ V_{DD} – 0.2 V or ≤ 0.2 V, Frequency = 0 MHz.
	I_{SBZZ}	—	10	—	10	—	10	mA	Device deselected all inputs = fixed and all inputs ≥ V_{DD} – 0.2 V or ≤ 0.2 V, ZZ ≥ V_{DD} – 0.2 V, Frequency = 0 MHz.
Output low voltage (3.3 V I/O)	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 8 mA
Output high voltage (3.3 V I/O)	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = –4 mA
Output low voltage (2.5 V I/O)	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 1 mA
Output high voltage (2.5 V I/O)	V_{OH}	2.0	—	2.0	—	2.0	—	V	I_{OH} = –1 mA

Note: 1. $\overline{LBO}$ pin has an internal pull-up, ZZ pin has an internal pull-down, and input leakage current < |5µA|.

Capacitance

(Ta = +25°C, f = 1.0 MHz, V_{DD} = 3.3 V and 2.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input capacitance	Cin	—	4	5	pF	1
Input/output capacitance	$C_{I/O}$	—	6	7	pF	1

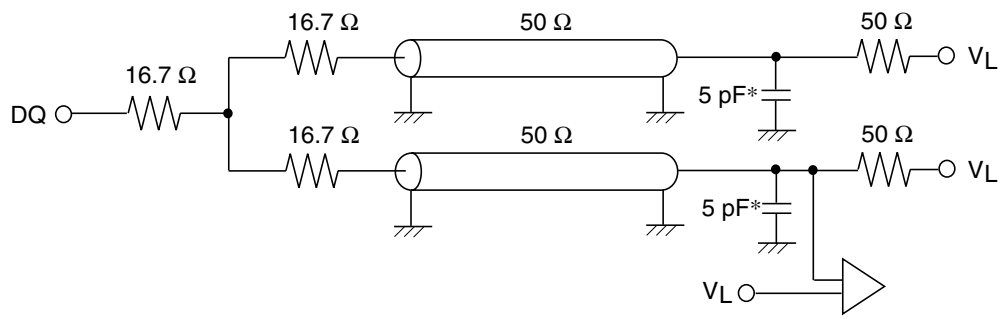
Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics

(Ta = 0 to +70°C, V_{DD} = 3.3 V +5%/–5% and 2.5 V +5%/–5%, V_{SS} = 0 V)

Test Conditions

- Input timing measurement reference level :1.4 V (3.3 V I/O)
  :1.2 V (2.5 V I/O)
- Input pulse levels : 0 V to 2.8 V (3.3 V I/O)
  : 0 V to 2.4 V (2.5 V I/O)
- Input rise and fall time: 2 V/ns (10% – 90%)
- Output timing reference level : 1.4 V (3.3 V I/O)
  : 1.2 V (2.5 V I/O)
- Output load: See figure



V_L = 1.4 V (3.3 V I/O) or 1.2 V (2.5 V I/O)

*(Including scope and jig)

	Symbol		HM66WP18100/HM66WP36512 -40		-50		-60			
Parameter	**Standard**	**Alternate**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Cycle time	t_{KHKH}	t_{CYC}	4.0	—	5.0	—	6.0	—	ns	
Clock access time	t_{KHQV}	t_{CA}	—	2.6	—	3.0	—	3.5	ns	
Output enable to output valid	t_{GLQV}	t_{OE}	—	2.6	—	3.0	—	3.5	ns	
Clock high to output active	t_{KHQX1}	t_{CLZ}	0.8	—	1.0	—	1.5	—	ns	
Clock high to output change	t_{KHQX2}	t_{COH}	0.8	—	1.0	—	1.5		ns	
Output enable to output active	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	ns	
Output disable to Q High-Z	t_{GHQZ}	t_{OHZ}	—	2.6	—	3.0	—	3.5	ns	1
Clock high to Q High-Z	t_{KHQZ}	t_{CHZ}	—	2.6	—	3.0	—	3.5	ns	1
Clock high pulse width	t_{KHKL}	t_{CH}	1.7	—	2.0	—	2.2	—	ns	
Clock low pulse width	t_{KLKH}	t_{CL}	1.7	—	2.0	—	2.2	—	ns	
Setup Times:			1.2	—	1.4	—	1.5	—	ns	
Address	t_{AVKH}	t_{SA}								
Clock Enable	t_{CENVKH}	t_{SCEN}								
Input Data	t_{DVKH}	t_{SD}								
Write ($\overline{WE}$,$\overline{BWa\text{-}d}$)	t_{WVKH}	t_{SW}								
Address Advance	t_{ADVVK}	t_{SADV}								
Chip Enable	t_{EVKH}	t_{SCE}								
Hold Times:			0.3	—	0.4	—	0.5	—	ns	
Address	t_{KHAX}	t_{HA}								
Clock Enable	t_{KHCENX}	t_{HCEN}								
Input Data	t_{KHDX}	t_{HD}								
Write ($\overline{WE}$,$\overline{BWa\text{-}d}$)	t_{KHWX}	t_{HW}								
Address Advance	t_{KHADVX}	t_{HADV}								
Chip Enable	t_{KHEX}	t_{HCE}								
ZZ Active to input ignored		t_{PDS}	2	—	2	—	2	—	cycle	4
ZZ Inactive to input Sampled		t_{PUS}	2	—	2	—	2	—	cycle	4
ZZ Active to sleep current		t_{ZZI}	—	2	—	2	—	2	cycle	4
ZZ Inactive to exit sleep current		t_{RZZI}	0	—	0	—	0	—	cycle	4

Notes: 1. Transition is measured ± 100 mV from steady-state voltage. This parameter is sampled.

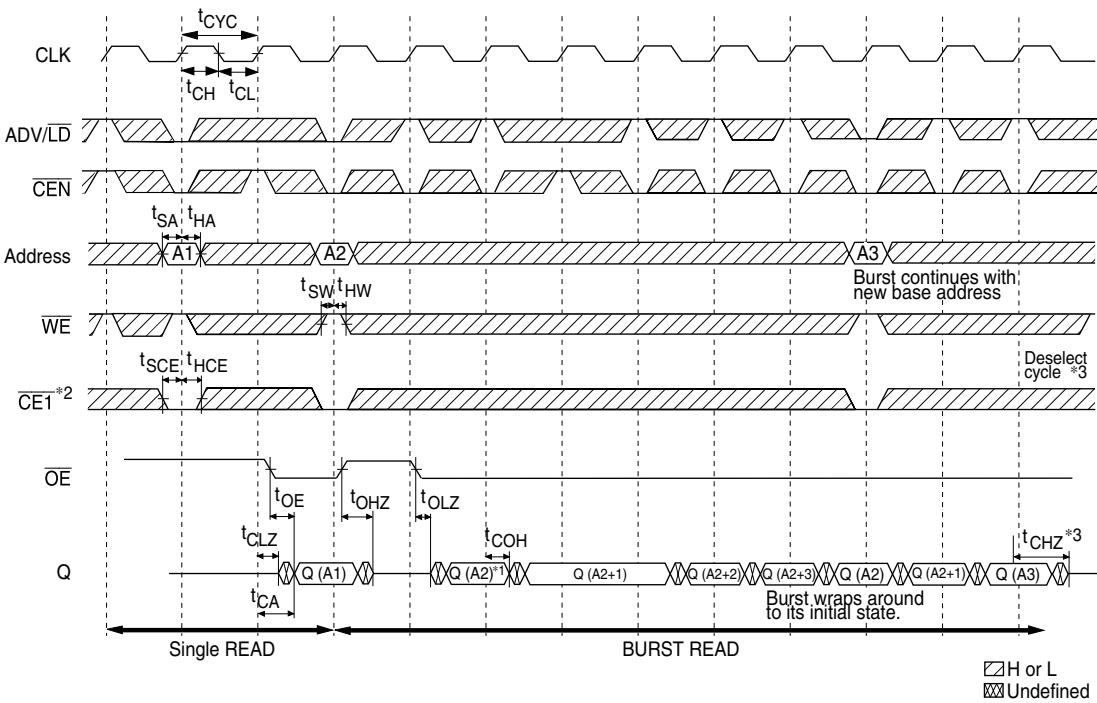
2. A READ cycle is defined by $\overline{WE}$ HIGH for the required setup and hold times. A WRITE cycle is defined by $\overline{WE}$ LOW for the required setup and hold times.

3. This is a synchronous device. All address must meet the specified setup and hold times for all rising edges of CLK when chip enabled. All other Synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK to remain enabled.

4. Data-output is not guaranteed during the cycle when transition of ZZ from low to high occurs.

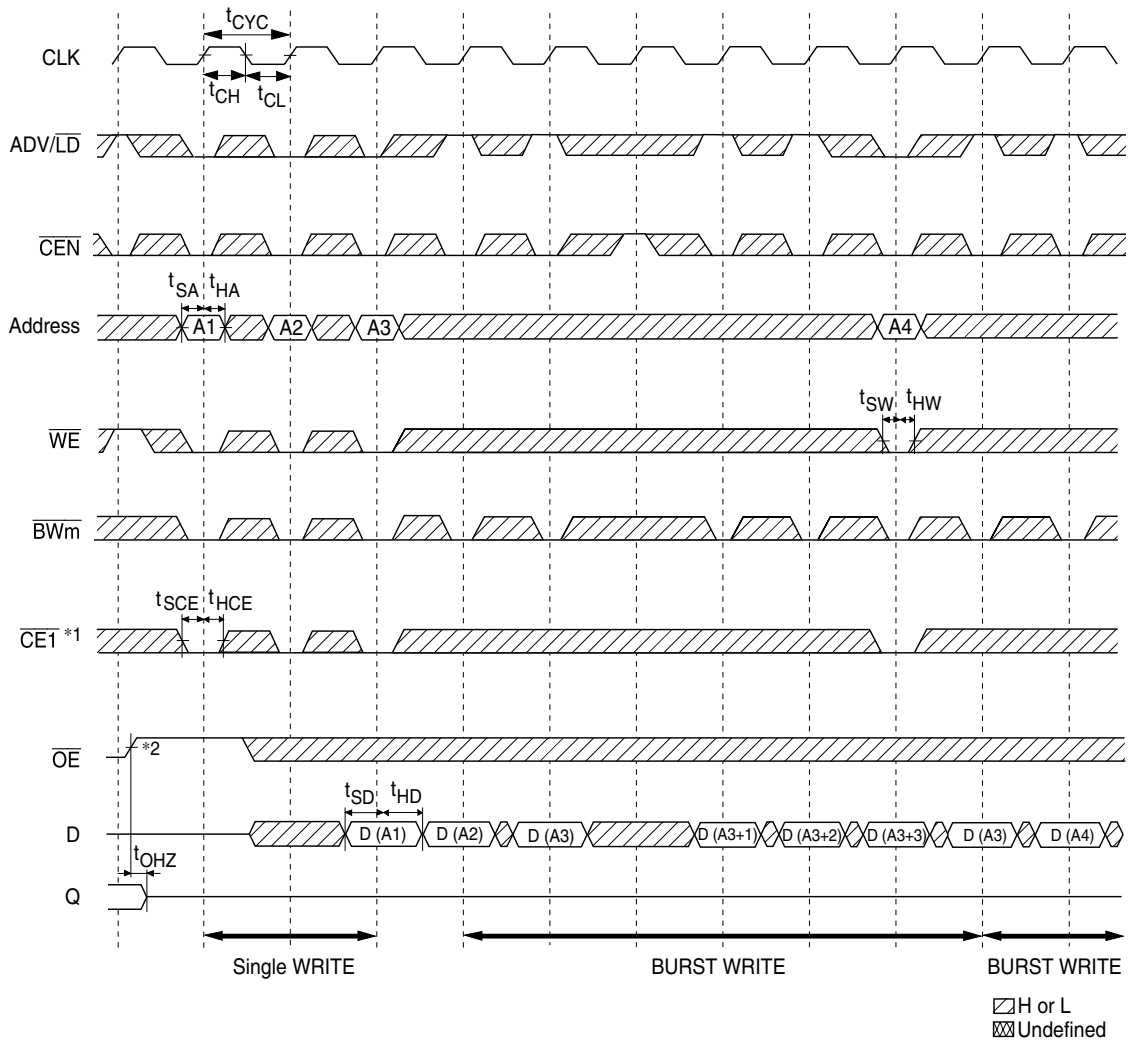
Timing Waveforms

Read Cycle



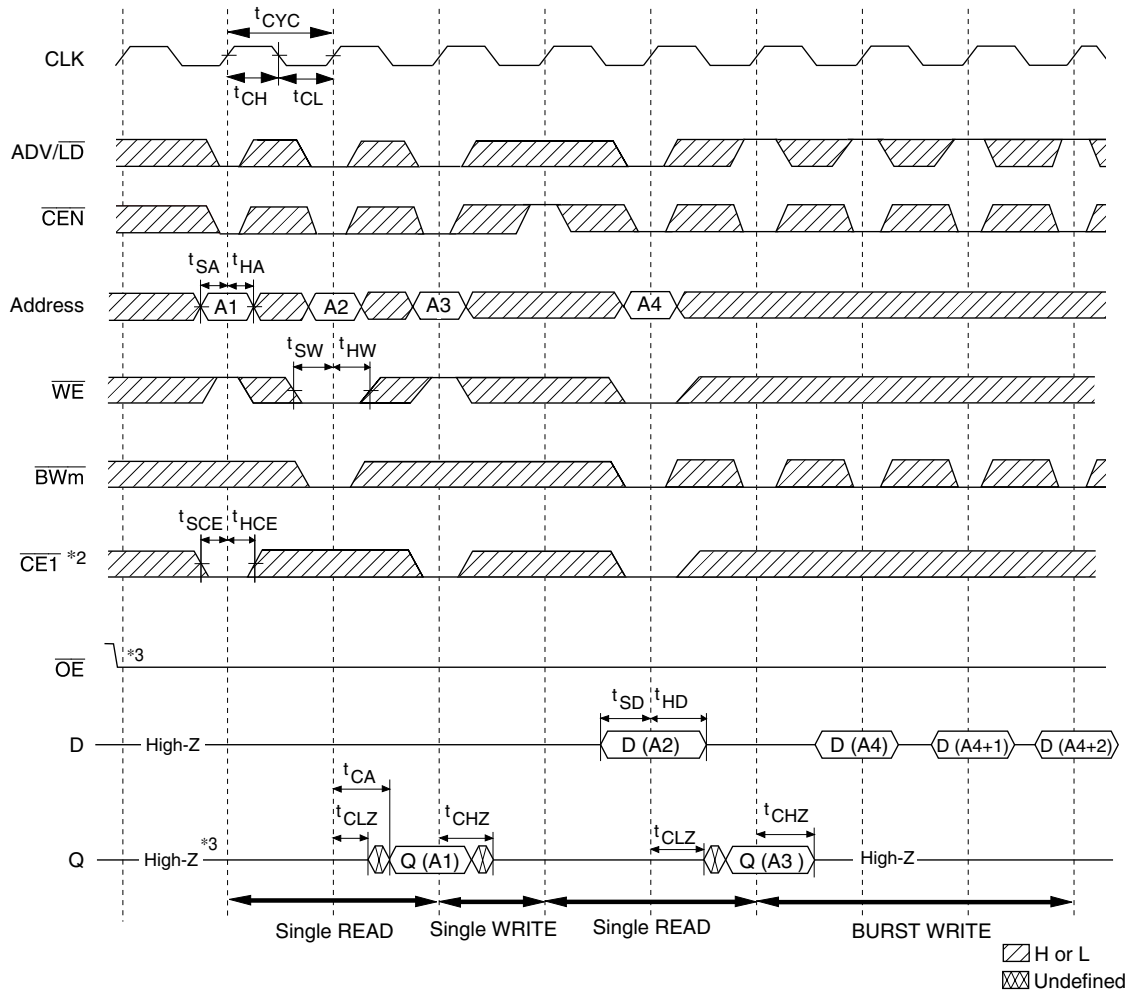
Notes: 1. Q (A2) refers to output from address A2. Q (A2 + 1) refers to output from next internal burst address following A2.
2. $\overline{CE3}$ and CE2 have timing identical to $\overline{CE1}$. On this diagram, when $\overline{CE1}$ is LOW, $\overline{CE3}$ is LOW and CE2 is HIGH. When $\overline{CE1}$ is HIGH, $\overline{CE3}$ is HIGH and CE2 is LOW.
3. Outputs are disabled within one clock cycle after deselect.
4. ZZ is LOW.

Write Cycle



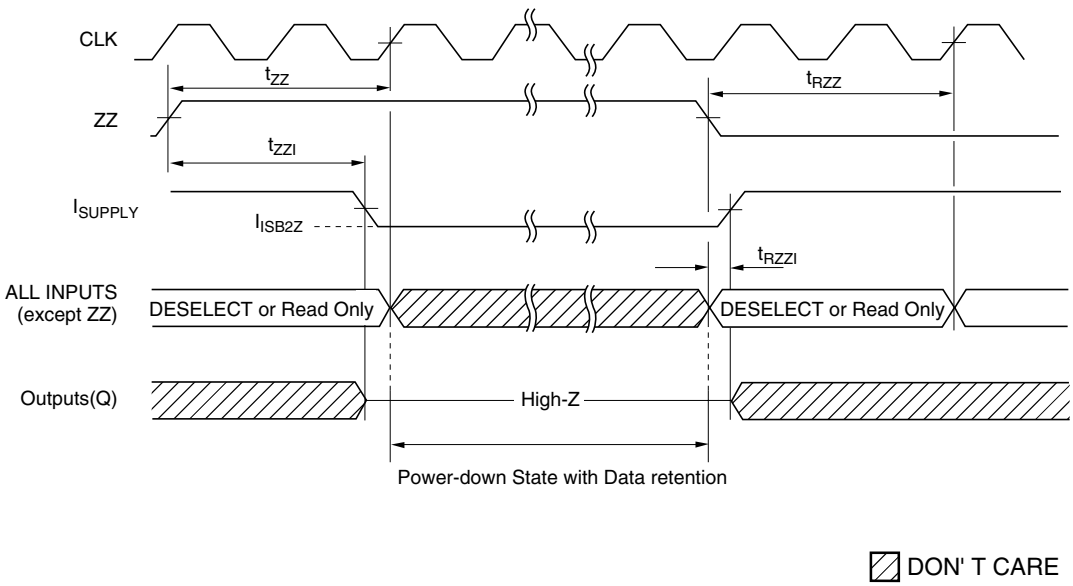
Notes: 1. $\overline{CE3}$ and CE2 have timing identical to $\overline{CE1}$. On this diagram, when $\overline{CE1}$ is LOW, $\overline{CE3}$ is LOW and CE2 is HIGH. When $\overline{CE1}$ is HIGH, $\overline{CE3}$ is HIGH and CE2 is LOW.
2. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
3. Full width WRITE can be initiated by $\overline{WE}$, $\overline{BWa}$ to $\overline{BWd}$ are LOW.
4. ZZ is LOW.

Read-Write Cycle



Notes: 1. Q (A3) refers to output from address A3.
2. $\overline{CE3}$ and CE2 have timing identical to $\overline{CE1}$. On this diagram, when $\overline{CE1}$ is LOW, $\overline{CE3}$ is LOW and CE2 is HIGH. When $\overline{CE1}$ is HIGH, $\overline{CE3}$ is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.
4. ZZ is LOW.

Power-down State



Notes: 1. The terms of t_{ZZ} and t_{RZZ} have to be that $\overline{CEN}$ is LOW.
2. Data-output is not guaranteed during the cycle when transition of ZZ from low to high occurs.

Boundary Scan Test Access Port Operations (only BGA)

Overview

In order to perform the interconnect testing of the modules that include this SRAM, the serial boundary scan test access port (TAP) is designed to operate in a manner consistent with IEEE Standard 1149.1 - 1990. But does not implement all of the functions required for 1149.1 compliance The HM66WP series contains a TAP controller. Instruction register, Boundary scans register, Bypass register and ID register.

Test Access Port Pins

Symbol I/O	Name
TCK	Test Clock
TMS	Test Mode Select
TDI	Test Data In
TDO	Test Data Out

Notes: This Device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1.
To disable the TAP, TCK must be connected to Vss. TDO should be left unconnected.
To test Boundary scan, ZZ pin need to be kept below V_{IL}.

TAP DC Operating Characteristics (Ta = 0°C to +70°C)

Parameter	Symbol	Min	Max	Notes
Boundary scan Input High voltage (3.3V I/O)	V_{IH}	2.0 V	V_{DD} +0.3V	
Boundary scan Input High voltage (2.5V I/O)	V_{IH}	1.7 V	V_{DD} +0.3V	
Boundary scan Input Low voltage (3.3V I/O)	V_{IL}	–0.3 V	0.8 V	
Boundary scan Input Low voltage (2.5V I/O)	V_{IL}	–0.3 V	0.7 V	
Boundary scan Input Leakage Current	I_{LI}	–5 µA	+5 µA	1
Boundary scan Output Leakage Current	I_{Lo}	–5 µA	+5 µA	1
Boundary scan Output Low voltage (3.3V/2.5V)	V_{OL}	—	0.4 V/0.4 V	2
Boundary scan Output High voltage (3.3V/2.5V)	V_{OH}	2.4 V/2.0 V	—	3

Notes: 1. $0 \le Vin \le V_{DD}$ for all logic input pin
2. I_{OL} = –8 mA at V_{DD} = 3.3 V , I_{OL} = –1 mA at V_{DD} = 2.5 V.
3. I_{OH} = 4 mA at V_{DD} = 3.3 V , I_{OH} = 1 mA at V_{DD} = 2.5 V.

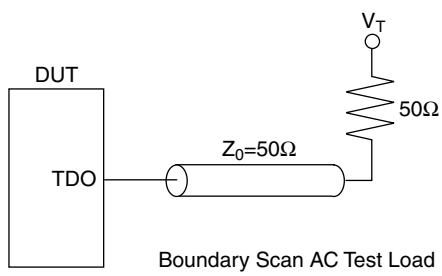
TAP AC Operating Characteristics (Ta = 0°C to +70°C)

Parameter	Symbol	Min	Max	Unit	Note
Test Clock Cycle Time	t_{THTH}	20	—	ns	
Test Clock High Pulse Width	t_{THTL}	8	—	ns	
Test Clock Low Pulse Width	t_{TLTH}	8	—	ns	
Test Mode Select Setup	t_{MVTH}	5	—	ns	
Test Mode Select Hold	t_{THMX}	5	—	ns	
Capture Setup	t_{CS}	5	—	ns	1
Capture Hold	t_{CH}	5	—	ns	1
TDI Valid to TCK High	t_{DVTH}	5	—	ns	
TCK High to TDI Don't Care	t_{THDX}	5	—	ns	
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns	
TCK Low to TDO Valid	t_{TLQV}	—	10	ns	

Note: 1. $t_{CS} + t_{CH}$ defines the minimum pause in RAM I/O pad transitions to assure pad data capture.

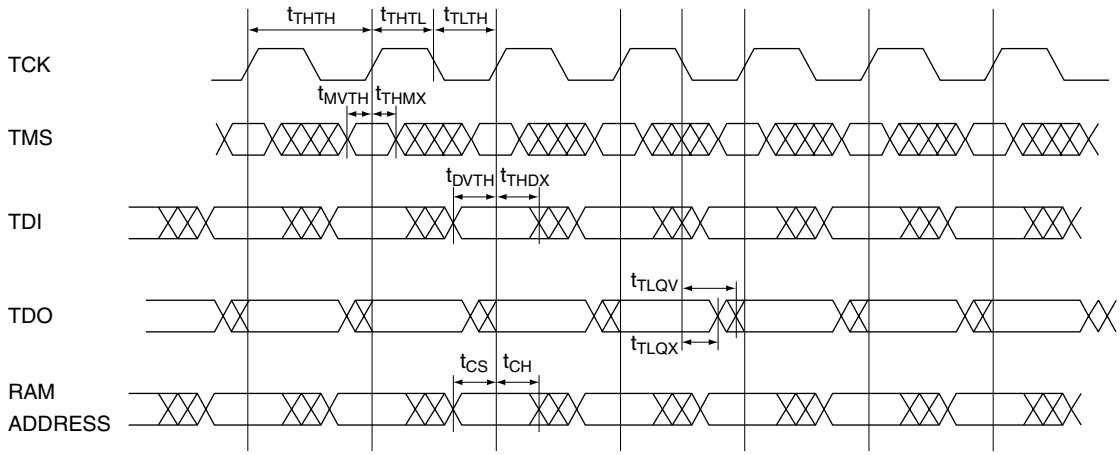
TAP AC Test Conditions (V_{DD} = 3.3 V and 2.5V)

	V_{DD} =3.3V	V_{DD} =2.5V
• Temperature	0°C ≤ Ta ≤ 70°C	0°C ≤ Ta ≤ 70°C
• Input timing measurement reference Level	1.4 V	1.2 V
• Input pulse levels	0 to 2.8 V	0 to 2.4 V
• Input Rise/Fall Time(10% to 90%)	2.0 ns typical	2.0 ns typical
• Output timing measurement reference Level	1.4 V	1.2 V
• Test load termination supply voltage (V_T)	1.4 V	1.2 V
• Output Load	See figures	See figures



Boundary Scan AC Test Load

TAP Controller Timing Diagram



TAP Controller Timing Diagram

Test Access Port Registers

Register Name	Length	Symbol	Note
Instruction Register	3 bits	IR [0;2]	
Bypass Register	1 bits	BP	
ID Register	32 bits	ID [0;31]	
Boundary Scan Register	70 bits	BS [1;70]	

TAP Controller Instruction Set

IR2	IR1	IR0	Instruction	Operation
0	0	0	SAMPLE-Z	Tristate all data drivers and capture the pad value
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	Tristate all data drivers and capture the pad value
0	1	1	BYPASS	
1	0	0	SAMPLE	
1	0	1	BYPASS	
1	1	0	BYPASS	
1	1	1	BYPASS	

Note: This Device does not perform EXTEST, INTEST or the preload portion of the PRELOAD command in IEEE 1149.1.

Boundary Scan Order (HM66WP36512BP)

Bit #	Bump ID	Signal name	Bit #	Bump ID	Signal name
1	2R	A5	36	6B	$\overline{CE3}$
2	3T	A10	37	5L	$\overline{BWa}$
3	4T	A11	38	5G	$\overline{BWb}$
4	5T	A14	39	3G	$\overline{BWc}$
5	6R	A13	40	3L	$\overline{BWd}$
6	3B	A3	41	2B	CE2
7	5B	A9	42	4E	$\overline{CE1}$
8	6P	DQa0	43	3A	A4
9	7N	DQa3	44	2A	A6
10	6M	DQa4	45	2D	DQc0
11	7L	DQa6	46	1E	DQc3
12	6K	DQa7	47	2F	DQc4
13	7P	DQa1	48	1G	DQc6
14	6N	DQa2	49	2H	DQc7
15	6L	DQa5	50	1D	DQc1
16	7K	DQa8	51	2E	DQc2
17	7T	$\overline{ZZ}$	52	2G	DQc5
18	6H	DQb7	53	1H	DQc8
19	7G	DQb6	54	5R	NC
20	6F	DQb4	55	2K	DQd7
21	7E	DQb3	56	1L	DQd6
22	6D	DQb0	57	2M	DQd4
23	7H	DQb8	58	1N	DQd3
24	6G	DQb5	59	2P	DQd0
25	6E	DQb2	60	1K	DQd8
26	7D	DQb1	61	2L	DQd5
27	6A	A16	62	2N	DQd2
28	5A	A8	63	1P	DQd1
29	4G	A17	64	3R	$\overline{LBO}$
30	4A	A18	65	2C	A7
31	4B	ADV/$\overline{LD}$	66	3C	A2
32	4F	$\overline{OE}$	67	5C	A12
33	4M	$\overline{CEN}$	68	6C	A15
34	4H	$\overline{WE}$	69	4N	A1
35	4K	CLK	70	4P	A0

Notes: 1. Bit#1 is the first scan bit to exit the chip.

2. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a “Place Holder”. Place holder registers are internally connected to V_{SS}.

3. ZZ must remain at V_{IL} during boundary scan.

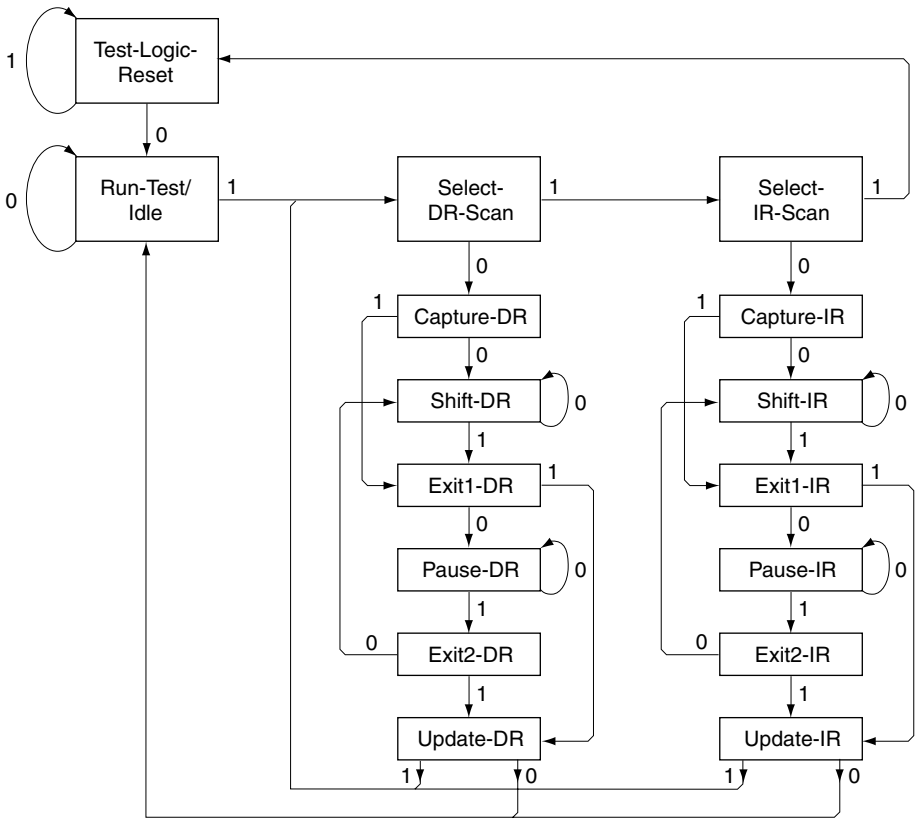
Boundary Scan Order (HM66WP18100BP)

Bit #	Bump ID	Signal name	Bit #	Bump ID	Signal name
1	2R	A5	36	2E	DQb7
2	2T	A10	37	2G	DQb6
3	3T	A15	38	1H	DQb5
4	5T	A14	39	5R	NC
5	6R	A12	40	2K	DQb4
6	3B	A3	41	1L	DQb3
7	5B	A9	42	2M	DQb2
8	7P	DQa0	43	1N	DQb1
9	6N	DQa1	44	2P	DQb0
10	6L	DQa2	45	3R	$\overline{\text{LBO}}$
11	7K	DQa3	46	2C	A7
12	7T	ZZ	47	3C	A2
13	6H	DQa4	48	5C	A13
14	7G	DQa5	49	6C	A17
15	6F	DQa6	50	4N	A1
16	7E	DQa7	51	4P	A0
17	6D	DQa8			
18	6T	A11			
19	6A	A16			
20	5A	A8			
21	4G	A18			
22	4A	A19			
23	4B	ADV/$\overline{\text{LD}}$			
24	4F	$\overline{\text{OE}}$			
25	4M	$\overline{\text{CEN}}$			
26	4H	$\overline{\text{WE}}$			
27	4K	CLK			
28	6B	$\overline{\text{CE3}}$			
29	5L	$\overline{\text{BWa}}$			
30	3G	$\overline{\text{BWb}}$			
31	2B	CE2			
32	4E	$\overline{\text{CE1}}$			
33	3A	A4			
34	2A	A6			
35	1D	DQb8			

Notes: 1. Bit#1 is the first scan bit to exit the chip.
2. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a “Place Holder”. Place holder registers are internally connected to V_{SS}.
3. ZZ must remain at V_{IL} during boundary scan.

ID Register

Part	Revision Number (31:28)	Device Density and Configuration (27:18)	Vendor Definition (17:12)	Vendor JEDEC Code (11:1)	Start Bit (0)
HM66WP36512	XXXX	0011100100	xxxxxx	00000000111	1
HM66WP18100	XXXX	0100000011	xxxxxx	00000000111	1



Notes: The value adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.
No matter what the original state of the controller, it will enter Test-Logic-Reset when TMS is held high for at least five rising edges of TCK

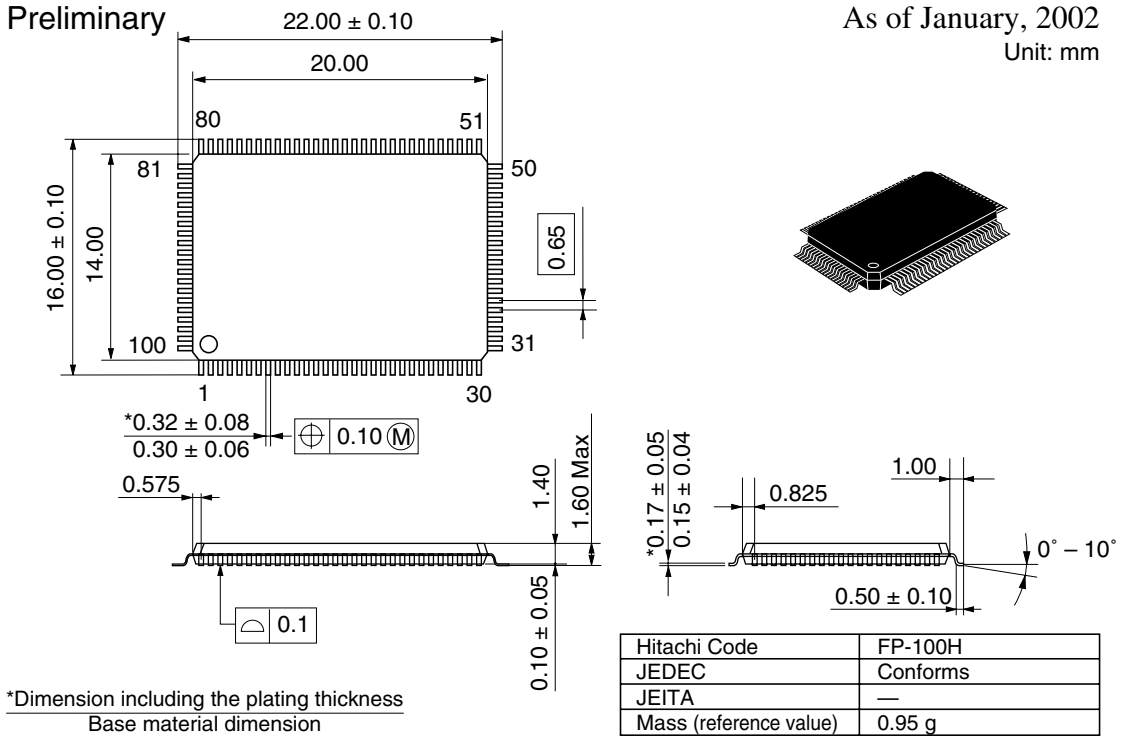
Package Dimensions

HM66WP18100FP, HM66WP36512FP Series (FP-100H)

Preliminary

As of January, 2002

Unit: mm



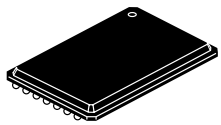
Hitachi Code	FP-100H
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.95 g

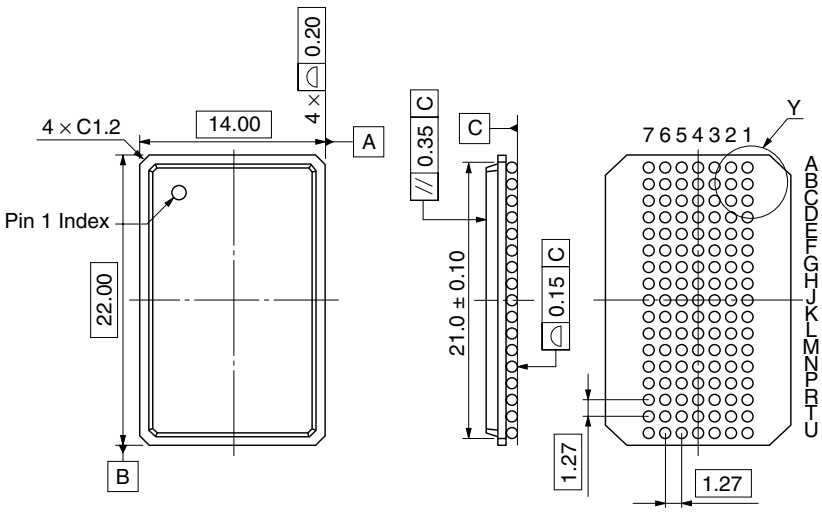
*Dimension including the plating thickness
Base material dimension

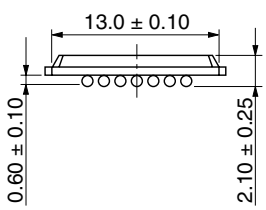
HM66WP18100BP, HM66WP36512BP Series (BP-119A)

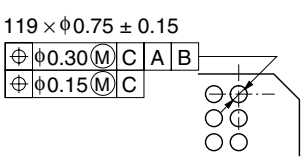
As of January, 2002

Unit: mm









Details of the part Y

Hitachi Code	BP-119A
JEDEC	Conforms
JEITA	—
Mass (reference value)	1.2 g

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