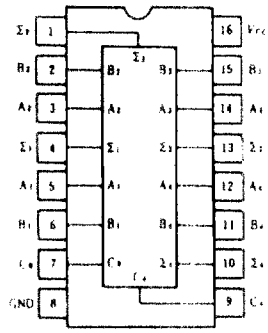
HD74HC283 ● 4-bit Binary Full Adder

The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. This adder features full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation. The adder logic, including the carry, is implemented in its true for meaning that the end-around carry can be accomplished without the need for logic or level inversion.

■ PIN ARRANGEMENT



(Top View)

■ FEATURES

- High Speed Operation: t_{pd}=19ns typ. (C_L=50pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: Vcc=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: Icc (static)=4μA max. (Ta=25°C)

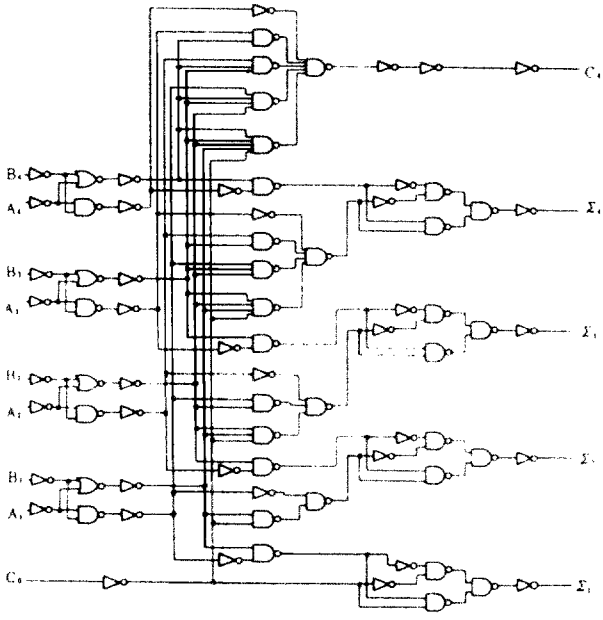
■ FUNCTION TABLE

Inputs				Outputs					
				When C_0=L		When C_2=L	When C_0=H		When C_2=H
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H; high level, L; low level

Notes) Input conditions at A_1, B_1, A_2, B_2, and C_0 are use to determine outputs Σ_1 and Σ_2 and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4 are then used to determine outputs Σ_3, Σ_4, and C_4.

■ BLOCK DIAGRAM



■ DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		$Ta=25°C$ min	typ	max	$Ta=-40\sim+85°C$ min	max	Unit
Input Voltage	V_{IH}	2.0			1.5	—	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	
		6.0			4.2	—	—	4.2	—	
	V_{IL}	2.0			—	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	
Output Voltage	V_{OH}	2.0	$V_{in}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	1.9	2.0	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	
		4.5		$I_{OH}=-4mA$	4.18	—	—	4.13	—	
		6.0		$I_{OH}=-5.2mA$	5.68	—	—	5.63	—	
	V_{OL}	2.0	$V_{in}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	—	0.0	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	
		4.5		$I_{OL}=4mA$	—	—	0.26	—	0.33	
		6.0		$I_{OL}=5.2mA$	—	—	0.26	—	0.33	
Input Current	I_{in}	6.0	$V_{in}=V_{CC}$ or GND		—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	$V_{in}=V_{CC}$ or GND, $I_{out}=0\mu A$		—	—	4.0	—	40	μA

■ AC CHARACTERISTICS ($C_L=50pF$, Input $t_r=t_f=6ns$)

Item	Symbol	V_{CC}(V)	Test Conditions	$Ta=25°C$ min	typ	max	$Ta=-40\sim+85°C$ min	max	Unit
Propagation Delay Time	t_{PLH} t_{PHL}	2.0	C_n to Σ_n	—	—	150	—	190	ns
		4.5		—	19	30	—	38	
		6.0		—	—	26	—	33	
	t_{PLH} t_{PHL}	2.0	A_n or B_n to Σ_n	—	—	150	—	190	ns
		4.5		—	19	30	—	38	
		6.0		—	—	26	—	33	
	t_{PLH} t_{PHL}	2.0	C_n to C_{n+1}	—	—	150	—	190	ns
		4.5		—	19	30	—	38	
		6.0		—	—	26	—	33	
	t_{PLH} t_{PHL}	2.0	A_n or B_n to C_{n+1}	—	—	150	—	190	ns
		4.5		—	19	30	—	38	
		6.0		—	—	26	—	33	
Output Rise/Fall Time	t_{TLH} t_{THL}	2.0		—	—	75	—	95	ns
		4.5		—	5	15	—	19	
		6.0		—	—	13	—	16	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF