High-Speed CMOS SynchroSwitch™ Clocked 8 Port x 4 Crossbar Switch

QS3B842

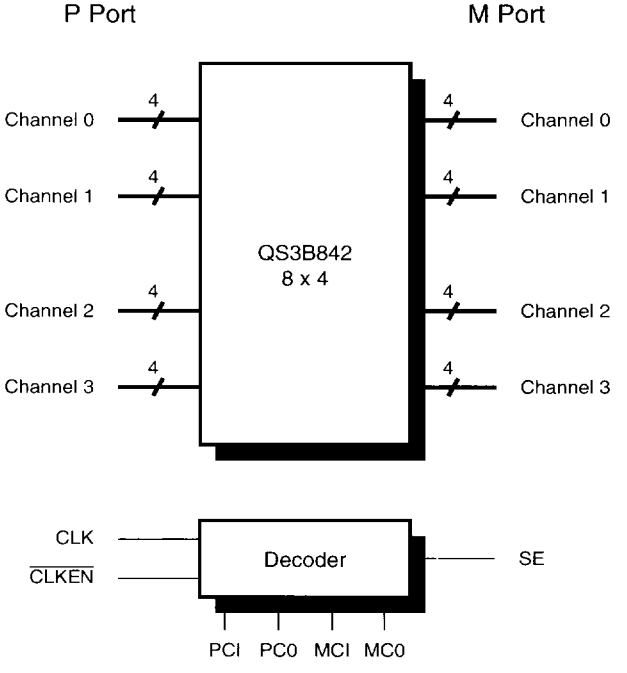
FEATURES/BENEFITS

- Bi-directional analog or digital switching
- Eight ports of 4 bits
- Decoded and registered control signals
- Zero added signal skew
- Overriding Switch Enable disconnects all channels
- Available in 48-pin QVSOP, SSOP
- Low power QCMOS™ Technology
- Zero added ground bounce

DESCRIPTION

The QS3B842 is a QuickSwitch based crossbar switch with eight ports of four bits. Each M port can connect to any P port (see table). Data flow is transparent and bi-directional and requires no direction control. In addition all ports are disconnected when SE (switch enable) is LOW.The QuickSwitch crossbar is ideal for implementing switching protocols in networking systems, data bus order changes, and other multi-way datacommunication and multiprocessing applications. This part can also be used where multiple DSPs or microprocessors communicate with slave devices or memories.

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

SWITCH ENABLE (SE)

This is an overriding switch enable. When HIGH, all switches are enabled or ON. When LOW, all switches are disabled or OFF.

CLOCK (CLK)

This is a free running clock which is used to update the contents of the P and M registers when $\overline{CLKEN}$ is LOW.

CLOCK ENABLE ($\overline{CLKEN}$)

When LOW, allows the clock to change the P and M registers. When HIGH, the clock input is disabled.

PCx and MCx CONTROLS

When selected, (see table) controls which P channel connects to which M channel. Four selections qualified each with four clocks are needed to fully configure every channel. Single word updates can be used to reconfigure a sub-section of the device. The SE pin should be LOW when reconfiguring the channels as there could be possible bus contention. Once fully configured, the SE pin can then go HIGH, enabling all the I/O channels.

e.g. Old Configuration

Connection		PC1	PC0	MC1	MC0
M0	P1	0	1	0	0
M1	P0	0	0	0	1
M2	P3	1	1	1	0
M3	P2	1	0	1	1

e.g. New Configuration Sequence

Connection		PC1	PC0	MC1	MC0	CLK	$\overline{CLKEN}$	SE
M0	P3	1	1	0	0	↑	0	0
M1	P1	0	1	0	1	↑	0	0
M2	P0	0	0	1	0	↑	0	0
M3	P2	1	0	1	1	↑	0	0
Channels Configured						X	0	1

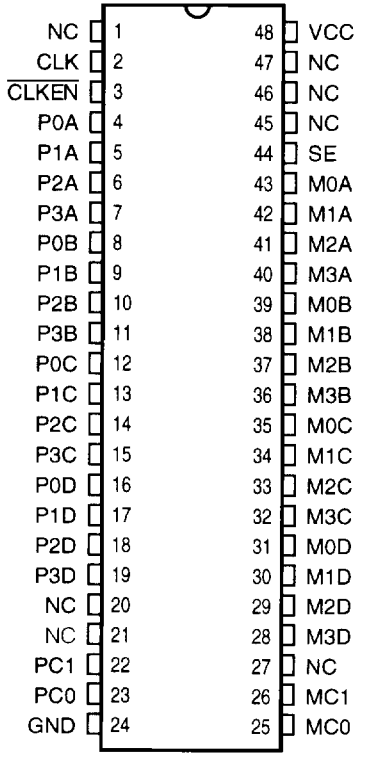
FUNCTION TABLE

SE	CLK	$\overline{CLKEN}$	PC1	PC0	MC1	MC0	Channel P	Channel M
1	↑	0	0	0	0	0	0	0
1	↑	0	0	0	0	1	0	1
1	↑	0	0	0	1	0	0	2
1	↑	0	0	0	1	1	0	3
1	↑	0	0	1	0	0	1	0
1	↑	0	0	1	0	1	1	1
1	↑	0	0	1	1	0	1	2
1	↑	0	0	1	1	1	1	3
1	↑	0	1	0	0	0	2	0
1	↑	0	1	0	0	1	2	1
1	↑	0	1	0	1	0	2	2
1	↑	0	1	0	1	1	2	3
1	↑	0	1	1	0	0	3	0
1	↑	0	1	1	0	1	3	1
1	↑	0	1	1	1	0	3	2
1	↑	0	1	1	1	1	3	3
1	↑	1	X	X	X	X	Previous State	
0	X	X	X	X	X	X	Hi-Z	Hi-Z

Note: Selections marked with the same letter (X or Y) indicates ports connected together.

PIN CONFIGURATION
(All Pins Top View)

QVSOP (Q1),
SSOP (PV)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	−0.5V to +7.0V
DC Switch Voltage V_S	−0.5V to Vcc + 0.3V
DC Input Voltage V_{IN}	−0.5V to Vcc + 0.3V
AC Input Voltage (for a pulse width ≤ 20 ns)	−3.0V
DC Input Diode Current with $V_I < 0$	−20 mA
DC Output Current Max. Sink Current/Pin	120 mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	−65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

CAPACITANCE

T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	SSOP Typ	SSOP Max	QVSOP Typ	QVSOP Max	Units
Control Pins	5	7	5	7	pF
QuickSwitch Channels Off	20	—	20	—	pF
QuickSwitch, One to One Channels	40	—	40	—	pF

Note: Capacitance is characterized but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions	Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Pins	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Pins	—	—	0.8	V
$\lvert I_{IN} \rvert$	Input Leakage Current(2)	$0 \le V_{IN} \le V_{CC}$	—	—	1	µA
$\lvert I_{OZ} \rvert$	Off-State Current (Hi-Z)	$0 \le A, B \le V_{CC}$	—	—	1	µA
R_{ON}	Switch On Resistance	V_{CC} = Min., V_{IN} = 0.0V, I_{ON} = 30 mA	—	10	—	Ω
		V_{CC} = Min., V_{IN} = 2.4V, I_{ON} = 15 mA	—	15	—	
		V_{CC} = Min., V_{IN} =4.0V, I_{ON} = 15 mA	—	27	—	

Notes:
1. Typical values indicate Vcc = 5.0V and T_A = 25°C.
2. Measured by voltage drop between A and B pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (A, B) pins.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	Vcc = Max., V_{IN} = GND or Vcc, f = 0	600	µA
ΔI_{CC}	Power Supply Current(2) per Input HIGH	Vcc = Max., V_{IN} = 3.4V, f = 0 per Control Input	2.5	mA
Q_{CCD}	Dynamic Power Supply Current per MHz(3)	Vcc = Max., A and B Pins Open, Control Inputs Toggling @ 50% Duty Cycle	1.0	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V, control inputs only). A and B pins do not contribute to Icc.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed by design, but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, Vcc = 5.0V ± 5%
C_{LOAD} = 50 pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
t_{PLH} t_{PHL}	Single Channel Port Propagation Delay[3]	—	1.25	—	ns
t_{SCS}	Control S Inputs to CLK Setup Time	2	—	—	ns
t_{HCS}	Control S Inputs to CLK Hold Time	0	—	—	ns
t_{SEC}	$\overline{CLKEN}$ to CLK Setup Time [2]	2	—	—	ns
t_{HEC}	$\overline{CLKEN}$ to CLK Setup Time [2]	0	—	—	ns
t_W	Clock Pulse Width (HIGH)	3	—	—	ns
t_{PZL} t_{PZH}	Asynchronous Enable to Turn On Delay[1]	1.5	—	7.0	ns
t_{PLZ} t_{PHZ}	Asynchronous Enable to Turn Off Delay[1,2]	1.5	—	6.5	ns
|Qcl|	Charge Injection[4,5]	—	1.5	—	pC

Notes:
1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
4. Measured at switch turn off, A to C, load = 50 pF in parallel with 10 meg scope probe, V_{IN} at A = 0.0V.
5. Characterized parameter but not production tested.

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TIMING DIAGRAM