MICRO NETWORKS

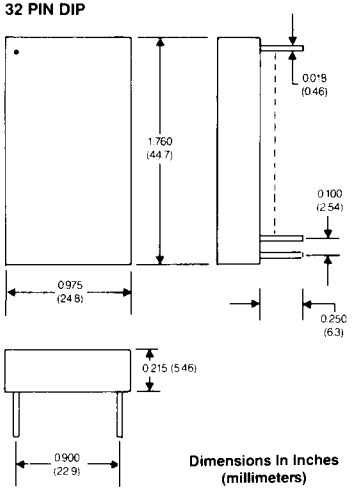
# MD2840/2841/2842

100/200/500msec
INTEGRATING A/D CONVERTERS

## FEATURES

- **20-Bit Integrating A/D**
- **Programmable Conversion Time**
- **Continuous Sampling**
- **$<10\mu V$ Sensitivity**
- **Repeatability to 0.3ppm**
- **Microprocessor Compatible**
- **1,000,000:1 Dynamic Range**
- **No Dead Time**

32 PIN DIP




Dimensions In Inches
(millimeters)

## DESCRIPTION

Models MD2840/2841/2842 are complete, integrating A/D converters performing 20-bit conversions in 100 milliseconds, 200 milliseconds and 500 milliseconds respectively. This series uses a charged-balanced asynchronous V/F converter architecture with internal counter/timer for ultra-precise repeatability of wide-dynamic-range, slowly varying signals.

With an input range of $-10\mu V$ to $-10V$, this series provides A/D conversion with a dynamic range of 1,000,000:1 (120db) without the complications and errors associated with gain-ranging or logarithmic schemes.

Their unique architecture allows for continuous integration of the input signal, improving noise rejection and avoiding the annoying dead time associated with most integrating converters. The MD2840/2841/2842 Series achieves remarkable repeatability of 0.3 ppm at up to 100 samples per second depending on mode, speed, and resolution chosen (see respective applications criteria).

Commands to the converter and data from the converter are communicated over an 8-bit microprocessor-compatible bus. The unit can be used in continuous-sample or triggered mode, where a data-ready flag alerts the $\mu P$ that the conversion is complete.

## APPLICATIONS

**Analytical Instrumentation**
**Automatic Test Equipment**
**Clinical Chemistry**
**Data-Acquisition Systems**
**Elemental Analysis**
**Magnetometers**
**Medical Instrumentation**
**Seismology**
**Thickness & Weighing Systems**
**Industrial Data Collection**



MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

April 1992

# MD2840/2841/2842 V/F, F/V CONVERTERS

**ABSOLUTE MAXIMUM RATINGS**

| | |
|---|---|
| Operating Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −25°C to +100°C |
| +15V Supply (Pin 31) | +15.45 V |
| −15V Supply (Pin 32) | −15.45 V |
| +5V Analog Supply (Pin 29) | +5.25 V |
| +5V Digital Supply (Pin 15) | +5.25 V |
| Digital Inputs (Pins 4, 5, 6, 20, 21, 22, 23, 25, 26) | −0.3V to +5.3V |
| Analog Input | −15 V to +15V |

**ORDERING INFORMATION**
**PART NUMBER** MD2840 / 2841 / 2842

10MHz Full-scale
5MHz Full-scale
2MHz Full-scale

**SPECIFICATIONS ($T_A$ = +25°C, Supplies = ±15V and +5V unless otherwise specified)**

| ANALOG INPUTS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|
| Input Voltage Range | | 0 to −10 | | Volts |
| Overrange | | | 5 | % |
| Configuration | | Single-Ended | | |
| Input Impedance<br>MD2840, MD2841<br>MD2842 | | <br>6<br>14 | | <br>kΩ<br>kΩ |
| Offset Voltage (trimmable to zero) | | | ±10 | mV |
| **TRANSFER CHARACTERISTICS** | | | | |
| Full-Scale Output MD2840<br>MD2841<br>MD2842 | | 10<br>5<br>2 | | MHz<br>MHz<br>MHz |
| Gain Error (trimmable to zero) | | | ±1 | % |
| Differential Nonlinearity MD2840<br>MD2841<br>MD2842 | | | 0.1<br>0.2<br>0.5 | ppm of FSR<br>ppm of FSR<br>ppm of FSR |
| Integral Nonlinearity MD2840<br>(maximum) MD2841<br>MD2842 | | ±0.05% FS ± 0.05% $V_{IN}$<br>±0.02% FS ± 0.02% $V_{IN}$<br>±0.01% FS ± 0.01% $V_{IN}$ | | |
| Full-Scale Step Response MD2840<br>(maximum) MD2841<br>MD2842 | | 5μsec + 2 cycles of new $f_{OUT}$<br>10μsec + 2 cycles of new $f_{OUT}$<br>20μsec + 2 cycles of new $f_{OUT}$ | | |
| Overload Recovery MD2840<br>(maximum) MD2841<br>MD2842 | | 12 cycles of new $f_{OUT}$<br>10 cycles of new $f_{OUT}$<br>8 cycles of new $f_{OUT}$ | | |
| Noise (3σ) MD2840<br>($V_{IN}$ = −10V, 1 sample/sec, MD2841<br>3 minutes) MD2842 | | 5<br>4<br>3 | | μV<br>μV<br>μV |
| **STABILITY** | | | | |
| Gain Temperature Coefficient | | 60 | 100 | ppm of FSR/°C |
| Offset Temperature Coefficient | | 10 | 30 | ppm of FSR/°C |
| Power Supply Rejection Gain<br>Offset | | | 200<br>10 | ppm of FSR/%$V_S$<br>μV/%$V_S$ |
| Warm-up Time (to specified accuracy) | | | 2 | Minutes |
| **DIGITAL INPUTS** | | | | |
| Logic Levels Logic "1"<br>Logic "0" | +2.4 | | <br>+0.4 | Volts<br>Volts |
| Pulse Width R/W<br>All Others | 50<br>10 | | | nsec<br>nsec |
| **POWER SUPPLY REQUIREMENTS** | | | | |
| ±15V Supplies<br>+5V Supplies | ±14.55<br>+4.75 | | ±15.45<br>+5.25 | Volts<br>Volts |
| Current Drains +15V<br>−15V<br>+5V | | 3<br>10<br>200 | | mA<br>mA<br>mA |

## THEORY OF OPERATION

The MD2840/2841/2842 Series uses a charge-balanced asynchronous V/F converter with internal counter-timer architecture as shown in Figure 1. The full-scale range of the V/F is 10MHz for the 2840, 5MHz for the 2841 and 2MHz for the 2842. The input signal is tracked by the V/F, producing a pulse frequency linearly proportional to its full scale, ie:

$$\frac{V_{in}}{V_{FS}} = \frac{F_{out}}{F_{FS}}$$

This frequency is accumulated by the counter/timer for the full conversion time of the A/D and presented at the output as a binary word up to 24 bits wide. The continuous tracking and accumulation of pulses performs an inherently monotonic integrating function.

Once the pulse accumulation is complete, the count is instantaneously transferred to the output stage, ready to be accessed by the $\mu$P. In the continuous sample mode, the counter/timer instantaneously begins to accumulate counts for the next measurement. In the external trigger mode, the counter/timer awaits a trigger command before beginning the next accumulation of pulses.

In both cases the V/F continues to generate a pulse frequency proportionately tracking the input signal. There is no dead time on these converters, so the integration period and the conversion time is the same and the terms are used interchangeably.

**SENSITIVITY VS SPEED** — The sensitivity of the MD2840/2841/2842 Series is directly proportional to the amount of time the converter is allowed to integrate the input signal.

$$\text{Sensitivity} = \frac{V_{FS}}{F_{FS} \bullet T_C}$$

Where $V_{FS}$ = Full-scale Voltage
$F_{FS}$ = Full-scale Frequency of the V/F
$T_C$ = Conversion Time

**EXAMPLE** — If the MD2840, (with its 10MHz V/F) integrates the input signal for 1/10th of a second, it will accumulate 1,000,000 pulses. If the full-scale input voltage is 10V, each pulse counted will represent 10$\mu$V. Thus, the sensitivity of the MD2840 at 10 samples per second is 10$\mu$V.

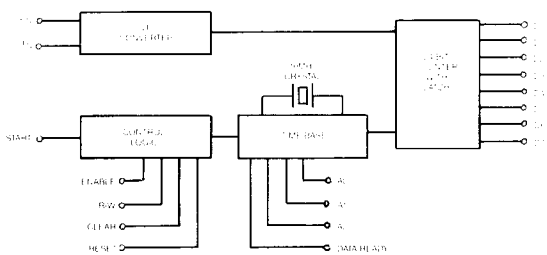


**Figure 1. Md2840/2841/2842 Block Diagram**

**CHOOSING A CONVERSION TIME** — The architecture of the MD2840/2841/2842 Series allows the designer to choose the conversion time of the A/D converter, for the sensitivity, for integration period, or for a combination of both criteria.

**A. For Sensitivity** — Often sensitivity, that is, the minimum change in input voltage detectable by the converter, will be the overriding criterion.

In that case, calculate the percent of full-scale represented by the sensitivity. The inverse of that number represents the full scale count needed.

$$S = V_{FS}/(F_{FS} \bullet T_C)$$

For Example
10$\mu$V on 10$V_{FS}$ = 1ppm
1/1ppm = $10^6$ counts
or
1mV on 10V = 0.01%
1/0.01% = $10^4$ counts

Next, determine the amount of time required for the V/F to generate that count full scale. That will be your conversion time:

| Model | $10^6$ Counts | | $10^4$ Counts |
|---|---|---|---|
| MD2840 (10MHz) | 0.1 sec | or | 0.001 sec |
| MD2841 (5MHz) | 0.2 sec | | 0.002 sec |
| MD2842 (2MHz) | 0.5 sec | | 0.005 sec |

**B. For Integration Period** —

Integration Period = $T_C = V_{FS}/(F_{FS} \bullet \text{Sensitivity})$

Example: At 100 msec integrating (conversion) time

| Model | Count | Resolution | Sensitivity |
|---|---|---|---|
| MD2840 (10MHz) | $10^6$ counts FS | ~20 Bits | 10$\mu$V |
| MD2841 (5MHz) | $5 \times 10^5$ counts FS | ~19 Bits | 20$\mu$V |
| MD2842 (2MHz) | $2 \times 10^5$ counts FS | ~18 Bits | 50$\mu$V |

**C. Combination** — In multiplexed systems different sensitivity/speed combinations may be required for each channel. This is easily accomplished with the MD2840/2841/2842 Series by a simple program command setting the conversion time.

With the very wide dynamic range of the MD2840/2841/2842 Series the entire input range can be sampled at high speed and low resolution until the desired level is detected. Then the integration time can be extended for higher-sensitivity measurements.

Where several instruments share one analog front-end design — a combination of speed and sensitivity can be programmed into the MD2840/2841/2842 Series "on the fly."

Sometimes the conversion time dominates the design decision. This is true when trying to reject periodic normal-mode noise — such as 50/60 Hz line pickup. Then the conversion time should be set at an integer multiple of the period of the noise (ie. 20 msec or 40 msec or 60 msec for 50Hz rejection). 100 msec integration is common as it rejects both 50 and 60 Hz pickup. Once the conversion time is chosen, the resolution and sensitivity can be calculated.

| Model/ Conversion Time | **MD2840** 10MHz | **MD2841** 5MHz | **MD2842** 2MHz |
|---|---|---|---|
| 100 SPS | 100$\mu$V (16 Bits) | 200$\mu$V (15 Bits) | 500$\mu$V (14 Bits) |
| 10 SPS | 10$\mu$V (20 Bits) | 20$\mu$V (19 Bits) | 50$\mu$V (18 Bits) |
| 1 SPS | 1$\mu$V (23 Bits) | 2$\mu$V (22 Bits) | 5$\mu$V (21 Bits) |

**Table 1 - Sensitivity and Resolution With 0-10V F.S.**

## PROGRAMMING CONVERSION TIME

Conversion time is programmed by writing an 8-bit word to the A/D converter. R/W should be placed in a logic 0. Program data are loaded on lines D0-D7 and the Enable command is strobed low per Figure 2.

Note setup and hold time of 10 nsec minimum before and after Enable and the 50 nsec minimum Enable pulse width.

The programmed conversion time ($T_C$) is related to an external clock ($F_{Clk}$) by the following formula. Clock frequencies up to 50MHz are acceptable.

$$T_C = \frac{1}{F_{Clk}} \times B \times 10^N$$

$$\text{For a 10MHz Crystal } T_C = \frac{1}{10^7} \times B \times 10^N$$

STEP 1: Select desired conversion (integration) time.
STEP 2: Multiply time base by $F_{Clk}$. The answer is B X $10^N$.
STEP 3: Choose B as large as possible within 1-16 range. Determine appropriate N.
STEP 4: Assemble program byte (with MSB = 1) selecting N & B from Table 2.

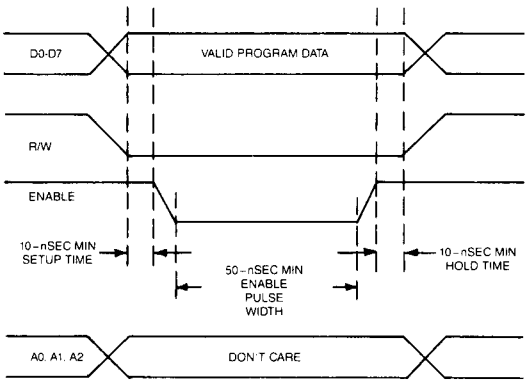



**Figure 2. WRITE Command Timing**

| MSB D7 | | D6 | D5 | D4 | | LSB D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| MSB | | N2 | N1 | N0 | | B3 | B2 | B1 | B0 |
| 0 | N= | N2 | N1 | N0 | B= | B3 | B2 | B1 | B0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 2 | 1 | 1 | 1 | 0 |
| | 2 | 0 | 1 | 0 | 3 | 1 | 1 | 0 | 1 |
| | 3 | 0 | 1 | 1 | 4 | 1 | 1 | 0 | 0 |
| | 4 | 1 | 0 | 0 | 5 | 1 | 0 | 1 | 1 |
| | 5 | 1 | 0 | 1 | 6 | 1 | 0 | 1 | 0 |
| | 6 | 1 | 1 | 0 | 7 | 1 | 0 | 0 | 1 |
| | 7 | 1 | 1 | 1 | 8 | 1 | 0 | 0 | 0 |
| | | | | | 9 | 0 | 1 | 1 | 1 |
| | | | | | 10 | 0 | 1 | 1 | 0 |
| | | | | | 11 | 0 | 1 | 0 | 1 |
| | | | | | 12 | 0 | 1 | 0 | 0 |
| | | | | | 13 | 0 | 0 | 1 | 1 |
| | | | | | 14 | 0 | 0 | 1 | 0 |
| | | | | | 15 | 0 | 0 | 0 | 1 |
| | | | | | 16 | 0 | 0 | 0 | 0 |

**Table 2 - Compiling the Conversion Time Byte.**

**Example 1**

1) For $T_C$ = 100 msec and $F_{Clk}$ = 10MHz
2) $T_C \times F_{Clk} = B \times 10^N$
   100 msec x 10 x $10^6$ = 10 x $10^5$
3) Choose N=5 B=10

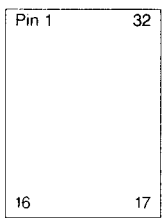
| | | MSB | N | B |
|---|---|---|---|---|
| 4) | Code | 0 | 101 | 0110 |

**Example 2**

1) For $T_C$ = 1 msec and $F_{Clk}$ = 10MHz
2) $T_C \times F_{Clk} = B \times .10^N$
   1 msec X 10 X $10^6$ = 10 X $10^3$
3) Choose N=3 B=10

| | | MSB | N | B |
|---|---|---|---|---|
| 4) | Code | 0 | 011 | 0110 |

## PIN DESIGNATIONS




| | | | |
|---|---|---|---|
| 1 | $V_{IN}$ | 32 | -15V |
| 2 | $I_{IN}$ | 31 | +15V |
| 3 | Offset Trim | 30 | Analog Ground |
| 4 | A2 | 29 | +5V (ANA) |
| 4 | A1 | 28 | $F_{OUT}$ -V/F Output Frequency |
| 6 | A0 | 27 | $F_{IN}$ -Input to Counter |
| 7 | D0 | 26 | R/W-Read/Write Select |
| 8 | D1 | 25 | Enable |
| 9 | D2 | 24 | DR-Data Ready |
| 10 | D3 | 23 | R-Reset |
| 11 | D4 | 22 | S-Start |
| 12 | D5 | 21 | CS/SS |
| 13 | D6 | 20 | CLK In |
| 14 | D7 | 19 | CLK Out |
| 15 | +5V (DIG) | 18 | Xtal |
| 16 | Digital Ground | 17 | Xtal |

## READING THE DATA

The MD2840/2841/2842 Series is capable of up to 24-bit measurements. These are read out on the 8-bit bus in three bytes. There are also overflow and programming bytes. The bytes are addressed at pin A0, A1, A2 per Table 3 via the timing commands in Figure 3.

To read data, set the R/W line to the logical "1" (high) state, and the A0, A1, A2 control lines to the appropriate states for the data byte desired. The order in which these signals are applied isn't important, as long as they are present and static for at least 10 nsec before the Enable (E) line is activated, and for a minimum of 10 nsec after Enable (E) is removed. The Enable line performs the actual read operation; it is a negative pulse, at least 50 nsec wide. Valid data is present on the output bus 30 nsec maximum after the leading edge of Enable; the data bus returns to a high impedance state 25 nsec maximum after the trailing edge of the Enable pulse.

| A0 | A1 | A2 | COMMAND | BYTE |
|---|---|---|---|---|
| 0 | 0 | 0 | READ | LOWER |
| 1 | 0 | 0 | READ | MIDDLE |
| 0 | 1 | 0 | READ | UPPER |
| 1 | 1 | 0 | READ | OVER-FLOW |
| 1 | 0 | 1 | READ | PROG BYTE |

**Table 3 - Addressing the data bytes.**

## OVERFLOW AND PROGRAMMING READBACK BYTES

If the 24-Bit counter overflows, the overflow bit ($D_0$) on the Overflow Byte (A = 110) will be in a high state. The data bits will roll over to zero and continue to count. Thus, using the overflow bit, it is possible to use the MD2840/2841/2842 Series as a 25-bit converter. See Table 3 and Figure 3 for commands and timing.

At any time the A/D can be interrogated as to its programmed status by reading the Program Readback Byte (A = 101). This will read back the conversion time program byte.

### OPTIONS

1. Offset voltage may be trimmed to zero using a 20KΩ potentiometer with drift less than 100ppm/°C.
2. Full Scale output can be trimmed to zero error using a 200Ω potentiometer with drift less than 100ppm/°C.
3. +5V (ANA) may be regulated for optimal performance using a National 78L05 (typical) +5V regulator.
4. An optical isolator or isolation transformer may be inserted between $F_{out}$ and $F_{in}$ to isolate the analog and digital sections of the A/D, if dictated by system requirements.
5. Clock frequency may come from a system clock, up to 50MHz maximum, applied to $CLK_{IN}$ (pin 20). Alternately an oscillator clock can be generated using a crystal (10MHz typical). $C_{Trim}$ may then be added to trim the crystal to the exact frequency desired. $C_{Trim}$ values between 2 and 25pF are typical.

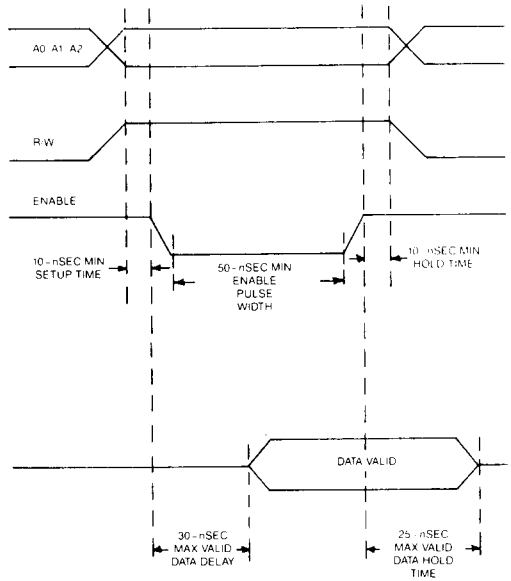



**Figure 3. READ Command Timing**

### NOTES:

**DR — Data Ready** — Generates a logical "1" that indicates that data has been latched and is ready to read. On Reset (pin 23) Data Ready becomes active high and remains high until a READ operation is performed.

**R — Reset** — When logical "0" is applied to pin 23 all operations are stopped and all counters and latches are reset to zero. A minimum pulse width of 100 nsec at logical 0 is requred.

**S — Start and CS/SS** — Continuous Sample /Synchronous Start — When CS/SS is low, the converter, after receiving a single start command, will continuously convert the input. When CS/SS is High, the converter will wait for a START command before beginning the next conversion. The START command is positive edge - triggered.

**+5V (DIG) and +5V (VFC)** may be supplied from the same +5V supply. See Option #3.

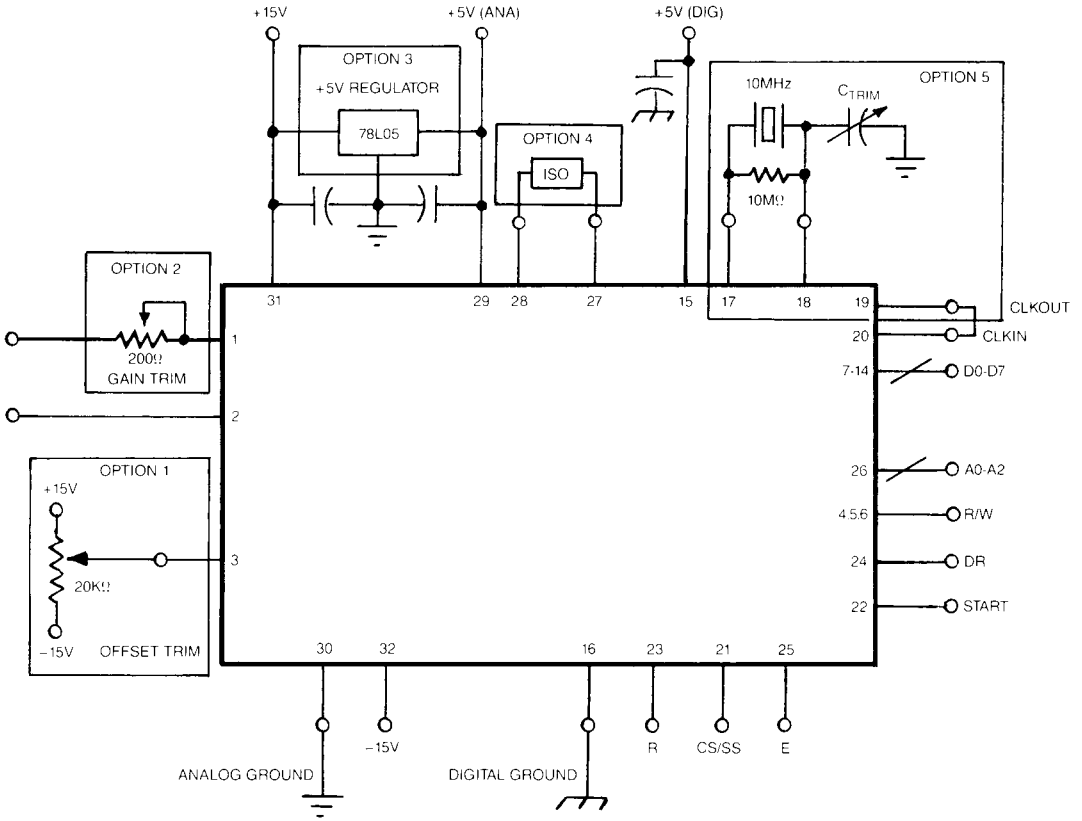
**$F_{out}$ and $F_{in}$** should be tied together for normal operation. $F_{out}$ can be used as a test point to check the output of the V/F. An optical isolator or isolation transformer may be inserted between $F_{out}$ and $F_{in}$ to totally isolate the analog and digital sections of the converter. See Option #4.

**CLK IN** Receives a system clock up to 50MHz. $CLK_{in}$ should be tied to $CLK_{out}$ if Crystal Oscillator Clock Circuit is used. See Option #5.

**Xtal** No connection if clock is supplied by System to pin 20 ($CLK_{in}$). For self-generated Crystal Clock See Option #5.

### ORDERING INFORMATION

**MD284020 Bits • 100 msec**
**MD284120 Bits • 200 msec**
**MD284220 Bits • 500 msec**




**Connection Diagram With Options**