

T6L92

Source Driver for TFT LCD Panels

The T6L92 is a 384-output channel TFT-LCD source driver IC for XGA and SXGA panel applications. The device incorporates Reduced Swing Differential Signaling (RSDS) to reduce EMI. It receives 9-bit differential data from the timing controller and generates output voltage for 64 grayscales. The T6L92 supplies 14 sections of voltage-reference for Gamma correction.

Features

- 6bit resolution : 64 grayscale levels
- Panel drive outputs : 384 outputs, R-DAC, reference analog voltage inputs
- High-speed operation : 85 MHz / 2.7V max
- Power supply voltage : Digital power supply voltage . . . 2.7 to 3.6 V
Analog power supply voltage . . . 6.5 to 15.5 V
- Operating temperature : -20 to 75°C
- Package : TCP / COF
- RSDS input interface for low EMI
- Multiple devices can be cascaded.

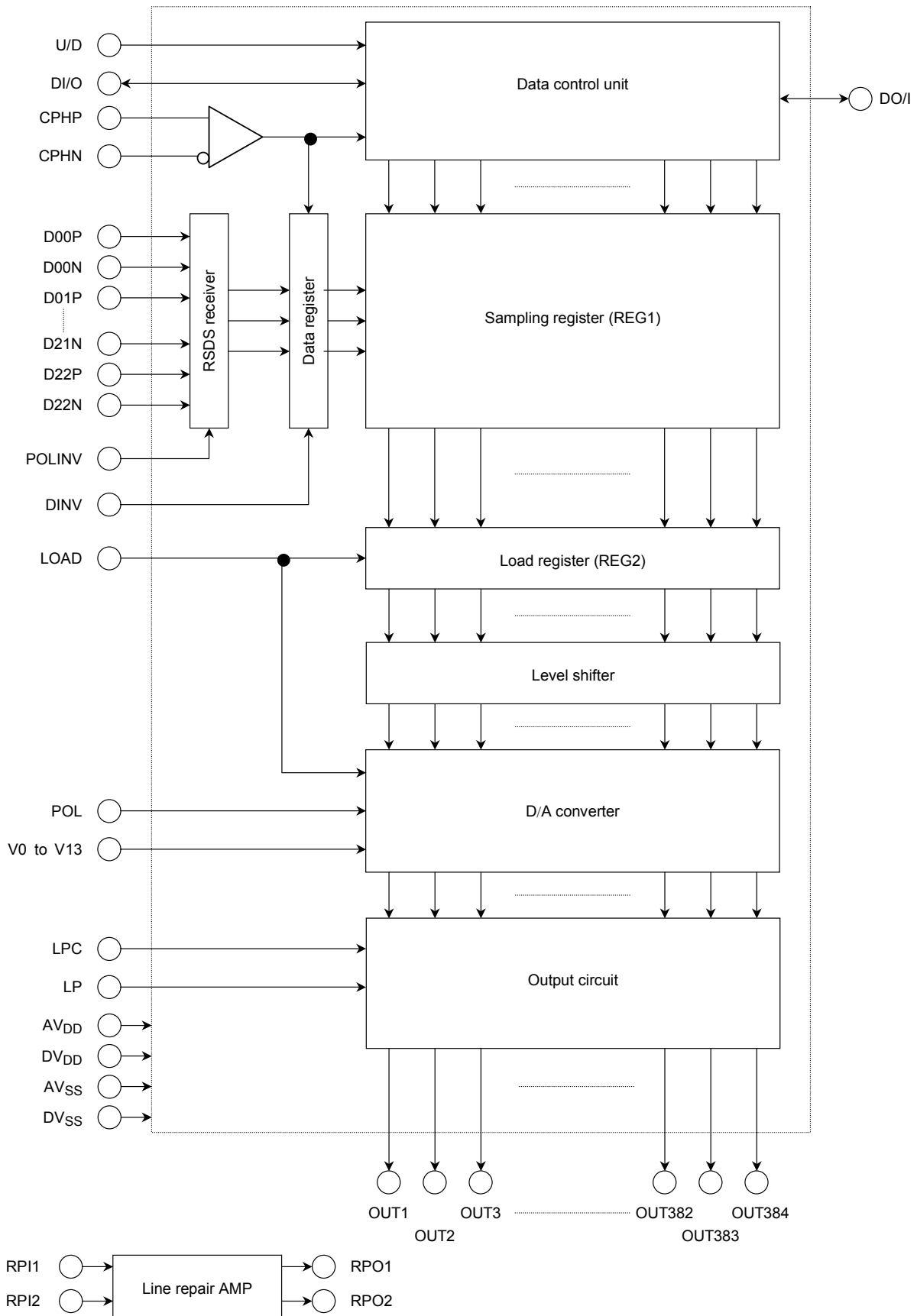
Unit: mm

T6L92	User Pitch Area	
	IN	OUT

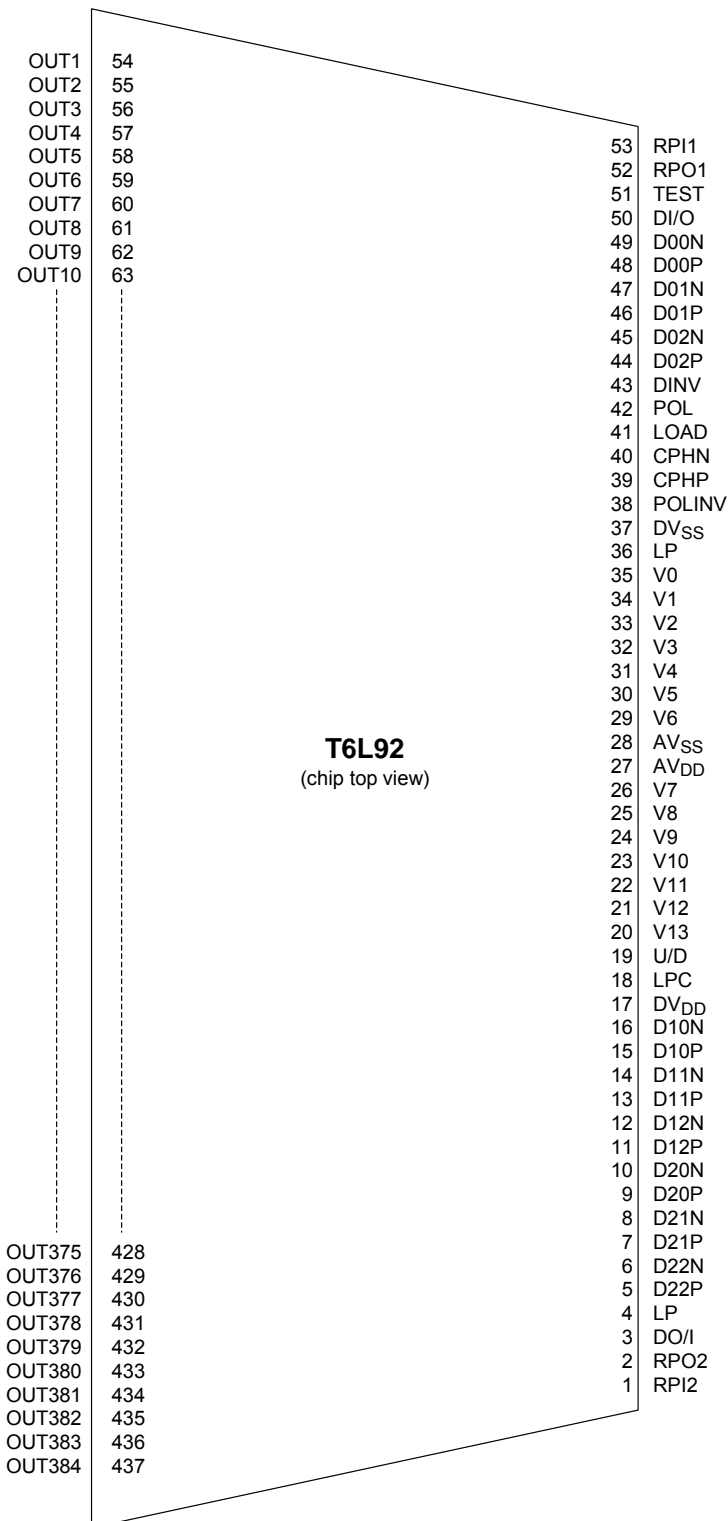
For the latest TCP specifications and product line-up, contact Toshiba or your local sales office.

TCP (Tape Carrier Package)

Block Diagram



Pin Assignment



The figure above shows an example of the pin assignment in the TCP/COF. It does not specify the pad layout on the chip. For the latest TCP/COF specifications, contact Toshiba or your local sales office.

Pin Functions

Pin Name	I/O	Function																
D/I/O DO/I	I/O	<p>Data transfer enable pin These pins, become active at high signal, initiating the transferred data into the sampling register of the device. One is configured as an input and the other is configured as an output of which directions are determined by U/D as shown below.</p> <table border="1"> <thead> <tr> <th>U/D</th> <th>D/I/O</th> <th>DO/I</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Input</td> <td>Output</td> </tr> <tr> <td>L</td> <td>Output</td> <td>Input</td> </tr> </tbody> </table> <p>When set for input A high on DI/O or DO/I is latched into the internal logic synchronously with the falling edge of CPH. When the internal circuit is in standby state, the device is ready to transfer data. The grayscale data is latched in sequentially, starting at the 2nd fall of CPH.</p> <p>When set for output The pin is used to transfer the enable signal to the T6L92 at the next stage of the LCD driver. The pin enters standby state after outputting a high.</p>	U/D	D/I/O	DO/I	H	Input	Output	L	Output	Input							
U/D	D/I/O	DO/I																
H	Input	Output																
L	Output	Input																
U/D	I	<p>Transfer direction select pin This pin controls the direction in which the data is transferred into the sampling register. Data is transferred synchronously with each rising edge of CPH in one of the following sequences: When U/D is high, data is transferred in the order OUT1 to OUT3, OUT4 to OUT6, OUT7 to OUT9, ... When U/D is low, the direction is reversed to give OUT382 to OUT384, OUT379 to OUT381, OUT376 to OUT378, ... The voltage applied to this pin must be a DC-level voltage that is either high or low.</p>																
CPHP/N	I	<p>Data transfer clock pin Transfers grayscale data. Sequentially latches grayscale data into REG1 in sync with each rising / falling edge of CPH.</p>																
D00P/N to D02P/N D10P/N to D12P/N D20P/N to D22P/N	I	<p>Grayscale data bus pins Inputs output data consisting of 6 bits for three channels (RGB) in one transfer.</p>																
DINV	I	<p>Data polarity inverting pin : DC-level input (Pull-down) Selects inversion or non-inversion of grayscale data bus at the rising edge of CPH. DINV = Low: Data bus not inverted DINV = High: Data bus inverted</p>																
POLINV	I	<p>Differential pins inverting pin (Pull-up) This signal controls the differential input pins inversion internal to the driver. POLINV = Low: The pin assignment of differential pair is inverted. (DxxP/DxxN→DxxN/ DxxP) POLINV = High: The pin assignment of differential pair is not inverted.</p>																
POL	I	<p>Polarity inverting pin Latches the input signal into the internal logic in sync with the rising edge of LOAD. POL = Low: The reference voltage for odd-numbered outputs is input from V7 to V13; for even-numbered outputs, V0 to V6. POL = High: The reference voltage for odd-numbered outputs is input from V0 to V6; for even-numbered outputs, V7 to V13.</p>																
LOAD	I	<p>Data load input pin After the data transfer enable pin (DO/I, DI/O) = "H" outputs, when a high voltage is supplied to the load input and latches the falling edge of CPH, the data in the sampling register is transferred to the load register. High level period of OUT1 to OUT384 is Hi-z state.</p>																
LP	I	<p>Low power control input pin (pull-up) The current consumption is lowered by controlling the constant current source of the output amplifier. In low power mode, the AV_{DD} of current consumption can be reduced. LP is pulled down to DV_{SS} in the LSI. (See page7) • LP = high : Nomal power mode • LP = low or open : Low power mode</p> <table border="1"> <thead> <tr> <th>Pin</th> <th colspan="2">LP= "L" or open</th> <th>LP= "H"</th> </tr> </thead> <tbody> <tr> <td>POL</td> <td>Switch</td> <td>No switch</td> <td>Don't care</td> </tr> <tr> <td>Output current (LOAD= "H")</td> <td>Reset</td> <td>No reset</td> <td>No reset</td> </tr> <tr> <td>OUT1 to OUT384 (LOAD= "H")</td> <td colspan="3">Hi-z</td> </tr> </tbody> </table>	Pin	LP= "L" or open		LP= "H"	POL	Switch	No switch	Don't care	Output current (LOAD= "H")	Reset	No reset	No reset	OUT1 to OUT384 (LOAD= "H")	Hi-z		
Pin	LP= "L" or open		LP= "H"															
POL	Switch	No switch	Don't care															
Output current (LOAD= "H")	Reset	No reset	No reset															
OUT1 to OUT384 (LOAD= "H")	Hi-z																	

Pin Name	I/O	Function
LPC	I	Low power control input pin (pull-down) <ul style="list-style-type: none"> • LPC = high : Low power mode (Analog current is about 30% to 50% lower.) • LPC = low or open : Nomal power mode
V0 to V13	I	Reference analog voltage input pins Externally input reference analog voltage inputs voltage. $AV_{SS} < V13 < V12 < V11 < \dots < V7 < AV_{DD} / 2, AV_{DD} / 2 < V6 < \dots < V2 < V1 < V0 < AV_{DD}$ or $AV_{SS} < V7 < V8 < V9 < \dots < V13 < AV_{DD} / 2, AV_{DD} / 2 < V0 < \dots < V4 < V5 < V6 < AV_{DD}$
OUT1 to OUT384	O	LCD panel drive pins
RPI1, RPI2	I	The Structure of the line-repair amp is the same as that of the analog output. RPI1 (RPI2) → impedance changed → RPO1 (RPO2)
RPO1, RPO2	O	
AV _{DD}		Analog power supply pin
DV _{DD}		Digital power supply pin
AV _{SS}		Analog GND pin
DV _{SS}		Digital GND pin
TEST	I	Test pin This pin should be left open or set to DV _{SS} level (pull-down).

Device Operation**(1) Starting data transfer**

A high input to the data transfer enable pin (DI/O or DO/I) is latched into the internal logic synchronously with the falling edge of CPH, setting the device ready to transfer data. The first data transfer starts at the second fall of CPH.

(*) See Timing Diagram 1

(2) Data transfer method

After the data is latched into the internal logic synchronously with the falling edge of CPH, the data is latched in from the grayscale bus to the sampling register synchronously with each rising / falling edge of CPH.

Grayscale data are written as three outputs in parallel during one transfer. Data transfer completes after 128 transfers. Then the device enters Standby mode.

(*) See Timing Diagram 1

(3) Terminating data transfer

The data transfer enable pin (DO/I or DI/O) output goes high synchronously with the falling edge of CPH two clock period before the last data is latched in. It is held high until the next rise of CPH (see Timing diagram 1 and 2).

The output from this pin can be connected directly as input to the data transfer enable pin (DI/O or DO/I) of the next stage LCD driver. In this way, multiple devices can be easily cascaded to drive a large screen.

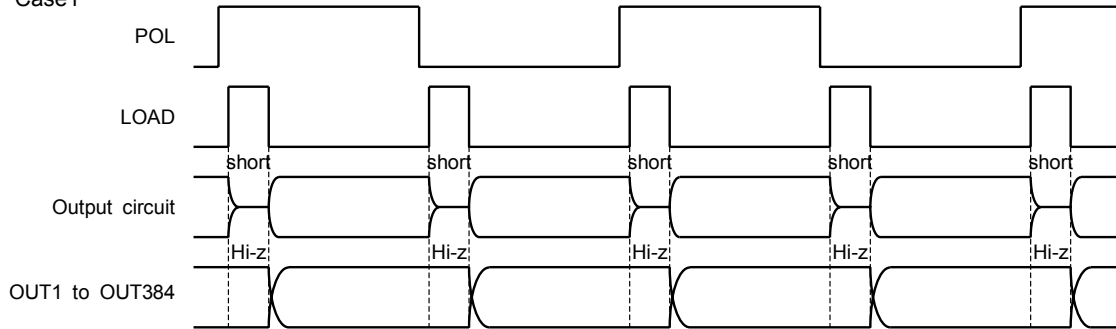
(*) See Timing Diagram 1

(4) Panel drive output

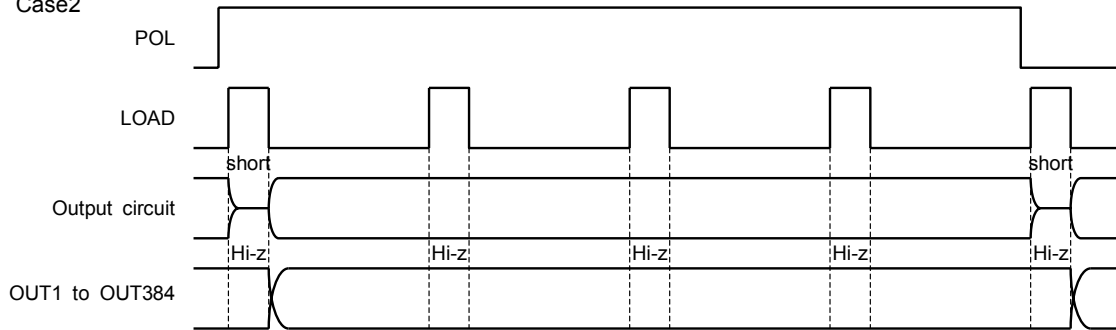
After the data transfer enable pin (DO/I, DI/O) = H outputs, when a high voltage is supplied to the load input, the data in the sampling register (REG1) are transferred to the load register (REG2). The device starts updating output to the LCD panel drive pins at the falling edge of LOAD. LCD panel driver pins are Hi-z during LOAD = high. When LP is low, and when the level at which POL is latched into the internal logic differs from the level latched in one LOAD period before, the odd output circuit and even circuit are short (Ex. OUT1 and OUT2, OUT3 and OUT4, ... , OUT383 and OUT384).

• LP = "L"

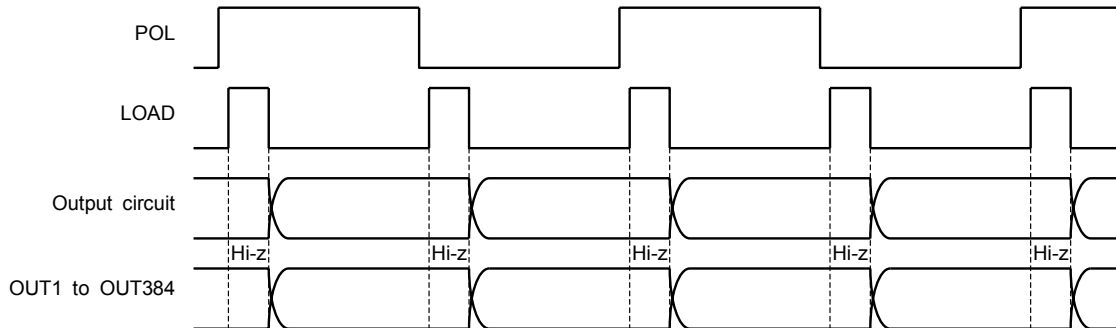
Case1



Case2

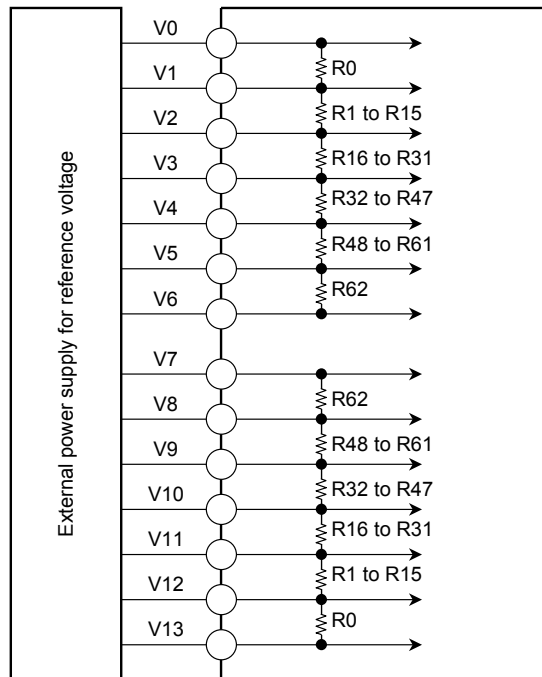


• LP = "H"



(5) Reference power supply circuit

The D/A converter is comprised of ladder resistors and switches.



• **Resistors between power supply pins for reference analog voltage inputs**

Unit (Ω)

Resistor Name	Resistance Value (Ω)	Resistor Name	Resistance Value (Ω)	Resistor Name	Resistance Value (Ω)	Resistor Name	Resistance Value (Ω)
R ₀	800	R ₁₆	300	R ₃₂	100	R ₄₈	100
R ₁	750	R ₁₇	250	R ₃₃	100	R ₄₉	100
R ₂	700	R ₁₈	250	R ₃₄	100	R ₅₀	100
R ₃	650	R ₁₉	250	R ₃₅	100	R ₅₁	100
R ₄	600	R ₂₀	200	R ₃₆	100	R ₅₂	100
R ₅	550	R ₂₁	200	R ₃₇	100	R ₅₃	150
R ₆	550	R ₂₂	200	R ₃₈	100	R ₅₄	150
R ₇	500	R ₂₃	150	R ₃₉	100	R ₅₅	150
R ₈	500	R ₂₄	150	R ₄₀	100	R ₅₆	200
R ₉	400	R ₂₅	150	R ₄₁	100	R ₅₇	200
R ₁₀	400	R ₂₆	150	R ₄₂	100	R ₅₈	250
R ₁₁	350	R ₂₇	100	R ₄₃	100	R ₅₉	250
R ₁₂	350	R ₂₈	100	R ₄₄	100	R ₆₀	300
R ₁₃	350	R ₂₉	100	R ₄₅	100	R ₆₁	500
R ₁₄	300	R ₃₀	100	R ₄₆	100	R ₆₂	800
R ₁₅	300	R ₃₁	100	R ₄₇	100		

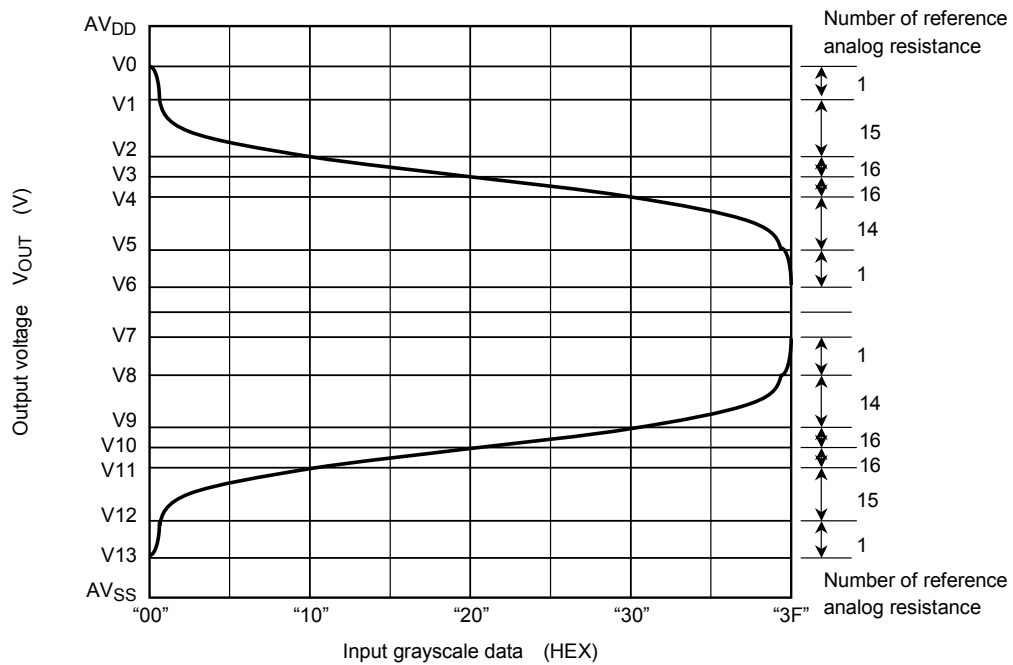
(6) Relationship between grayscale data and output voltage

The output voltage is determined according to the grayscale data values and the 14 power supply voltages for reference analog voltage inputs.

Grayscale Data	Output
D00P/N to D02P/N	OUT (3m - 2)
D10P/N to D12P/N	OUT (3m - 1)
D20P/N to D22P/N	OUT (3m)

(*) m = 1, 2, 3, ..., 126, 127, 128

● **Schematic of reference analog voltage inputs**



DINV = low level, POLINV = high level

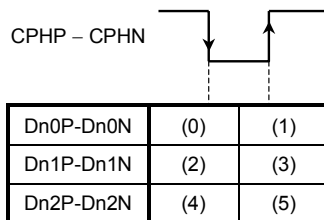
$AV_{SS} < V_{13} < V_{12} < V_{11} < \dots < V_7 < AV_{DD} / 2$, $AV_{DD} / 2 < V_6 < \dots < V_2 < V_1 < V_0 < AV_{DD}$
 or $AV_{SS} < V_7 < V_8 < V_9 < \dots < V_{13} < AV_{DD} / 2$, $AV_{DD} / 2 < V_0 < \dots < V_4 < V_5 < V_6 < AV_{DD}$

- Relationship 1 between grayscale data and output voltage (grayscale data: 00H to 1FH)

(NOTE)

Grayscale Data	(5)	(4)	(3)	(2)	(1)	(0)	Output Voltage			
							Positive polarity		Negative polarity	
00H	0	0	0	0	0	0	V00H'	V0	V00H'	V13
01H	0	0	0	0	0	1	V01H'	V1	V01H'	V12
02H	0	0	0	0	1	0	V22H'	$V1 + (V2 - V1) \times 750/7250$	V22H'	$V12 + (V11 - V12) \times 750/7250$
03H	0	0	0	0	1	1	V23H'	$V1 + (V2 - V1) \times 1450/7250$	V23H'	$V12 + (V11 - V12) \times 1450/7250$
04H	0	0	0	1	0	0	V24H'	$V1 + (V2 - V1) \times 2100/7250$	V24H'	$V12 + (V11 - V12) \times 2100/7250$
05H	0	0	0	1	0	1	V25H'	$V1 + (V2 - V1) \times 2700/7250$	V25H'	$V12 + (V11 - V12) \times 2700/7250$
06H	0	0	0	1	1	0	V26H'	$V1 + (V2 - V1) \times 3250/7250$	V26H'	$V12 + (V11 - V12) \times 3250/7250$
07H	0	0	0	1	1	1	V27H'	$V1 + (V2 - V1) \times 3800/7250$	V27H'	$V12 + (V11 - V12) \times 3800/7250$
08H	0	0	1	0	0	0	V28H'	$V1 + (V2 - V1) \times 4300/7250$	V28H'	$V12 + (V11 - V12) \times 4300/7250$
09H	0	0	1	0	0	1	V29H'	$V1 + (V2 - V1) \times 4800/7250$	V29H'	$V12 + (V11 - V12) \times 4800/7250$
0AH	0	0	1	0	1	0	V2AH'	$V1 + (V2 - V1) \times 5200/7250$	V2AH'	$V12 + (V11 - V12) \times 5200/7250$
0BH	0	0	1	0	1	1	V2BH'	$V1 + (V2 - V1) \times 5600/7250$	V2BH'	$V12 + (V11 - V12) \times 5600/7250$
0CH	0	0	1	1	0	0	V2CH'	$V1 + (V2 - V1) \times 5950/7250$	V2CH'	$V12 + (V11 - V12) \times 5950/7250$
0DH	0	0	1	1	0	1	V2DH'	$V1 + (V2 - V1) \times 6300/7250$	V2DH'	$V12 + (V11 - V12) \times 6300/7250$
0EH	0	0	1	1	1	0	V2EH'	$V1 + (V2 - V1) \times 6650/7250$	V2EH'	$V12 + (V11 - V12) \times 6650/7250$
0FH	0	0	1	1	1	1	V2FH'	$V1 + (V2 - V1) \times 6950/7250$	V2FH'	$V12 + (V11 - V12) \times 6950/7250$
10H	0	1	0	0	0	0	V10H'	V2	V10H'	V11
11H	0	1	0	0	0	1	V11H'	$V2 + (V3 - V2) \times 300/2750$	V11H'	$V11 + (V10 - V11) \times 300/2750$
12H	0	1	0	0	1	0	V12H'	$V2 + (V3 - V2) \times 550/2750$	V12H'	$V11 + (V10 - V11) \times 550/2750$
13H	0	1	0	0	1	1	V13H'	$V2 + (V3 - V2) \times 800/2750$	V13H'	$V11 + (V10 - V11) \times 800/2750$
14H	0	1	0	1	0	0	V14H'	$V2 + (V3 - V2) \times 1050/2750$	V14H'	$V11 + (V10 - V11) \times 1050/2750$
15H	0	1	0	1	0	1	V15H'	$V2 + (V3 - V2) \times 1250/2750$	V15H'	$V11 + (V10 - V11) \times 1250/2750$
16H	0	1	0	1	1	0	V16H'	$V2 + (V3 - V2) \times 1450/2750$	V16H'	$V11 + (V10 - V11) \times 1450/2750$
17H	0	1	0	1	1	1	V17H'	$V2 + (V3 - V2) \times 1650/2750$	V17H'	$V11 + (V10 - V11) \times 1650/2750$
18H	0	1	1	0	0	0	V18H'	$V2 + (V3 - V2) \times 1800/2750$	V18H'	$V11 + (V10 - V11) \times 1800/2750$
19H	0	1	1	0	0	1	V19H'	$V2 + (V3 - V2) \times 1950/2750$	V19H'	$V11 + (V10 - V11) \times 1950/2750$
1AH	0	1	1	0	1	0	V1AH'	$V2 + (V3 - V2) \times 2100/2750$	V1AH'	$V11 + (V10 - V11) \times 2100/2750$
1BH	0	1	1	0	1	1	V1BH'	$V2 + (V3 - V2) \times 2250/2750$	V1BH'	$V11 + (V10 - V11) \times 2250/2750$
1CH	0	1	1	1	0	0	V1CH'	$V2 + (V3 - V2) \times 2350/2750$	V1CH'	$V11 + (V10 - V11) \times 2350/2750$
1DH	0	1	1	1	0	1	V1DH'	$V2 + (V3 - V2) \times 2450/2750$	V1DH'	$V11 + (V10 - V11) \times 2450/2750$
1EH	0	1	1	1	1	0	V1EH'	$V2 + (V3 - V2) \times 2550/2750$	V1EH'	$V11 + (V10 - V11) \times 2550/2750$
1FH	0	1	1	1	1	1	V1FH'	$V2 + (V3 - V2) \times 2650/2750$	V1FH'	$V11 + (V10 - V11) \times 2650/2750$

(NOTE)



(See Page13)

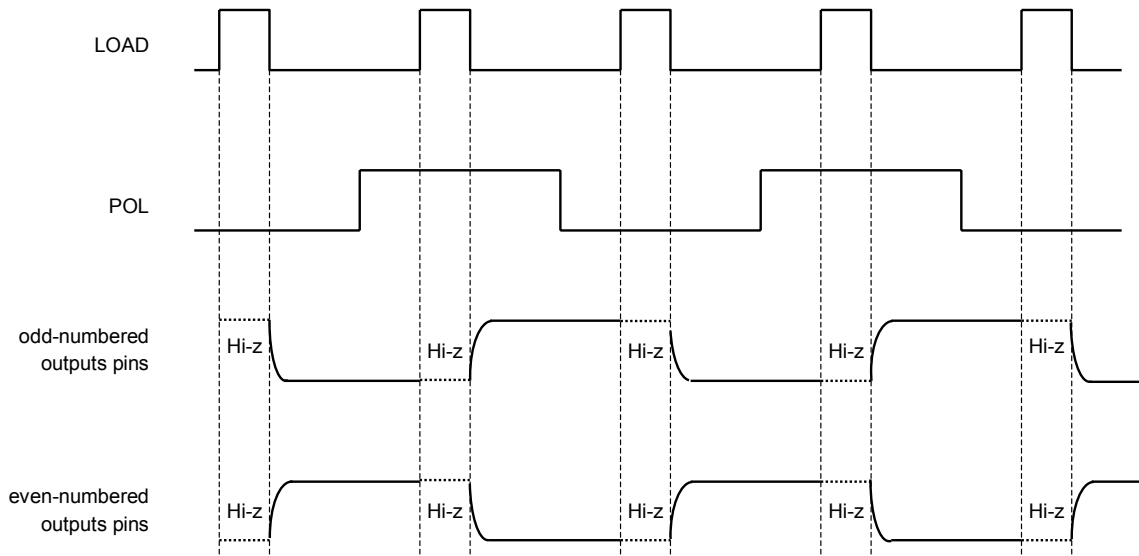
(*) n = 0, 1, 2

- Relationship 2 between grayscale data and output voltage (grayscale data: 20H to 3FH)

(NOTE)

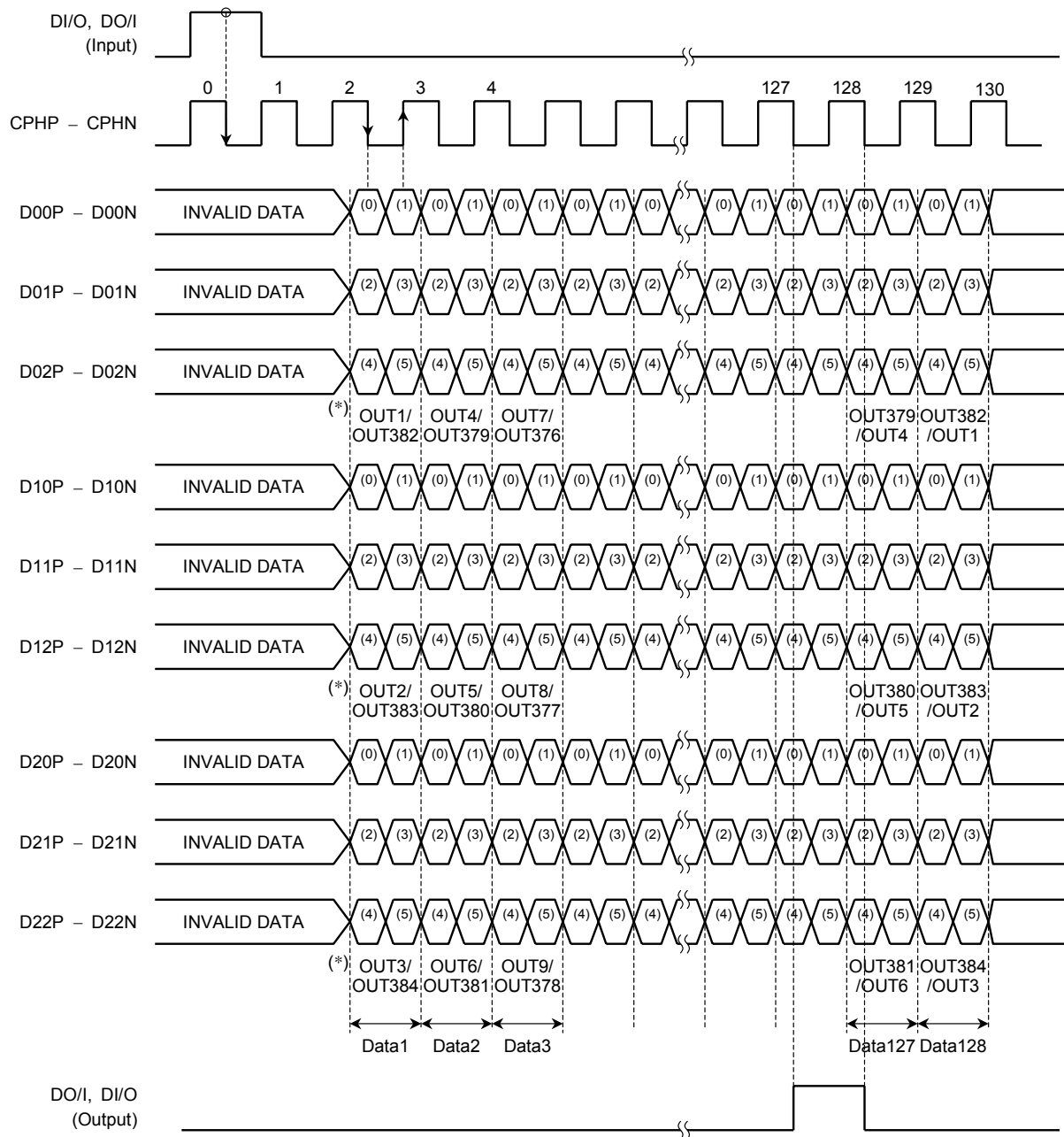
Grayscale Data	(5)	(4)	(3)	(2)	(1)	(0)	Output Voltage			
							Positive polarity		Negative polarity	
20H	1	0	0	0	0	0	V20H	V3	V20H'	V10
21H	1	0	0	0	0	1	V21H	$V3 + (V4 - V3) \times 100/1600$	V21H'	$V10 + (V9 - V10) \times 100/1600$
22H	1	0	0	0	1	0	V22H	$V3 + (V4 - V3) \times 200/1600$	V22H'	$V10 + (V9 - V10) \times 200/1600$
23H	1	0	0	0	1	1	V23H	$V3 + (V4 - V3) \times 300/1600$	V23H'	$V10 + (V9 - V10) \times 300/1600$
24H	1	0	0	1	0	0	V24H	$V3 + (V4 - V3) \times 400/1600$	V24H'	$V10 + (V9 - V10) \times 400/1600$
25H	1	0	0	1	0	1	V25H	$V3 + (V4 - V3) \times 500/1600$	V25H'	$V10 + (V9 - V10) \times 500/1600$
26H	1	0	0	1	1	0	V26H	$V3 + (V4 - V3) \times 600/1600$	V26H'	$V10 + (V9 - V10) \times 600/1600$
27H	1	0	0	1	1	1	V27H	$V3 + (V4 - V3) \times 700/1600$	V27H'	$V10 + (V9 - V10) \times 700/1600$
28H	1	0	1	0	0	0	V28H	$V3 + (V4 - V3) \times 800/1600$	V28H'	$V10 + (V9 - V10) \times 800/1600$
29H	1	0	1	0	0	1	V29H	$V3 + (V4 - V3) \times 900/1600$	V29H'	$V10 + (V9 - V10) \times 900/1600$
2AH	1	0	1	0	1	0	V2AH	$V3 + (V4 - V3) \times 1000/1600$	V2AH'	$V10 + (V9 - V10) \times 1000/1600$
2BH	1	0	1	0	1	1	V2BH	$V3 + (V4 - V3) \times 1100/1600$	V2BH'	$V10 + (V9 - V10) \times 1100/1600$
2CH	1	0	1	1	0	0	V2CH	$V3 + (V4 - V3) \times 1200/1600$	V2CH'	$V10 + (V9 - V10) \times 1200/1600$
2DH	1	0	1	1	0	1	V2DH	$V3 + (V4 - V3) \times 1300/1600$	V2DH'	$V10 + (V9 - V10) \times 1300/1600$
2EH	1	0	1	1	1	0	V2EH	$V3 + (V4 - V3) \times 1400/1600$	V2EH'	$V10 + (V9 - V10) \times 1400/1600$
2FH	1	0	1	1	1	1	V2FH	$V3 + (V4 - V3) \times 1500/1600$	V2FH'	$V10 + (V9 - V10) \times 1500/1600$
30H	1	1	0	0	0	0	V30H	V4	V30H'	V9
31H	1	1	0	0	0	1	V31H	$V4 + (V5 - V4) \times 100/2650$	V31H'	$V9 + (V8 - V9) \times 100/2650$
32H	1	1	0	0	1	0	V32H	$V4 + (V5 - V4) \times 200/2650$	V32H'	$V9 + (V8 - V9) \times 200/2650$
33H	1	1	0	0	1	1	V33H	$V4 + (V5 - V4) \times 300/2650$	V33H'	$V9 + (V8 - V9) \times 300/2650$
34H	1	1	0	1	0	0	V34H	$V4 + (V5 - V4) \times 400/2650$	V34H'	$V9 + (V8 - V9) \times 400/2650$
35H	1	1	0	1	0	1	V35H	$V4 + (V5 - V4) \times 500/2650$	V35H'	$V9 + (V8 - V9) \times 500/2650$
36H	1	1	0	1	1	0	V36H	$V4 + (V5 - V4) \times 650/2650$	V36H'	$V9 + (V8 - V9) \times 650/2650$
37H	1	1	0	1	1	1	V37H	$V4 + (V5 - V4) \times 800/2650$	V37H'	$V9 + (V8 - V9) \times 800/2650$
38H	1	1	1	0	0	0	V38H	$V4 + (V5 - V4) \times 950/2650$	V38H'	$V9 + (V8 - V9) \times 950/2650$
39H	1	1	1	0	0	1	V39H	$V4 + (V5 - V4) \times 1150/2650$	V39H'	$V9 + (V8 - V9) \times 1150/2650$
3AH	1	1	1	0	1	0	V3AH	$V4 + (V5 - V4) \times 1350/2650$	V3AH'	$V9 + (V8 - V9) \times 1350/2650$
3BH	1	1	1	0	1	1	V3BH	$V4 + (V5 - V4) \times 1600/2650$	V3BH'	$V9 + (V8 - V9) \times 1600/2650$
3CH	1	1	1	1	0	0	V3CH	$V4 + (V5 - V4) \times 1850/2650$	V3CH'	$V9 + (V8 - V9) \times 1850/2650$
3DH	1	1	1	1	0	1	V3DH	$V4 + (V5 - V4) \times 2150/2650$	V3DH'	$V9 + (V8 - V9) \times 2150/2650$
3EH	1	1	1	1	1	0	V3EH	V5	V3EH'	V8
3FH	1	1	1	1	1	1	V3FH	V6	V3FH'	V7

- LOAD, POL, and output waveforms



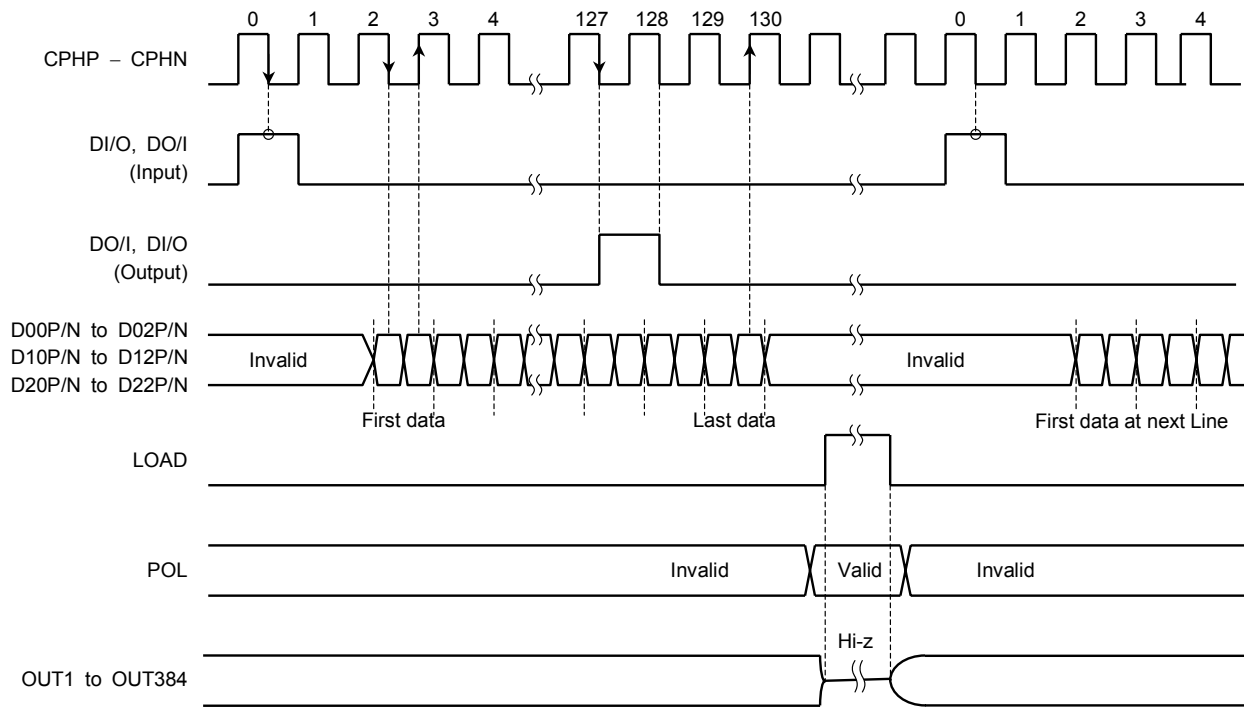
POL	odd-numbered outputs pins	even-numbered outputs pins
H	V0 to V6	V7 to V13
L	V7 to V13	V0 to V6

Timing Diagrams 1



(*) Upper stage : OUT1 → U/D = High level
 Lower stage : OUT382 → U/D = Low level

Timing Diagrams 2



Absolute Maximum Ratings (DV_{SS} = AV_{SS} = 0 V)

Characteristics	Symbol	Rating	Unit	Relevant Pin
Digital supply voltage	DV _{DD}	-0.3 to 4.0	V	
Analog supply voltage	AV _{DD}	-0.3 to 16.5	V	
Input voltage	V _{IN}	-0.3 to DV _{DD} + 0.3	V	
Reference analog voltage	V (0:13)	-0.3 to AV _{DD} + 0.3	V	V0~V13
Output voltage	V _{OUT}	-0.3 to DV _{DD} + 0.3	V	DI/O, DO/I
Storage temperature	T _{stg}	-55 to 125	°C	

Recommended Operating Conditions (DV_{SS} = AV_{SS} = 0 V)

Characteristics	Symbol	Test Condition	Rating	Unit	Relevant Pin
Digital supply voltage	DV _{DD}	—	2.7 to 3.6	V	
Analog supply voltage	AV _{DD}	—	6.5 to 15.5	V	
Reference analog voltage-1	V0 to V6	—	AV _{DD} - 0.1 to AV _{DD} / 2	V	
Reference analog voltage-2	V7 to V13	—	AV _{DD} / 2 to AV _{SS} + 0.1	V	
Operating temperature	T _{opr}	—	-20 to 75	°C	
Operating frequency	f _{CPH}		85 (max)	MHz	CPHP/N
Output load capacitance	C _L	—	150 (max)	pF/PIN	OUT1 to OUT384

Electrical Characteristics

DC Characteristics

(DV_{SS} = AV_{SS} = 0 V, DV_{DD} = 2.7 to 3.6 V, AV_{DD} = 6.5 V to 15.5 V, Ta = -20 to 75°C)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Max	Unit	Applicable Pin
Input voltage	Low level	V _{IL}	—	—	0	0.3 × DV _{DD}	V	(Note1)
	High level	V _{IH}		—	0.7 × DV _{DD}	DV _{DD}		
	Low level	V _{IL}		—	0	0.2 × DV _{DD}		DINV POLINV LP LPC
	High level	V _{IH}		—	0.8 × DV _{DD}	DV _{DD}		
Output voltage	Low level	V _{OL}	—	I _{OL} = 1 mA	0	0.4	V	DI/O, DO/I
	High level	V _{OH}		I _{OH} = -1 mA	DV _{DD} - 0.4	DV _{DD}		
Output voltage range		V _{DO}	—	—	0.1	AV _{DD} - 0.1	V	OUT1 to OUT384
Output voltage deviation	ΔV _O	—	—	AV _{DD} = 13.0 V, DV _{DD} = 3.0 V V _{OUT} = 2.0 to 11.0 V	—	±20	mV	OUT1 to OUT384
				AV _{DD} = 13.0 V, DV _{DD} = 3.0 V V _{OUT} = 0.9 to 2.0 V, V _{OUT} = 11.0 to 12.9 V	—	±30		
				AV _{DD} = 13.0 V, DV _{DD} = 3.0 V V _{OUT} = 0.1 to 0.9 V, V _{OUT} = 11.0 to 12.9 V	—	±40		
Average output amplitude voltage deviation between chips		ΔV _{DO}	—	AV _{DD} = 13.0 V, 32G/S	—	±7.5	mV	OUT1 to OUT384
Output amplitude voltage deviation (1)	ΔV _{p-p} (Note2)	—	—	AV _{DD} = 13.0 V, DV _{DD} = 3.0 V V _{OUT} = 0.1 to 0.8 V, V _{OUT} = 12.2 to 12.9 V	—	±30	mV	OUT1 to OUT384
				AV _{DD} = 13.0 V, DV _{DD} = 3.0 V V _{OUT} = 0.8 to 1.2 V, V _{OUT} = 11.8 to 12.2 V	—	±20		
				AV _{DD} = 13.0 V, DV _{DD} = 3.0 V V _{OUT} = 1.2 to 11.8 V	—	±10		
Output amplitude voltage deviation (2)		ΔV _{p-p} (Note2)	—	—	—	±30	mV	RPO1, RPO2
Gamma resistance fluctuation		R _γ	—	—	11095	20605	Ω	V0 to V13
Input leakage current		I _{CC}	—	—	-1	1	μA	(Note3)
Pull-down resistance		R _{iL}	—	—	—	150	kΩ	DINV / TEST LPC
Pull-up resistance		R _{iH}	—	—	—	200	kΩ	POLINV / LP
Current dissipation (1)		D _I DD	—	DV _{DD} = 3.0 V, f _{CPH} = 65 MHz, f _{LOAD} = 50 kHz, data pattern: 101010...	—	5	mA	DV _{DD}
Current dissipation (2)		A _I DD	—	(Note 4)	—	8	mA	AV _{DD}
Output current	I _{OLy} (Note5)	—	—	AV _{DD} = 8.0 V V _{OUT} = 4.0 V, V _{FORCE} = 1.0 V	0.4	—	mA	OUT1 to OUT384 RPO1, RPO2
	I _{OHy} (Note5)			AV _{DD} = 8.0 V V _{OUT} = 4.0 V, V _{FORCE} = 7.0 V	—	-0.4		

Note1: DI/O, DO/I, LOAD, POL

Note2: ΔV_{p-p} = max value of (ΔV_{p-p}H - ΔV_{p-p}L)

ΔV_{p-p}H : the gray level positive polarity driver output voltage deviation

ΔV_{p-p}L : the gray level negative polarity driver output voltage deviation

Note3: D00P/N to D02P/N, D10P/N to D12P/N, D20P/N to D22P/N, DI/O, DO/I, CPHP/N, LOAD, U/D, POL

Note4: $AV_{DD} = 10\text{ V}$, $DV_{DD} = 3.3\text{ V}$, $f_{CPH} = 65\text{ MHz}$, $f_{LOAD} = 50\text{ kHz}$, $f_{POL} = f_{LOAD} / 2 = 25\text{ kHz}$, no load, data pattern: 00000..., $V_2 = 9.5\text{ V}$, $V_{13} = 0.5\text{ V}$, LP = "H", LPC = "L"

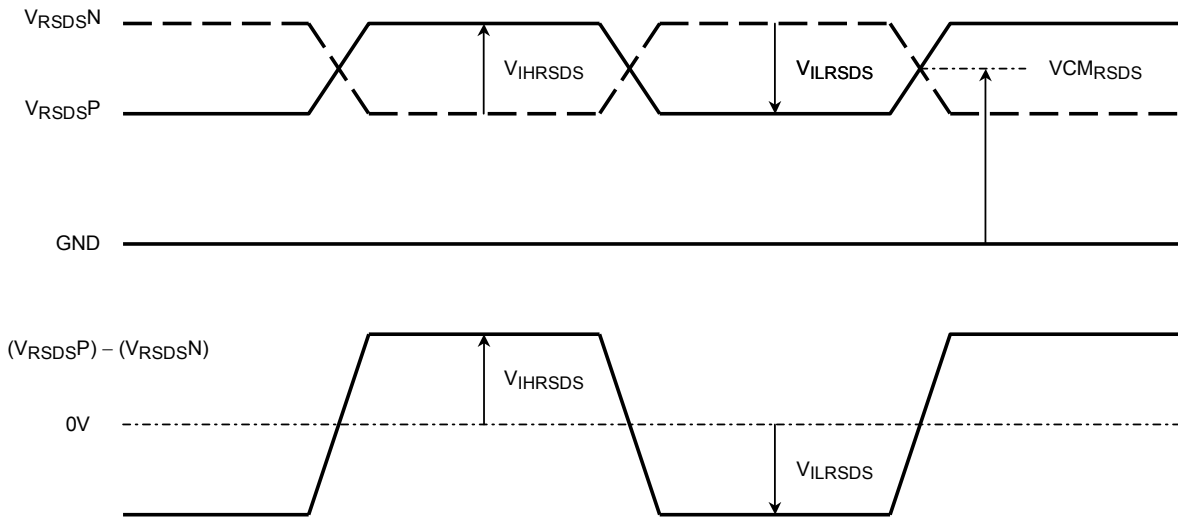
Note5: V_{OUT} is the voltage applied to analog output pins OUT1 to OUT384.
 V_{FORCE} is the output voltage of analog output pins OUT1 to OUT384.

RSDS Characteristics

Characteristics		Symbol	Test Circuit	Test Condition	Min	Max	Unit	Applicable Pin
RSDS input voltage	High level	V_{IHRSDS}	—	$V_{CMRSDS} = 1.2\text{ V}$	100	400	mV	D00P/N to D23P/N, CPHP/N
	Low level	V_{ILRSDS}			- 400	- 100		
RSDS common mode input voltage range		V_{CMRSDS} (Note6)	—	$V_{DIFFRSDS} = 200\text{ mV}$ (Note7)	0.7	1.4	V	

Note6: $V_{CMRSDS} = (V_{CPHP} + V_{CPHN}) / 2$ or $V_{CMRSDS} = (V_{DxxP} + V_{DxxN}) / 2$

Note7: $V_{DIFFRSDS} = V_{CPHP} - V_{CPHN}$ or $V_{DIFFRSDS} = V_{DxxP} - V_{DxxN}$
 The typical RSDS swing level of peak to peak is 400 mV.



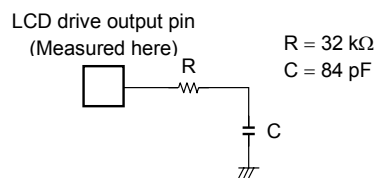
RSDS Signal definition

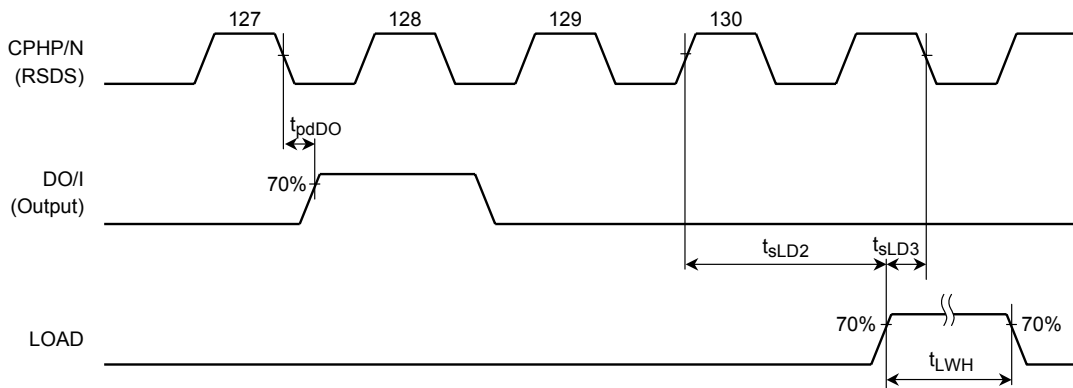
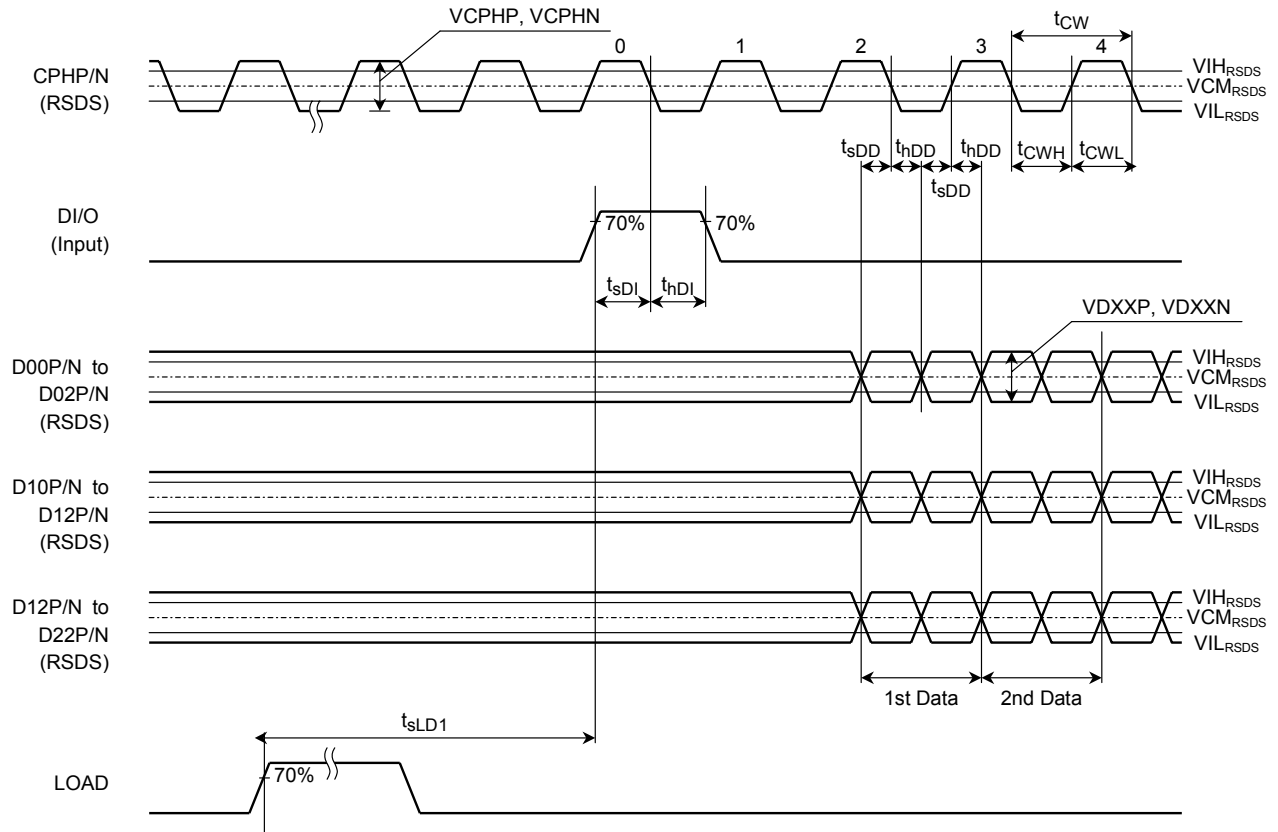
AC Characteristics

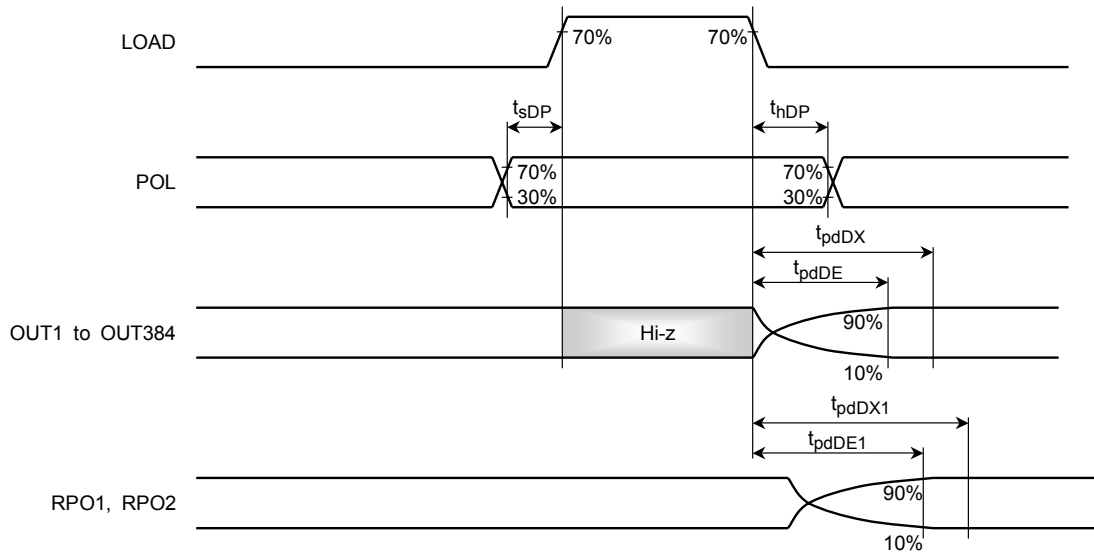
$DV_{SS} = AV_{SS} = 0\text{ V}$, $DV_{DD} = 2.7\text{ to }3.6\text{ V}$, $AV_{DD} = 6.5\text{ V to }15.5\text{ V}$, $T_a = -20\text{ to }75^\circ\text{C}$
 $VCM_{RSDS} = 1.2\text{V}$, $VDIFF_{RSDS} = 200\text{mV}$

Characteristics	Symbol	Test Circuit	Test Condition	Min	Max	Unit	
CPH pulse width	t_{CW}	—	—	12	—	ns	
CPH pulse width H	t_{CWH}	—	—	6	—	ns	
CPH pulse width L	t_{CWL}	—	—	6	—	ns	
Data setup time	t_{sDD}	—	—	2	—	ns	
Data hold time	t_{hDD}	—	—	0	—	ns	
Enable setup time	t_{sDI}	—	—	1	—	ns	
Enable hold time	t_{hDI}	—	—	2	—	ns	
LOAD high period	t_{LWH}	—	LP = "H" : Normal power mode	5	—	CPH cycle	
			LP = "L" : Low power mode	0.5	—	μs	
LOAD enable input period	t_{sLD1}	—	—	5	—	CPH cycle	
LOAD enable output period	t_{sLD2}	—	—	1	—	CPH cycle	
LOAD setup time	t_{sLD3}	—	—	4	—	ns	
Enable output delay time	t_{pdDO}	—	$C_L = 15\text{ pF}$	—	10	ns	
POL setup time	t_{sDP}	—	—	14	—	ns	
POL hold time	t_{hDP}	—	—	10	—	ns	
Output delay time 1	t_{pdDE}	—	Target output voltage $\times 0.9$ (Note 8)	LPC = "L"	—	3	μs
				LPC = "H"	—	5	
Output delay time 2	t_{pdDX}	—	Target output voltage $\pm \Delta V_O$ (Note 8)	LPC = "L"	—	5	μs
				LPC = "H"	—	7	
Output delay time 3	t_{pdDE1}	—	$C_L = 150\text{ pF}$	—	4	μs	
Output delay time 4	t_{pdDX1}	—	$C_L = 150\text{ pF}$	—	6	μs	

Note8: Output load condition







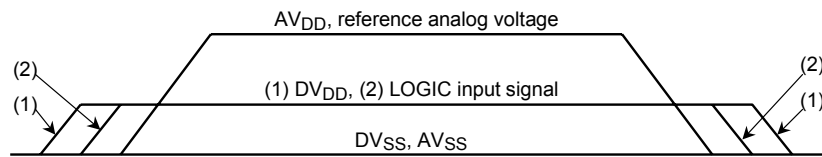
Power-On Sequence

At power ON, the sequence is: DVDD → LOGIC input signal → AVDD, reference analog voltage

At power OFF, the sequence is the reverse of that for power ON.

Turn ON/OFF power supplies for AVDD and reference analog voltage inputs simultaneously.

As long as the voltage condition $AVDD > DVDD$ is satisfied, all power supplies can be turned OFF simultaneously.



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