

CXM3559ER

The CXM3559ER is a SP9T antenna switch module for GSM/UMTS Dual-mode handset. The CXM3559ER has a built-in dual low pass filter and a +1.8 V CMOS compatible Decoder. The Sony GaAs junction gate pHEMT (JPHEMT) MMIC process is used for low insertion loss and linearity. The device has low BOM with no DC blocking capacitor.
(Application: Quad band GSM and triple band UMTS or CDMA dual-mode handset)

Features

- ◆ Low insertion loss: 0.90 dB (Typ.) On Tx1 (GSM Low band Tx)
 0.75 dB (Typ.) On Tx2 (GSM High band Tx)
- ◆ High attenuation: 28 dB (Min.) On Tx1 path @1648-1830 MHz
 25 dB (Min.) On Tx2 path @3420-3820 MHz
- ◆ RXs paths are changeable for band assignment
- ◆ Low voltage operation: $V_{DD} = +2.5\text{ V}$
- ◆ No DC blocking capacitors (Small device footprint)
- ◆ Small package size: VQFN-26P (3.0 mm × 3.8 mm × 0.8 mm Typ.)
- ◆ Lead-free and RoHS compliant

Structure

- ◆ GaAs junction-gate pHEMT (JPHEMT) MMIC switch, CMOS decoder and Dual-LPF

Note on Handling

GaAs MMIC's are ESD sensitive devices. Special handling precautions are required.

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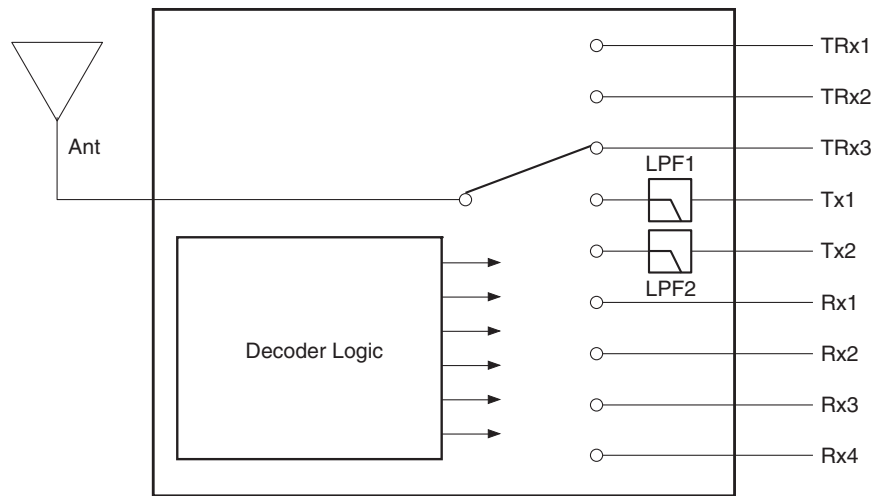


Absolute Maximum Ratings

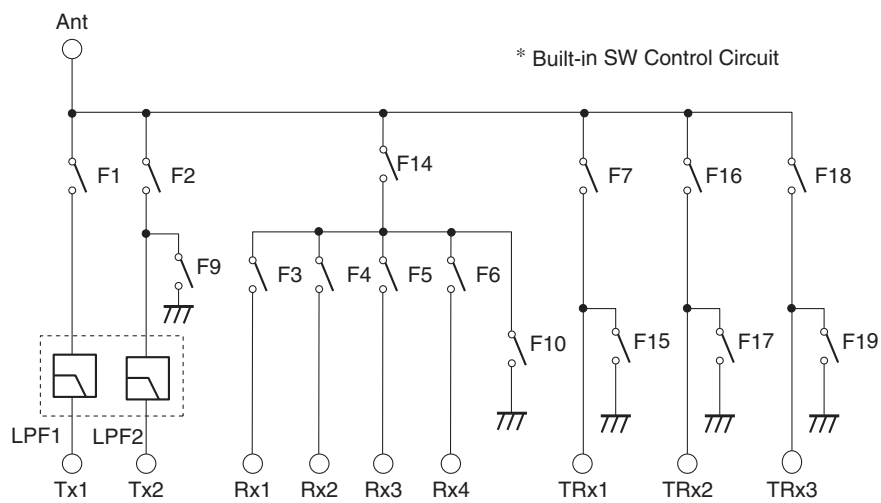
(Ta = 25 °C)

Bias voltage	V _{DD}	4	V
Control voltage (CTL-A/B/C/D)	V _{ctl}	4	V
Input power max. (Tx1)		36	dBm (Duty cycle = 12.5 %)
Input power max. (Tx2)		34	dBm (Duty cycle = 12.5 %)
Input power max. (TRx1)		32	dBm
Input power max. (Rx1, Rx2, Rx3, Rx4)		13	dBm
Operating temperature range		-35 to +90	°C
Storage temperature range		-65 to +150	°C

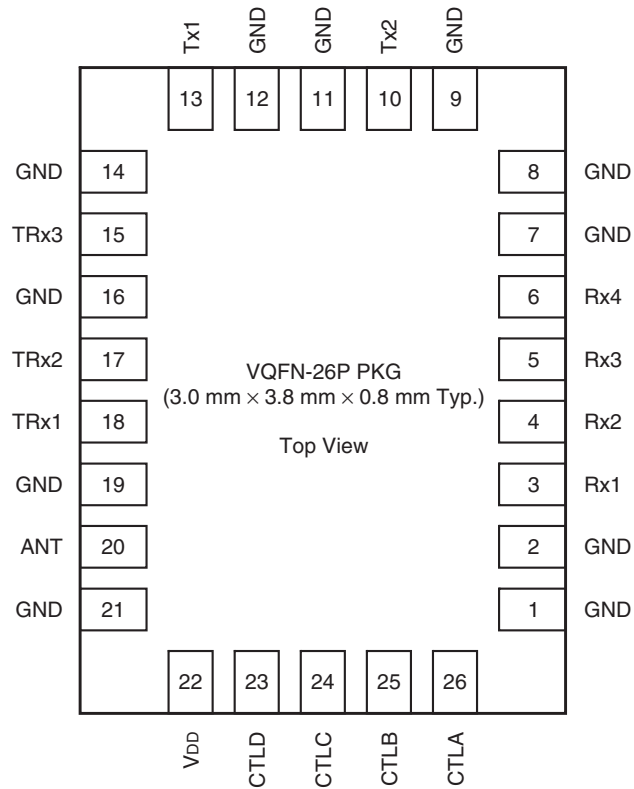
Block Diagram



RF Switch



Pin Configuration



Pin No.	Name	Pin No.	Name
1	GND	14	GND
2	GND	15	TRx3
3	Rx1	16	GND
4	Rx2	17	TRx2
5	Rx3	18	TRx1
6	Rx4	19	GND
7	GND	20	ANT
8	GND	21	GND
9	GND	22	V _{DD}
10	TX2 (DCS/PCS)	23	CTLD
11	GND	24	CTLC
12	GND	25	CTLB
13	TX1 (GSM850/900M)	26	CTLA

Truth Table

State	Active path	CTL state				Switch state														
		A	B	C	D	F1	F2	F3	F4	F5	F6	F7	F9	F10	F14	F15	F16	F17	F18	F19
1	Tx1	H	H	L	L	H	L	L	L	L	L	L	H	H	L	H	L	H	L	H
2	Tx2	H	L	L	L	L	H	L	L	L	L	L	L	H	L	H	L	H	L	H
3	Rx1* ¹	L	L	L	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	H
4	Rx2* ¹	L	L	H	L	L	L	L	H	L	L	L	H	L	H	H	L	H	L	H
5	Rx3* ¹	L	H	H	L	L	L	L	L	H	L	L	H	L	H	H	L	H	L	H
6	Rx4* ¹	L	H	L	L	L	L	L	L	L	H	L	H	L	H	H	L	H	L	H
7	TRx1* ²	H	L	H	L	L	L	L	L	L	L	H	H	H	L	L	L	H	L	H
8	TRx2* ²	H	H	H	L	L	L	L	L	L	L	L	H	H	L	H	H	L	L	H
9	TRx3* ²	—	—	—	H	L	L	L	L	L	L	L	H	H	L	H	L	H	H	L

*1 Each Rx path can be used from 869 MHz to 1990 MHz frequency. User can select these RX paths changeably.

*2 Each TRx path can be used from 824 MHz to 2170 MHz frequency. User can select these TRX paths changeably.

Supply Voltage Value

(Ta = 25 °C)

Item	Min.	Typ.	Max.	Unit
Bias voltage (V _{DD})	+2.5	+2.65	+3.3	V

Logic Value

(Ta = 25 °C)

Item	State	Min.	Typ.	Max.	Unit
Control voltage (CTL-A/B/C/D)	High	+1.5	+1.8	+3.3	V
	Low	0	—	+0.3	

Electrical Characteristics

(V_{DD} = +2.65 V, V_{ctl} = +1.8 V, T_a = +25 °C)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion loss	I.L.	Ant - Tx1	*1	—	0.90	1.05	dB
		Ant - Tx2	*2	—	0.75	0.95	
		Ant - Rx1, Rx2, Rx3, Rx4	*3	—	0.75	0.85	
			*4	—	1.00	1.15	
		Ant - TRx1	*5	—	0.65	0.80	
			*6	—	0.60	0.75	
			*7	—	0.50	0.60	
		Ant - TRx2	*5	—	0.60	0.75	
			*6	—	0.55	0.70	
			*7	—	0.50	0.60	
		Ant - TRx3	*5	—	0.60	0.75	
			*6	—	0.55	0.70	
			*7	—	0.50	0.60	

(V_{DD} = +2.65 V, V_{ctl} = +1.8 V, T_a = +25°C)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit	
Isolation	ISO	State 1						dB
		Tx1 - Rx1, RX2, Rx3, Rx4	824 to 915 MHz*1	45	55	—		
		Tx1 - TRx1		30	40	—		
		Tx1 - TRx2		45	50	—		
		Tx1 - TRx3		35	45	—		
		Tx1 - Tx2		18	22	—		
		Tx1 - Tx2		1648 to 1830 MHz*1	18	22	—	
		Tx2 - Ant	30		35	—		
		State 2						
		Tx2 - Rx1, RX2, Rx3, Rx4	1710 to 1910 MHz*2	40	50	—		
		Tx2 - TRx1, TRx2, TRx3		30	40	—		
		Tx2 - Tx1		20	25	—		
		State 7						
		TRx1 - Rx1, RX2, Rx3, Rx4	1920 to 2170 MHz*5 1710 to 1910 MHz*6 824 to 894 MHz*7	45	60	—		
		TRx1 - TRx2		20	25	—		
		TRx1 - Tx1, Tx2		20	25	—		
		TRx1 - TRx3		30	35	—		
		TRx1 - TRx3	1930 to 1980 MHz	35	39	—		
		State 8						
		TRx2 - Rx1, RX2, Rx3, Rx4	1920 to 2170 MHz*5 1710 to 1910 MHz*6 824 to 894 MHz*7	45	60	—		
		TRx2 - TRx1, TRx3		25	27	—		
		TRx2 - Tx1, Tx2		20	25	—		
		State 9						
		TRx3 - Rx1, Rx2, Rx3, Rx4	1920 to 2170 MHz*5 1710 to 1910 MHz*6 824 to 894 MHz*7	40	55	—		
		TRx3 - TRx2		20	25	—		
		TRx3 - Tx1, Tx2		20	25	—		
		TRx3 - TRx1		30	35	—		
		TRx3 - TRx1		1930 to 1980 MHz	35	40	—	

(V_{DD} = +2.65 V, V_{ctl} = +1.8 V, T_a = +25 °C)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Harmonics	2fo	Tx1 - Ant	*1	—	-45	-36	dBm
	3fo			—	-42	-36	
	2fo	Tx2 - Ant	*2	—	-55	-36	
	3fo			—	-45	-36	
	2fo	TRx1, 2, 3 - Ant	*5	—	-50	-36	
	3fo			—	-55	-36	
	2fo		*6	—	-55	-36	
	3fo			—	-55	-36	
	2fo		*7	—	-60	-36	
	3fo			—	-60	-36	
Attenuation	ATT		Tx1 - Ant	1648 to 1830 MHz	28	—	—
		2472 to 2745 MHz		30	—	—	
		3296 to 3660 MHz		20	—	—	
		Tx2 - Ant	3420 to 3820 MHz	25	—	—	
			5130 to 5730 MHz	25	—	—	
V.S.W.R.	ATT	All ports in active paths	824 to 2170 MHz	—	1.2	—	
Switching time	T _s		90 % OFF - 90 % ON	—		5	μs
Control current	I _{ctl}			—	5	20	μA
Supply current	I _{DD}		Active mode	—	0.18	0.40	mA

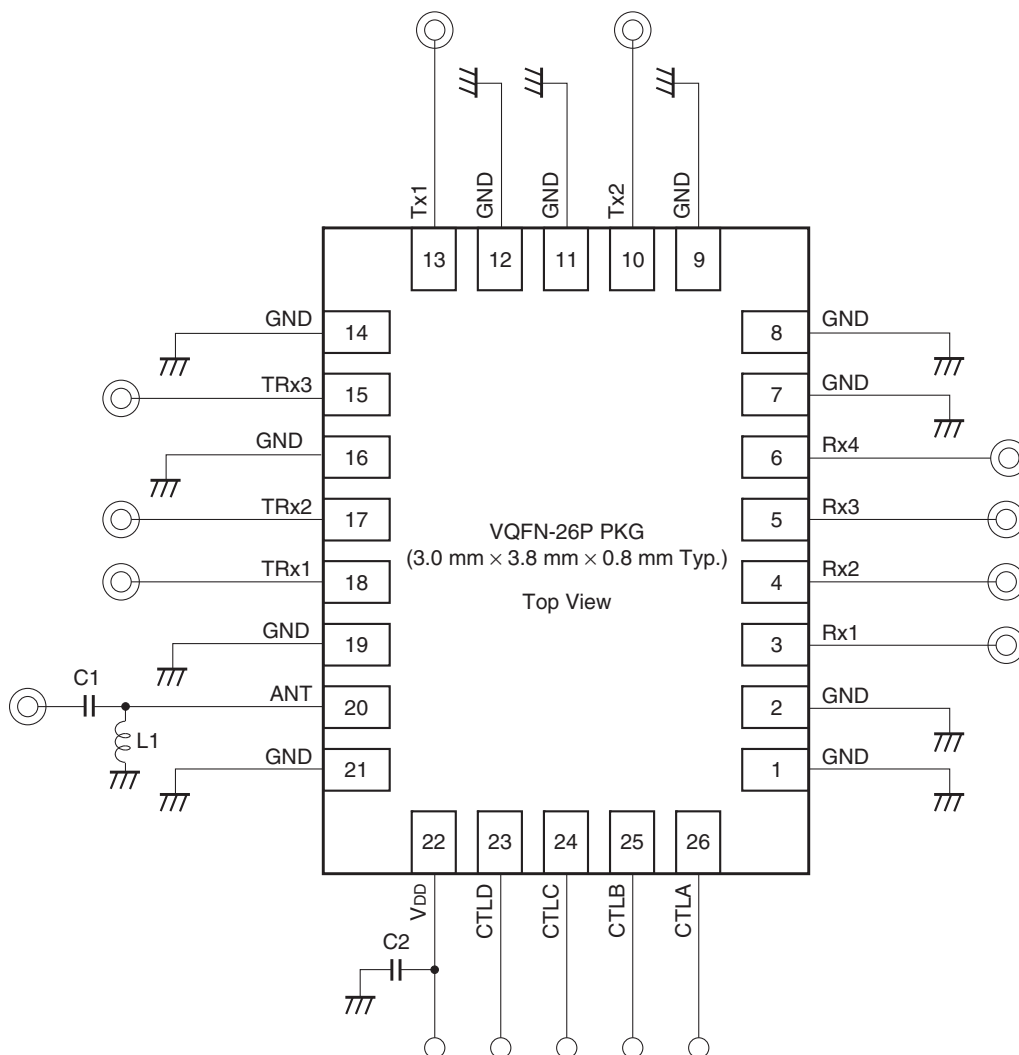
(V_{DD} = +2.65 V, V_{ctl} = +1.8 V, T_a = +25 °C)

Item	Symbol	Path	Condition			Min.	Typ.	Max.	Unit
Intermodulation distortion level in Rx band	IMD2	TRx1, 2, 3 - Ant	TRx: 835 MHz State7, 8, 9	Ant: 45 MHz	*8	—	-119	-114	dBm
				Ant: 1715 MHz	*9	—	-114	-109	
			TRx: 1880 MHz State7, 8, 9	Ant: 80 MHz	*10	—	-105	-100	
				Ant: 3840 MHz	*11	—	-102	-97	
			TRx: 1950 MHz State7, 8, 9	Ant: 190 MHz	*12	—	-103	-98	
				Ant: 4090 MHz	*13	—	-103	-98	
	IMD3	TRx1, 2, 3 - Ant	TRx: 835 MHz State7, 8, 9	Ant: 790 MHz	*14	—	-107	-102	
				Ant: 2550 MHz	*15	—	-110	-105	
			TRx: 1880 MHz State7, 8, 9	Ant: 1800 MHz	*16	—	-102	-97	
				Ant: 5720 MHz	*17	—	-108	-103	
			TRx: 1950 MHz State7, 8, 9	Ant: 1760MHz	*18	—	-102	-97	
				Ant: 6040 MHz	*19	—	-113	-108	

Electrical Characteristics are measured with all RF ports terminated in 50Ω.

- *1 Frequency = 824 to 915 MHz, Pin on Tx1: +35 dBm C.W.
- *2 Frequency = 1710 to 1910 MHz, Pin on Tx2: +32 dBm C.W.
- *3 Frequency = 869 to 960 MHz, Pin on Ant: +10 dBm C.W
- *4 Frequency = 1805 to 1990 MHz, Pin on Ant: +10 dBm C.W.
- *5 Frequency = 1920 to 2170 MHz, Pin on TRx1 or TRx2 or TRx3: +26 dBm C.W.
- *6 Frequency = 1710 to 1990 MHz, Pin on TRx1 or TRx2 or TRx3: +26 dBm C.W.
- *7 Frequency = 824 to 894 MHz, Pin on TRx1 or TRx2 or TRx3: +26 dBm C.W.
- *8 TRx port: +20 dBm, 835 MHz Ant port: -15dBm, 45 MHz
- *9 TRx port: +20 dBm, 835 MHz Ant port: -15dBm, 1715 MHz
- *10 TRx port: +20 dBm, 1880 MHz Ant port: -15dBm, 80 MHz
- *11 TRx port: +20 dBm, 1880 MHz Ant port: -15dBm, 3840 MHz
- *12 TRx port: +20 dBm, 1950 MHz Ant port: -15dBm, 190 MHz
- *13 TRx port: +20 dBm, 1950 MHz Ant port: -15dBm, 4090 MHz
- *14 TRx port: +20 dBm, 835 MHz Ant port: -15dBm, 790 MHz
- *15 TRx port: +20 dBm, 835 MHz Ant port: -15dBm, 2550 MHz
- *16 TRx port: +20 dBm, 1880 MHz Ant port: -15dBm, 1800 MHz
- *17 TRx port: +20 dBm, 1880 MHz Ant port: -15dBm, 5720 MHz
- *18 TRx port: +20 dBm, 1950 MHz Ant port: -15dBm, 1760 MHz
- *19 TRx port: +20 dBm, 1950 MHz Ant port: -15dBm, 6040 MHz
- *20 Measured with the recommended circuit.

Recommended Circuit



- Note) 1. No DC blocking capacitors are required on all RF ports.
 2. DC levels of all RF ports are GND.
 3. L1 inductor (22 nH) and C1 capacitor (22 pF) are recommended on Ant port for ESD protection.
 4. C2 capacitor (100 pF) is recommended.

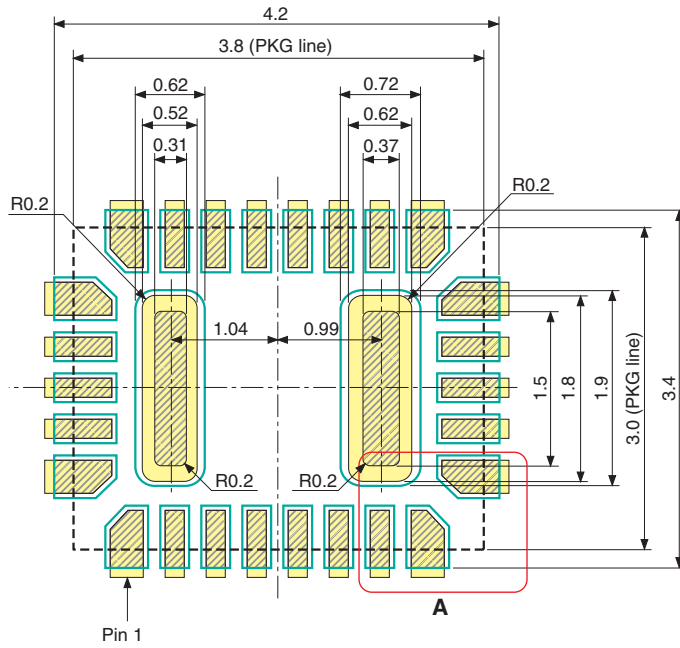
Foot Pattern

VQFN-26P-01 Macro (Reference)

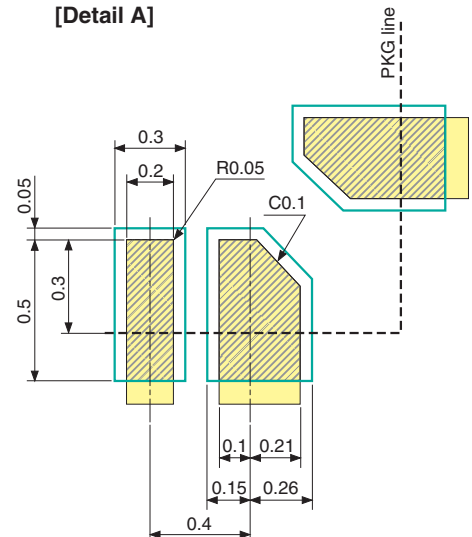
- PKG size: 3.8 mm × 3.0 mm
- Pin pitch: 0.4 mm

- : Land
- ▨ : Mask (Open area)
- : Resist (Open area)

* Metal mask thickness: 110 μm



[Detail A]



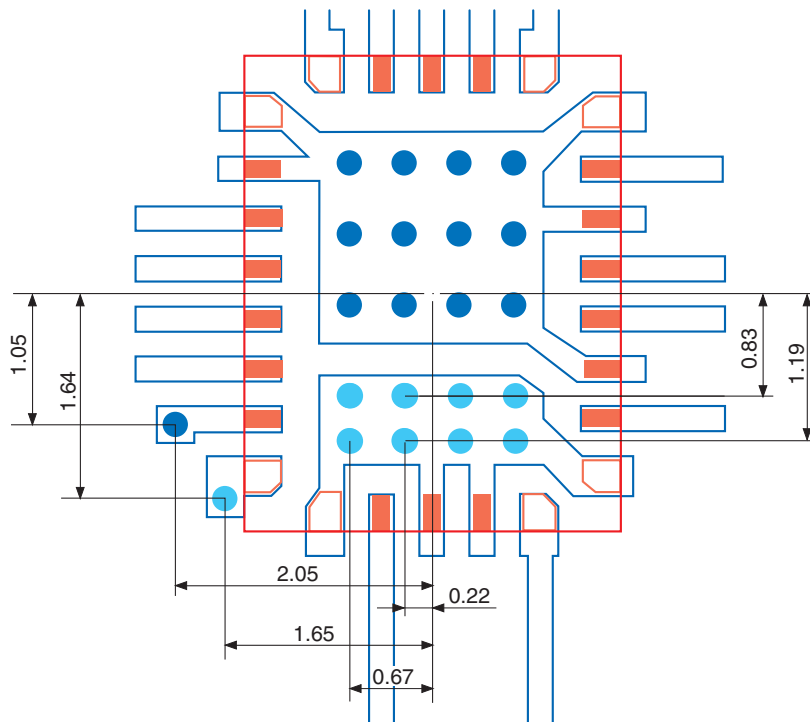
* Mask corner R = 0.05 mm

(Unit: mm)

Recommended PCB Design

The positions of the light blue via holes and relative GND patterns are strongly recommended for getting stable attenuation.

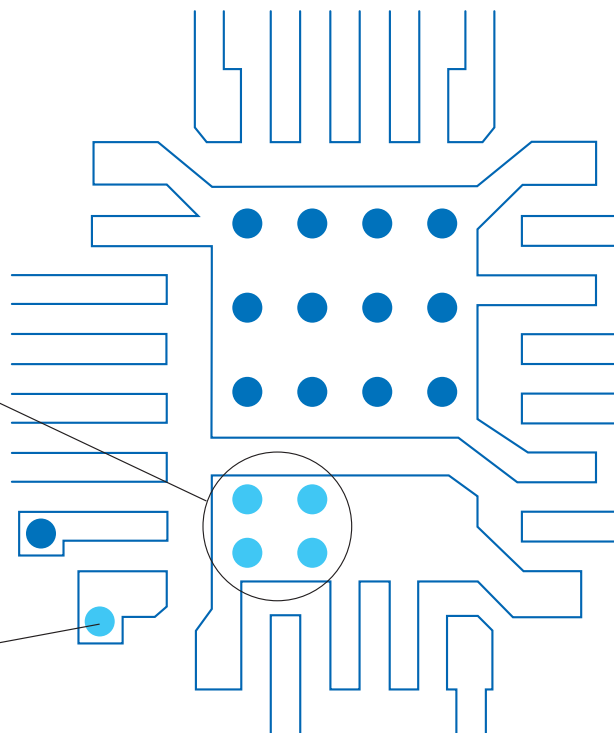
(Unit: mm)



- IC (VQFN-26P package)
- PCB metal pattern
- GND via hole for LPF (Light blue)
- GND via hole for switch

The positions of these via holes are recommended for stable attenuation.

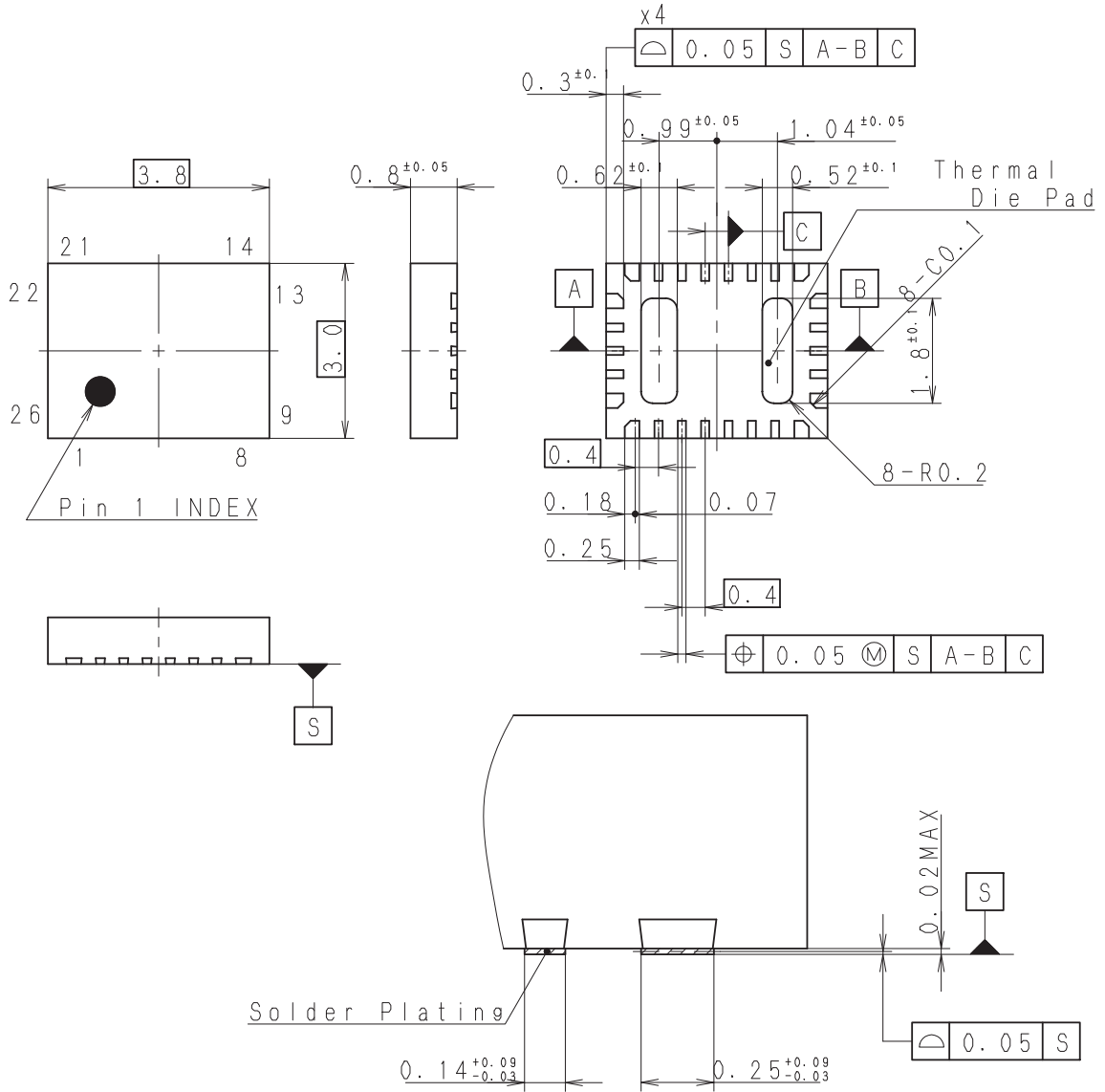
Independent GND with via hole.



Package Outline

(Unit: mm)

26PIN VQFN (PLASTIC)



Note:Cutting burr of lead are 0.05mm MAX.

TERMINAL SECTION
PACKAGE STRUCTURE

SONY CODE	VQFN-26P-01
JEITA CODE	_____
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	SOLDER PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.03g

PART No.	AP-4000-26008S	Rev. 0
ISSUED	' 07. 03. 08	REVISED
PRODUCTION LINE	_____	COMPILING DIV. SONY SEMICONDUCTOR KYUSHU.
REMARKS	PKG CODE:ER-026-AB	