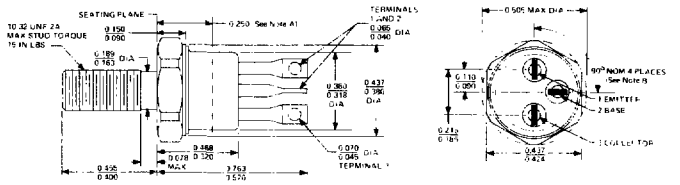
TYPES 2N5003, 2N5005, 2N5151, 2N5153
P-N-P SILICON POWER TRANSISTORS

HIGH-FREQUENCY POWER TRANSISTORS WITH COMPUTER-DESIGNED ISOTHERMAL GEOMETRY

- For Complementary Use With 2N5002, 2N5004, 2N5152, 2N5154
- 15 mJ Reverse Energy Rating with I_C = 10 A and 4 V Reverse Bias

***mechanical data**

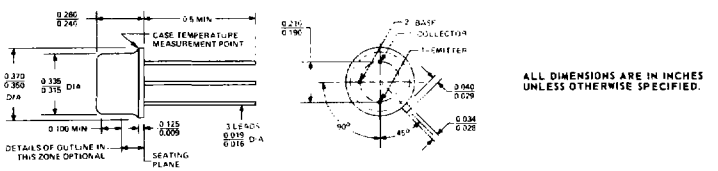
2N5003, 2N5005 — **ALL TERMINALS ARE INSULATED FROM THE CASE**



ALL JEDEC TO-59 DIMENSIONS AND NOTES ARE APPLICABLE

NOTES: A. Within this dimension, case diameter may vary.
B. Position of terminals with respect to the hexagon is not controlled.
C. The case temperature may be measured anywhere on the seating plane within 0.125 inch of the stud.
D. All dimensions are in inches unless otherwise specified.

2N5151, 2N5153 — **THE COLLECTOR IS IN ELECTRICAL CONTACT WITH THE CASE**



ALL JEDEC TO-39 DIMENSIONS AND NOTES ARE APPLICABLE

absolute maximum ratings at 25°C case temperature (unless otherwise noted)

	2N5003 2N5005	2N5151 2N5153
Collector-Base Voltage	←——— −100 V* ———	
Collector-Emitter Voltage (See Note 1)	←——— −80 V* ———	
Emitter-Base Voltage	←——— −5.5 V* ———	
Continuous Collector Current	−5 A*	−5 A*
Peak Collector Current (See Note 2)	−10 A*	−10 A
Continuous Base Current	−2 A*	−2.5 A*
Safe Operating Areas	See Figures 7* and 8	
Continuous Device Dissipation at 50°C Case Temperature (See Note 3)	50 W*	10 W*
Continuous Device Dissipation at 100°C Case Temperature (See Note 3)	33.3 W	6.7 W
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 4)	1 W*	
Unclamped Inductive Load Energy (See Note 5)	←——— 15 mJ ———	
Operating Collector Junction Temperature Range	−65°C to 200°C*	
Storage Temperature Range	−65°C to 200°C*	
Lead or Terminal Temperature 1/8 Inch from Case for 60 Seconds	←——— 300°C* ———	

NOTES: 1. This value applies when the base-emitter diode is open-circuited.
2. This value applies for $t_W \leq 8.3$ ms, duty cycle ≤ 1%.
3. For operation above (or below) 50°C case temperature, refer to Dissipation Derating Curves, Figures 9 and 10.
4. Derate linearly to 200°C free-air temperature at the rate of 5.7 mW/°C.
5. This rating is based on the capability of the transistors to operate safely in the unclamped inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors*†. L = 0.3 mH, R_{BB1} = 10 Ω, R_{BB2} = 100Ω, V_{BB1} = 10 V, V_{BB2} = 4 V, R_L = 0.1 Ω, V_{CC} = 10 V, I_{CM} = 10 A. Energy ≈ $I_C^2 L/2$.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

†This circuit appears on page 5-1 of this data book.

TYPES 2N5003, 2N5005, 2N5151, 2N5153
P-N-P SILICON POWER TRANSISTORS

*electrical characteristics at 25°C case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		2N5003 2N5151 MIN	2N5003 2N5151 MAX	2N5005 2N5153 MIN	2N5005 2N5153 MAX	UNIT
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = −100 mA, I_B = 0,	See Note 6	−80		−80		V
I_{CEO}	Collector Cutoff Current	V_{CE} = −40 V, I_B = 0			−50		−50	μA
I_{CES}	Collector Cutoff Current	V_{CE} = −60 V, V_{BE} = 0			−1		−1	μA
		V_{CE} = −100 V, V_{BE} = 0			−1		−1	mA
I_{CEV}	Collector Cutoff Current	V_{CE} = −60 V, V_{BE} = 2 V, T_C = 150°C			−500		−500	μA
I_{EBO}	Emitter Cutoff Current	V_{EB} = −4 V, I_C = 0			−1		−1	μA
		V_{EB} = −5.5 V, I_C = 0			−1		−1	mA
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = −5 V, I_C = −50 mA	See Notes 6 and 7	20		50		
		V_{CE} = −5 V, I_C = −2.5 A		30	90	70	200	
		V_{CE} = −5 V, I_C = −5 A		20		40		
		V_{CE} = −5 V, I_C = −2.5 A, T_C = −55°C		15		35		
V_{BE}	Base-Emitter Voltage	I_B = −250 mA, I_C = −2.5 A	See Notes 6 and 7		−1.45		−1.45	V
		I_B = −500 mA, I_C = −5 A			−2.2		−2.2	
		V_{CE} = −5 V, I_C = −2.5 A			−1.45		−1.45	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = −250 mA, I_C = −2.5 A	See Notes 6 and 7		−0.75		−0.75	V
		I_B = −500 mA, I_C = −5 A			−1.5		−1.5	
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio	V_{CE} = −5 V, I_C = −0.1 A, f = 1 kHz		20		50		
$\|h_{fe}\|$	Small-Signal Common-Emitter Forward Current Transfer Ratio	V_{CE} = −5 V, I_C = −0.5 A, f = 20 MHz		3		3.5		
C_{obo}	Common-Base Open-Circuit Output Capacitance	V_{CB} = −10 V, I_E = 0, f = 1 MHz			250		250	pF

NOTES: 6. These parameters must be measured using pulse techniques, t_w = 300 μs, duty cycle ≤ 1%.

7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

*JEDEC registered data

thermal characteristics

PARAMETER		2N5003 2N5005 MAX	2N5151 2N5153 MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	3	15	°C/W

switching characteristics at 25°C case temperature

PARAMETER		TEST CONDITIONS†			ALL TYPES TYP	UNIT
t_{on}	Turn-On Time	I_C = −5 A,	$I_{B(1)}$ = −500 mA,	$I_{B(2)}$ = 500 mA,	0.5	μs
t_{off}	Turn-Off Time	$V_{BE(off)}$ = 3.7 V,	R_L = 6 Ω,	See Figure 1	1.3	

† Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

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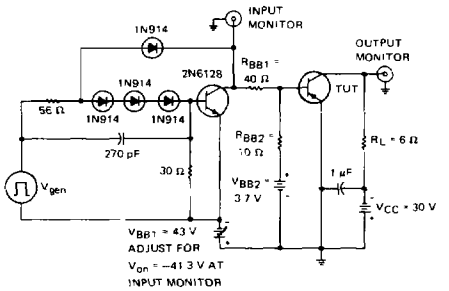
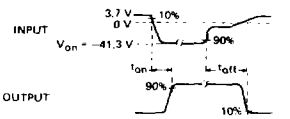
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. V_{gen} is a 30-V pulse (from 0 V) into a 50-Ω termination.
B. The V_{gen} waveform is supplied by a generator with the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, $Z_{out} = 50\ \Omega$, $t_w = 20\ \mu s$, duty cycle ≤ 2%.
C. Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 15$ ns, $R_{in} \geq 10\ M\Omega$, $C_{in} \leq 11.5$ pF.
D. Resistors must be noninductive types.
E. The d-c power supplies may require additional bypassing in order to minimize ringing.

FIGURE 1

TYPICAL CHARACTERISTICS

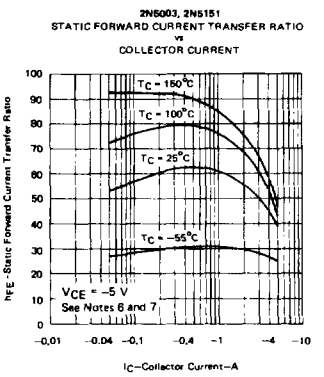


FIGURE 2

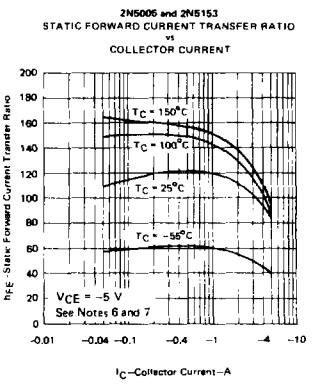


FIGURE 3

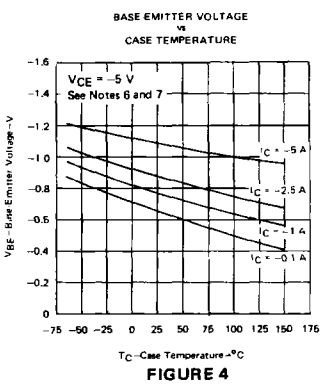


FIGURE 4

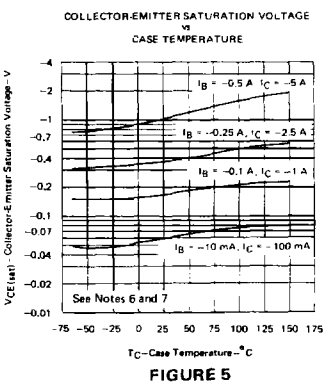


FIGURE 5

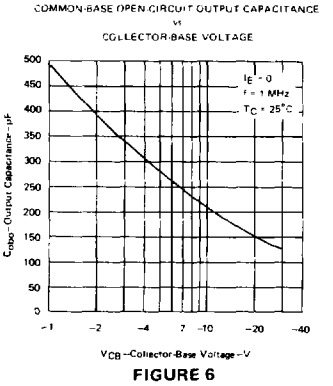


FIGURE 6

NOTES: 6. These parameters must be measured using pulse techniques. $t_w = 300\ \mu s$, duty cycle ≤ 1%.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts and located within 0.125 inch from the device body.

MAXIMUM SAFE OPERATING AREAS

MAXIMUM COLLECTOR CURRENT
vs
COLLECTOR-EMITTER VOLTAGE

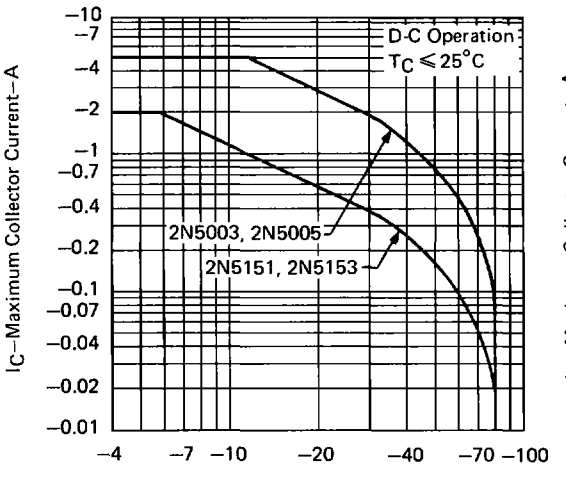


FIGURE 7

MAXIMUM COLLECTOR CURRENT
vs
UNCLAMPED INDUCTIVE LOAD

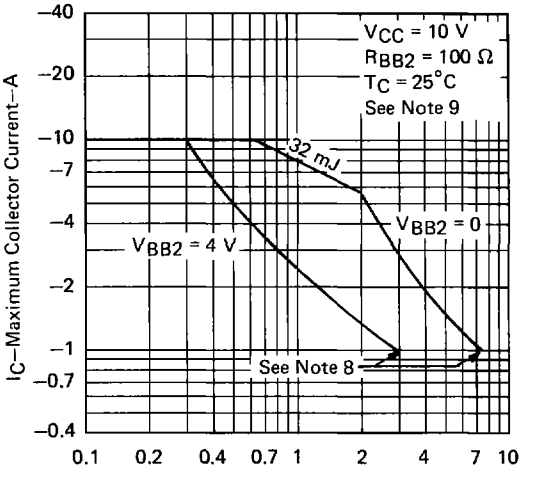


FIGURE 8

NOTES: 8. Above these points the safe operating areas have not been defined.

9. These curves are based on the capability of the transistors to operate safely in the unclamped inductive load circuit of Section 3.2 of the forthcoming JEDEC publication *Suggested Standards on Power Transistors.*† $R_{BB1} = 10 \cdot V_{BB1}/I_C$, V_{BB1} = 10 V, R_L = 0.1 Ω. Energy ≈ $I_C^2 L/2$.

†This circuit appears on page 5-1 of this data book.

THERMAL INFORMATION

2N5003, 2N5005
DISSIPATION DERATING CURVE

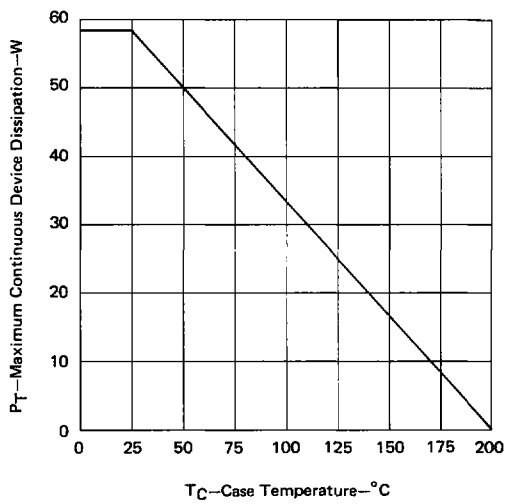


FIGURE 9

2N5151, 2N5153
DISSIPATION DERATING CURVE

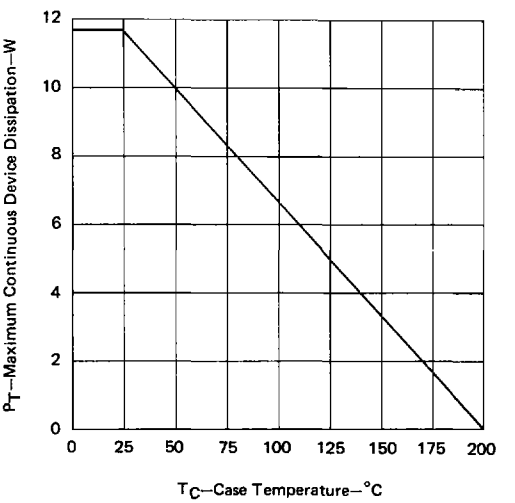


FIGURE 10

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