T8502 and T8503 Dual PCM Codecs with Filters

Features

- 5 V only
- Two independent channels
- Pin-selectable receive gain control
- Pin-selectable µ-law or A-law companding
- Automatic powerdown mode
- Low-power, latch-up-free CMOS technology
  — 40 mW/channel typical operating power dissipation
  — 12.5 mW/channel typical standby power dissipation
- Automatic master clock frequency selection
  — 2.048 MHz or 4.096 MHz
- Independent transmit and receive frame strobes
- 2.048 MHz or 4.096 MHz data rate
- On-chip sample and hold, autozero, and precision voltage reference
- Differential architecture for high noise immunity and power supply rejection
- Meets or exceeds ITU-T G.711—G.712 requirements and VF characteristics of D3/D4 (as per Agere Systems Inc.'s PUB43801)
- Operating temperature range: –40 °C to +85 °C

Description

The T8502 and T8503 devices are single-chip, two-channel, µ-law/A-law PCM codecs with filters. These integrated circuits provide analog-to-digital and digital-to-analog conversion. They provide the transmit and receive filtering necessary to interface a voice telephone circuit to a time-division multiplexed system. These devices are packaged in both 20-pin SOJs and 20-pin SOGs.

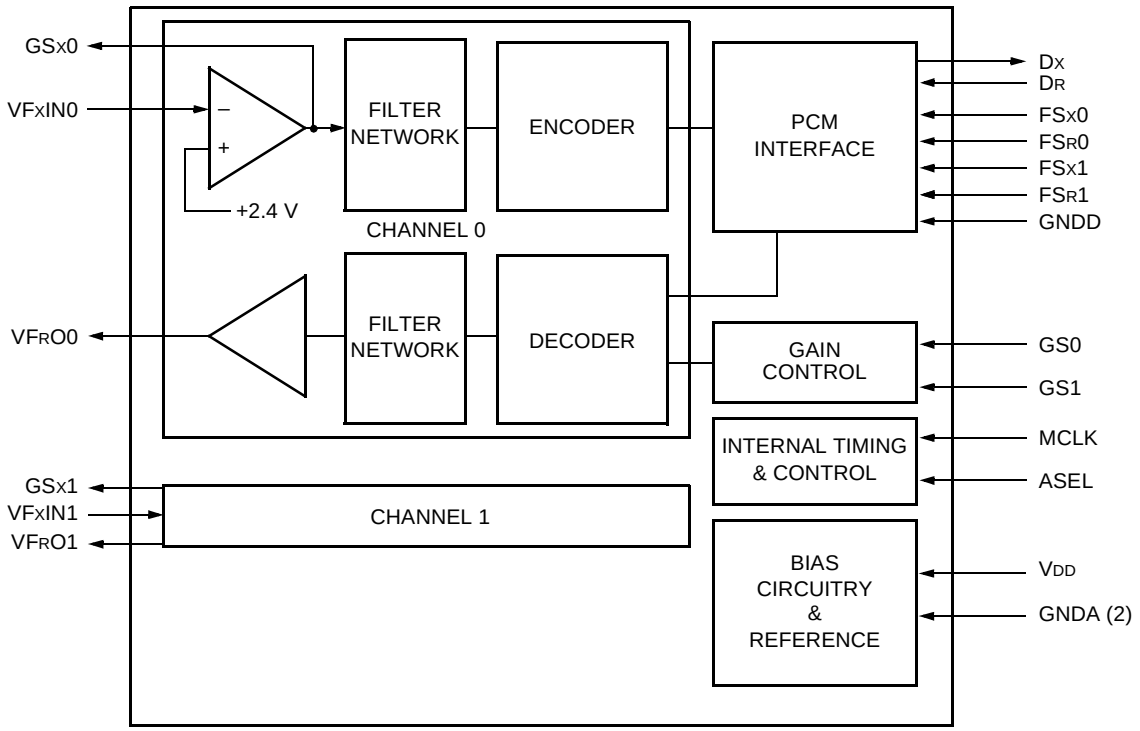
The T8502 differs from the T8503 in its timing mode. The T8502 operates in the delayed timing mode (digital data is valid one clock cycle after frame sync goes high), and the T8503 operates in the nondelayed timing mode (digital data valid when frame sync goes high).

Two channels of PCM data input and output are passed through only two ports, D_X and D_R, so some type of time-slot assignment is necessary. The scheme used here is to utilize a fixed-data rate mode of 32 or 64 time slots corresponding to master clock frequencies of either 2.048 MHz or 4.096 MHz, respectively. Each device has four frame sync (FS_X and FS_R) inputs, one pair for each channel. During a single 125 µs frame, each frame sync input is supplied a single pulse. The timing of the respective frame sync pulse indicates the beginning of the time slot during which the data for that channel is clocked in or out of the device. FS_X and FS_R must be high for a minimum of one master clock cycle. They can be operated independently, or they can be tied together for coincident transmit and receive data transfer. During a frame, channel 0 and 1 transmit frame sync pulses must be separated from each other by one or more time slots. Likewise, channel 0 and 1 receive frame sync pulses must be separated from each other by one or more time slots. Both transmit and receive frame strobes must be derived from master clock, but they do not need to be byte aligned.

A channel is placed in standby mode by removing both FS_X and FS_R for 500 µs. Note, if any one of those pulses (per channel) is removed, operation is indeterminate. Standby mode reduces overall device power consumption by turning off nonessential circuitry. Critical circuits that ensure a fast, quiet powerup are kept active. Master clock need not be active when both channels are in standby mode.

The frequency of the master clock must be either 2.048 MHz or 4.096 MHz. Internal circuitry determines the master clock frequency during the powerup reset interval.

Block Diagram



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February 2002
PB02-067ALC (Replaces PB00-050ALC)