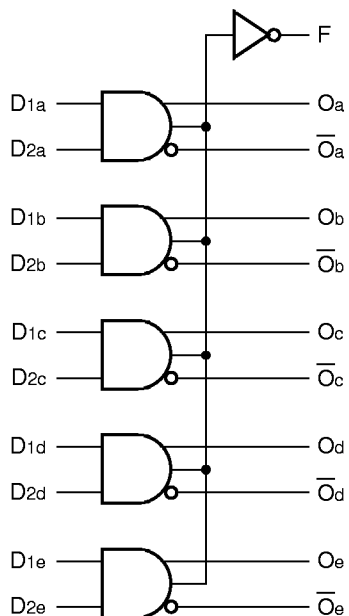


FEATURES

- Max. propagation delay of 1050ps
- IEE min. of -60mA
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 40% faster than National 300K at lower power
- Function and pinout compatible with National and Signetics F100K
- ESD protection of 2000V
- Available in 24-pin CERPDP, 24-pin CERPDP and 28-pin PLCC packages

BLOCK DIAGRAM



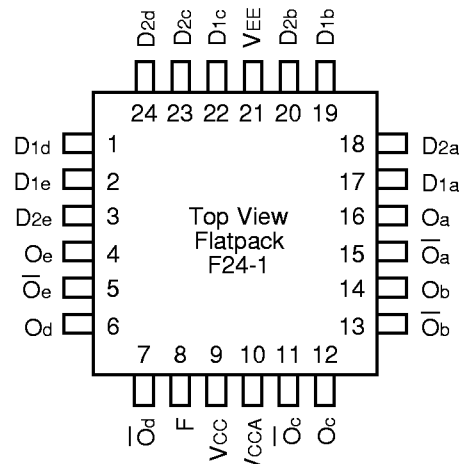
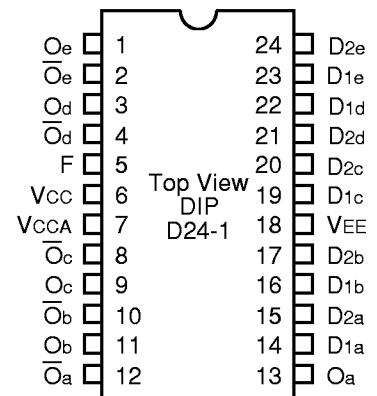
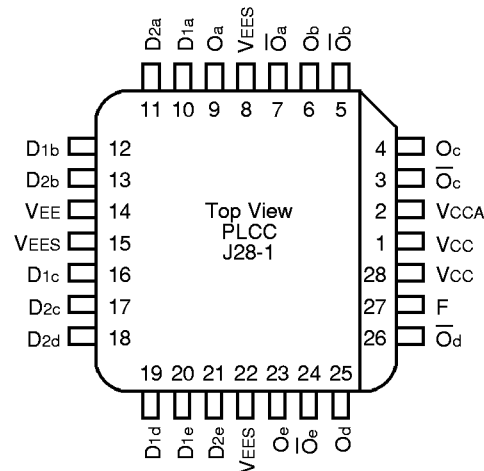
PIN NAMES

Pin	Function
Dna - Dne	Data Inputs (n-1...5)
E	Enable Input
Oa - Oe	Data Outputs
$\overline{Oa} - \overline{Oe}$	Complementary Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

DESCRIPTION

The SY100S304 is an ultra-fast quint AND/NAND gate designed for use in high-performance ECL systems. This device also features a Function (F) output which is the wire-NOR of the AND gate outputs. The inputs on the device have 75KΩ pull-down resistors.

PIN CONFIGURATIONS



DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current				μA	$V_{IN} = V_{IH} (Max.)$
	D2a — D2e	—	—	250		
	D1a — D1e	—	—	250		
I_{EE}	Power Supply Current	-60	-40	-30	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERDIP

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Dna — Dne to O, $\bar{O}$	300	1250	300	1250	300	1250	ps	
t_{PLH} t_{PHL}	Propagation Delay Data to F	600	1750	600	1750	600	1750	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

CERPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

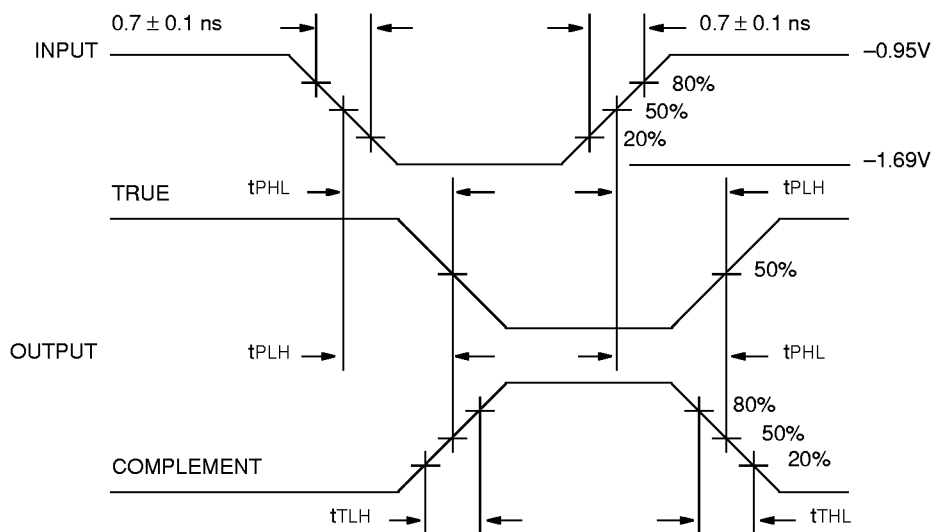
Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Dna — Dne to O, $\bar{O}$	300	1150	300	1150	300	1150	ps	
t_{PLH} t_{PHL}	Propagation Delay Data to F	600	1650	600	1650	600	1650	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0^{\circ}C$		$T_A = +25^{\circ}C$		$T_A = +85^{\circ}C$		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Dna — Dne to O, $\bar{O}$	300	1050	300	1050	300	1050	ps	
t_{PLH} t_{PHL}	Propagation Delay Data to F	600	1550	600	1550	600	1550	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM



Propagation Delay and Transition Times

NOTE:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$

PRODUCT ORDERING CODE

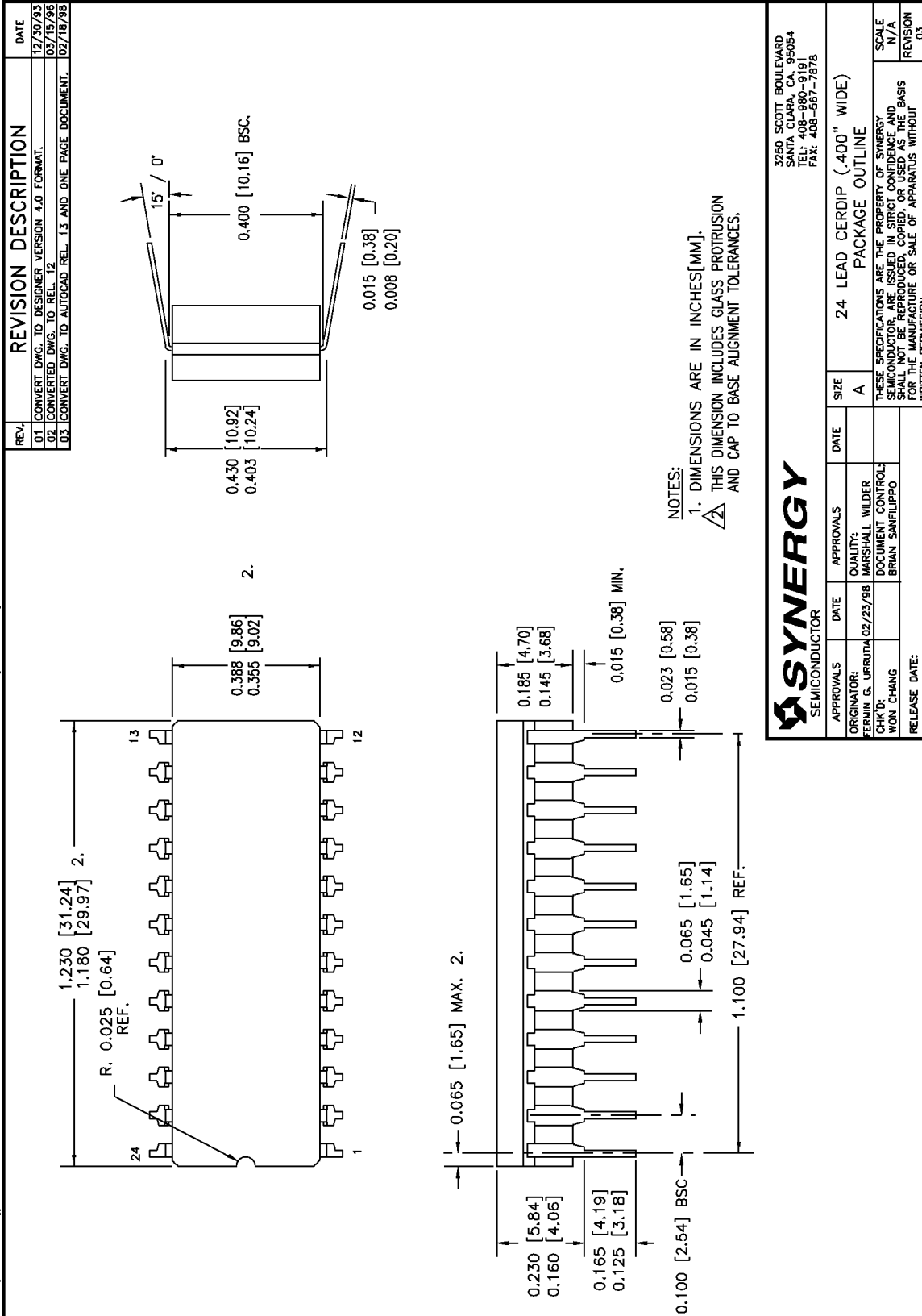
Ordering Code	Package Type	Operating Range
SY100S304DC	D24-1	Commercial
SY100S304FC	F24-1	Commercial
SY100S304JC	J28-1	Commercial
SY100S304JCTR	J28-1	Commercial

24 LEAD CERPDP (D24-1)

FILE/REV #: PD0003A03

PD/0003/ASCORP

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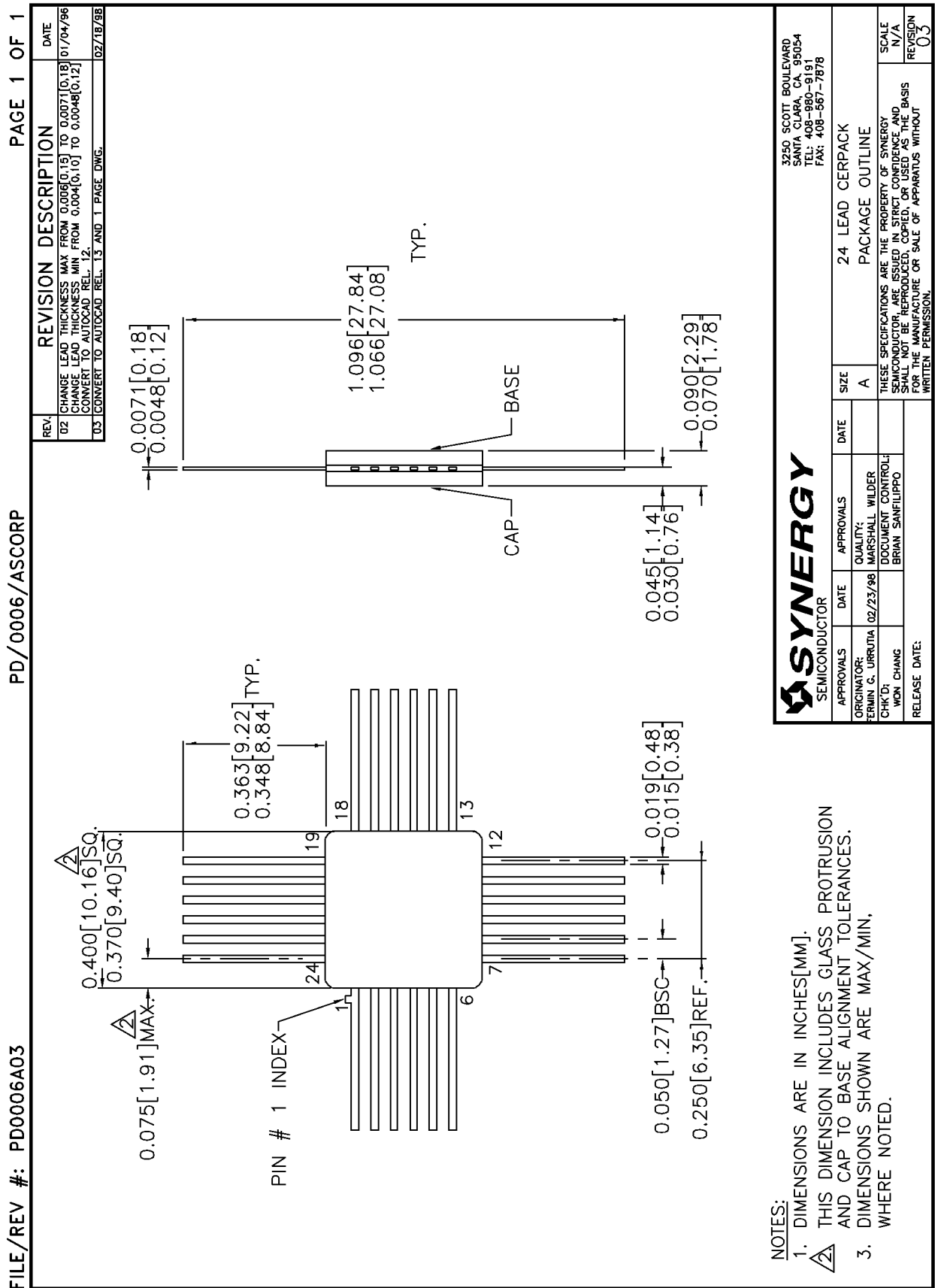
SYNERGY
SEMICONDUCTOR

3250 SCOTT BOULEVARD
SANTA CLAY, CA 95054
TEL: 408-980-9191
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	24 LEAD CERPDP (.400" WIDE) PACKAGE OUTLINE	SCALE
ORIGINATOR: FERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A		N/A
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO				
RELEASE DATE:						REVISION 03

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24 LEAD CERPACK (F24-1)



NOTES:

- DIMENSIONS ARE IN INCHES[MM].
- THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
- DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

SYNERGY
SEMICONDUCTOR

3250 SCOTT BOULEVARD
SANTA CLARA, CA 95054
TEL: 408-980-8191
FAX: 408-567-7878

24 LEAD CERPACK
PACKAGE OUTLINE

QUALITY: MARSHALL WILDER
DOCUMENT CONTROL:
BRIAN SANFILIPPO

RELEASE DATE:

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SCALE: N/A
REVISION: 03

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

FILE/REV #: PD0008A03

PD/0008/ASCORP

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