Military 10H751

Advance Information

Quad TTL/NMOS to MECL Translator

ELECTRICALLY TESTED PER:
MPG 10H751

The 10H751 is a quad translator for interfacing data between a saturated logic section and the MECL section of digital systems when only a + 5.0 Vdc power supply is available. The 10H751 has TTL/NMOS complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input at a low logic level, it forces all true outputs to the MECL low logic state (≈ +3.2 V) and all inverting outputs to the MECL high state (≈ + 4.1 V).

The 10H751 can also used with the 10H750 to transmit and receive TTL/NMOS information differentially via balanced twisted pair lines.

- Single + 5.0 V Power Supply
- All V_{CC} Pins Isolated On Chip
- Differentially Drive Balanced Lines
- t_{pd} = 1.3 ns typical

PIN ASSIGNMENTS

FUNCTION	DIL	BURN-IN (CONDITION C)
B_{OUT}	1	GND
$\overline{B_{OUT}}$	2	GND
NC	3	V_{CC}
A_{OUT}	4	GND
$\overline{A_{OUT}}$	5	GND
V_{CC}	6	V_{CC}
B_{IN}	7	GND
A_{IN}	8	GND
Common Strobe	9	GND
GND	10	GND
TTL V_{CC}	11	V_{CC}
D_{IN}	12	GND
NC	13	GND
C_{IN}	14	V_{CC}
V_{CC}^2	15	V_{CC}
$\overline{D_{OUT}}$	16	GND
D_{OUT}	17	GND
$\overline{C_{OUT}}$	18	GND
C_{OUT}	19	GND
TTL V_{CC}	20	V_{CC}

BURN - IN CONDITIONS:
V_{TT} = -2.0 V MAX/ -2.2 V MIN
V_{EE} = -5.7 V MAX/ -5.2 V MIN

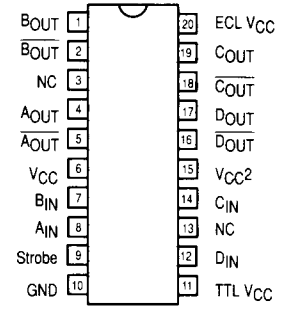
This document contains information on a new product. Specifications and information herein are subject to change without notice.

AVAILABLE AS

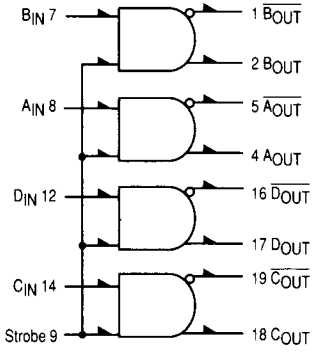
1) JAN: N/A
2) SMD: N/A
3) 883: 10H751/BXAJC
X = CASE OUTLINE AS FOLLOWS:

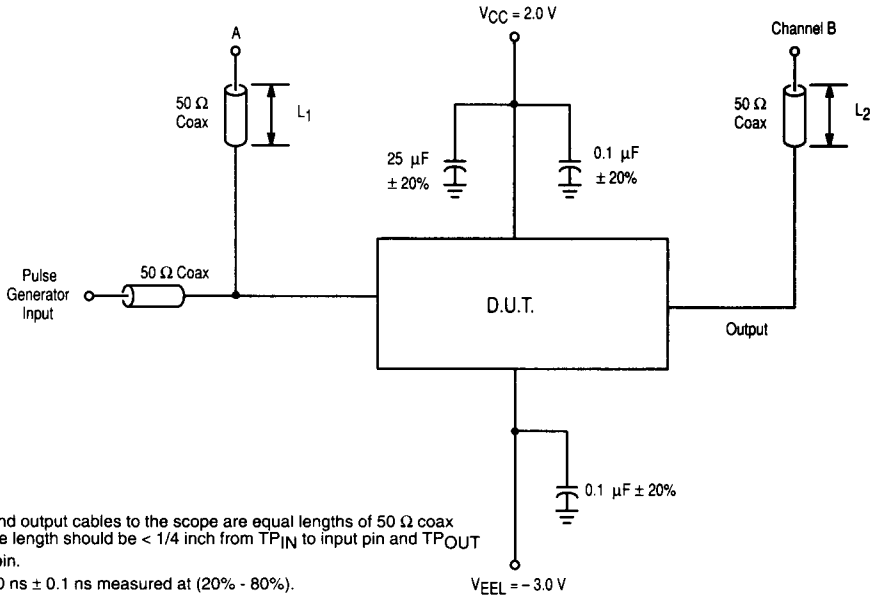
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coax cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.
2. $t_r = t_f = 2.0$ ns ± 0.1 ns measured at (20% - 80%).
3. $P_W \geq 20$ ns.
4. $P_{RF} = 1.0$ MHz.
5. All unused outputs should be loaded 100 Ω to ground.
6. 2:1 divider may be used.
7. $L_1 = L_2$: Matched for equal time delay.

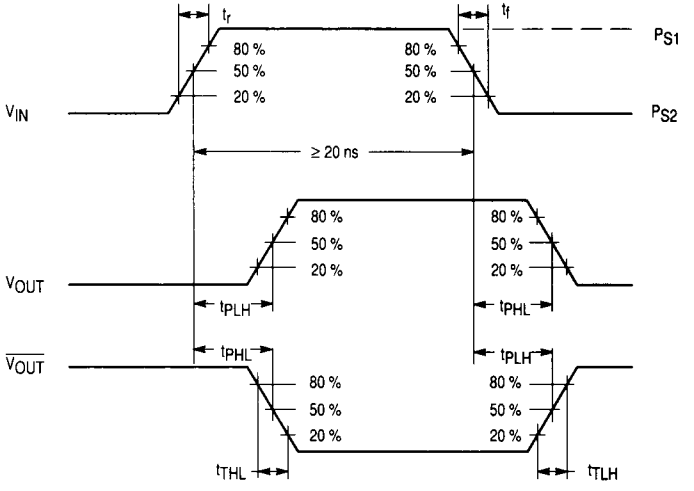


Figure 1. Switching Test Circuit and Waveforms

10H751
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to –2.0 volts.

Test Temperature	Test Voltage Values (Volts)						
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{CC}	V_{CCL}	V_{CCH}
T_A = 25 °C	+2.7	+0.4	+2.0	+0.8	+5.0	+4.75	+5.25
T_A = 125 °C	+2.7	+0.4	+2.0	+0.8	+5.0	+4.75	+5.25
T_A = - 55 °C	+2.7	+0.4	+2.0	+0.8	+5.0	+4.75	+5.25

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to + 3.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	GND	V_{CC}	V_{CCL}	V_{CCH}	P. U. T.
V_{OH}	High Output Voltage	4.00	4.30	4.08	4.30	3.80	4.20	V	7 - 9, 12, 14			10	6, 11, 15, 20			1, 2, 4, 5, 16 - 19
V_{OL}	Low Output Voltage	3.00	3.40	3.05	3.40	3.05	3.37	V		7 - 9, 12, 14		10	6, 11, 15, 20			1, 2, 4, 5, 16 - 19
V_{OHH}	High Output Voltage	4.27	4.50	4.33	4.60	3.90	4.40	V				10			6, 11, 15, 20	1, 2, 4, 5, 16 - 19
V_{OLL}	Low Output Voltage	3.30	3.80	2.80	3.20	2.80	3.12	V		7 - 9, 12, 14		10		6, 11, 15, 20		1, 2, 4, 5, 16 - 19
V_{OLH}	Low Output Voltage	3.30	3.80	3.30	3.70	3.30	3.62	V				10			6, 11, 15, 20	1, 2, 4, 5, 16 - 19
V_{OHL}	High Output Voltage	3.77	4.20	3.83	4.10	3.50	3.91	V			7 - 9, 12, 14	10		6, 11, 15, 20		1, 2, 4, 5, 16 - 19
I_{CC}	Power Supply Current (ECL)		45		50		50	mA				10	6, 11, 15, 20			20
I_{CC}	Power Supply Current (TTL)		15		20		20	mA				10	6, 11, 15, 20			11
I_{INH1}	Input Current High		20		25		25	µA	7 - 9, 12, 14	7 - 9, 12, 14		10			6, 11, 15, 20	7, 8, 12, 14
I_{INH2}	Input Current High		80		100		100	µA	9	7 - 9, 12, 14		10			6, 11, 15, 20	9
I_{INL1}	Input Current Low		- 0.6		- 0.8		- 0.8	µA		7 - 9, 12, 14		10	7 - 9, 12, 14		6, 11, 15, 20	7, 8, 12, 14
I_{INL2}	Input Current Low		- 2.4		- 3.2		- 3.2	µA		9		10	7, 8, 12, 14		6, 11, 15, 20	9

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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW			
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND			
		Subgroup 9		Subgroup 10		Subgroup 11						
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	GND	P.U.T.
t_{TLH}/ t_{TLH}	Rise & Fall Time	0.6	1.7	0.9	1.8	0.5	1.7	ns	7, 8, 12, 14	1, 2, 4, 5, 16, 17, 18, 19	10	1, 2, 4, 5, 16, 17, 18, 19
t_{pd}	Propagation Delay	0.4	2.2	0.3	2.65	0.2	2.2	ns	7, 8, 12, 14	1, 2, 4, 5, 16, 17, 18, 19	10	1, 2, 4, 5, 16, 17, 18, 19