HY514404B Series

1M x 4-bit CMOS DRAM with Extended Data Out

DESCRIPTION

This family is a 4M bit dynamic RAM organized 1,048,576 x 4-bit configuration with Extended Data Out mode CMOS DRAMs. Extended Data Out mode offers high speed random access of memory cells within the same row. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(50,60 or 70ns) and package type(SOJ, TSOP-II and reverse TSOP-II) and power consumption (Normal or Low power with Self refresh). Hyundai's advanced circuit design and process technology allow this device to achieve high bandwidth, low power consumption and high reliability.

ORDERING INFORMATION

Part Number	SPEED	Power	Pkg.
HY514404BJ	50/60/70		SOJ
HY514404BLJ	50/60/70	L-part	SOJ
HY514404BSLJ	50/60/70	SL-part	SOJ
HY514404BT	50/60/70		TSOP-II
HY514404BLT	50/60/70	L-part	TSOP-II
HY514404BSLT	50/60/70	SL-part	TSOP-II
HY514404BR	50/60/70		TSOP-II(R)
HY514404BLR	50/60/70	L-part	TSOP-II(R)
HY514404BSLR	50/60/70	SL-part	TSOP-II(R)

FEATURES

- Low power dissipation
  Max. battery back-up 1.65mW (SL-part)
  Max. CMOS standby 1.1mW (SL-part)
  5.5mW
  Max. TTL standby 11.0mW
  Max. Self Refresh 1.1mW (SL-part)
  Max. operating

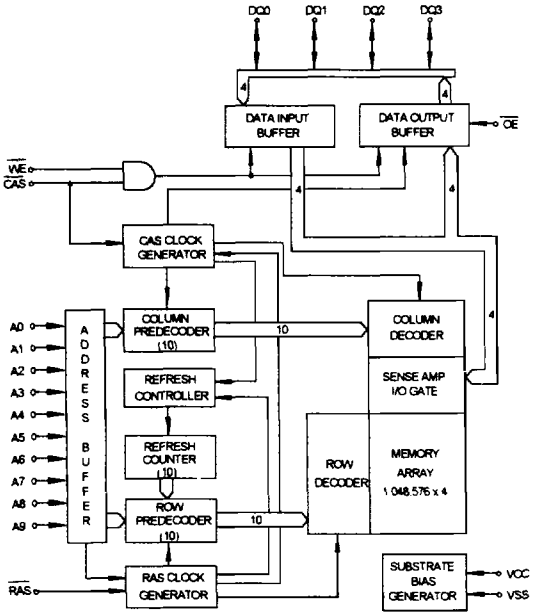
Speed	Power
50	550.0mW
60	495.0mW
70	440.0mW

- Single power supply of 5V±10%
- TTL compatible inputs and outputs
- Fast access time and cycle time

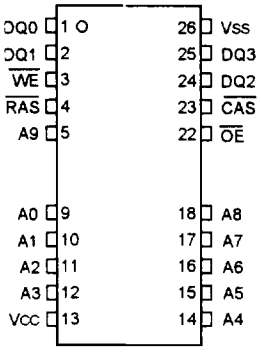
Speed	tRAC	tCAC	tHPC
50ns	50ns	13ns	20ns
60ns	60ns	15ns	25ns
70ns	70ns	18ns	30ns

- Extended Data Out Operation
- Read-Modify-Write Capability
- /CAS-before-/RAS, /RAS-only, Hidden refresh and Self Refresh
  - 1024 refresh cycles / 128ms (SL-part)
  - 1024 refresh cycles / 16ms
- JEDEC standard pinout
  20/26-pin SOJ (300mil)
  20/26-pin TSOP(300mil)

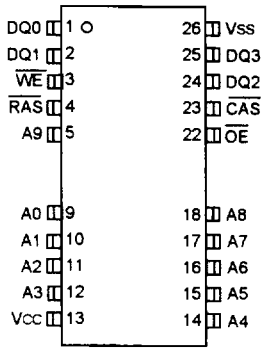
BLOCK DIAGRAM



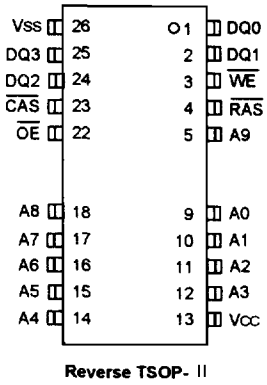
PIN CONFIGURATION (Marking Side)



20/26-pin SOJ (300mil)



20/26-pin TSOP (300mil)



20/26-pin TSOP-II (300mil)

PIN DESCRIPTION

/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0-A9	Address Input
DQ0-DQ3	Data I/O
Vcc	Power (+5V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	-55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin relative to Vss	-1.0 to 7.0	V
V_{CC}	Voltage on Vcc relative to Vss	-1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	0.90	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	℃ · sec

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0℃ to 70℃)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	Vcc+1.0	V
V_{IL}	Input Low Voltage	-1.0	-	0.8	V

Note: All voltages are referenced to Vss.

DC CHARACTERISTICS

(T_A=0℃ to 70℃, Vcc=5V ± 10%, Vss=0V, unless otherwise noted.)

Symbol	Parameter	Test Conditions	Speed/ Power	Min.	Max.	Unit	Note
I_{LI}	Input Leakage current (Any Input Pins)	Vss ≤ V_{IN} ≤ Vcc + 1.0V All other pins not under test = Vss		-10	10	uA	
I_{LO}	Output Leakage current (High Impedance State)	Vss ≤ V_{OUT} ≤ Vcc, /RAS & /CAS at V_{IH}		-10	10	uA	
I_{CC1}	Vcc Supply Current, Operating	tRC=tRC (min.)	50 60 70	- - -	100 90 80	mA	1,2,3
I_{CC2}	Vcc Supply Current, TTL Standby	/RAS & /CAS at V_{IH},(min.) other inputs ≥ Vss		-	2	mA	
I_{CC3}	Vcc Supply Current, /RAS-only Refresh	tRC=tRC (min.)	50 60 70	-	100 90 80	mA	1,3
I_{CC4}	Vcc Supply Current, EDO Page Mode	tHPC=tHPC (min.)	50 60 70	-	100 90 80	mA	1,2,3
I_{CC5}	Vcc Supply Current, CMOS Standby	/RAS & /CAS ≥ Vcc - 0.2V	SL-part	-	1 200	mA uA	5
I_{CC6}	Vcc Supply Current, /CAS-before-/RAS Refresh	tRC=tRC (min.)	50 60 70	-	100 90 80	mA	1,3
I_{CC7}	Vcc Supply Current Battery Back Up (SL-part only)	tRC= 125us, /CAS = CBR cycling or 0.2V /WE = Vcc - 0.2 V	tRAS ≤ 300ns	-	300	uA	1,4,5
		A0-9 = Vcc - 0.2 V, or 0.2 V DQ0-DQ3 = 0.2, Vcc - 0.2 V, or open	tRAS ≤ 1us	-	400		
I_{CC8}	Vcc Supply Current Self Refresh (SL-part only)	/RAS & /CAS ≤ 0.2V /OE & /WE & A0-9 = Vcc - 0.2 V, or 0.2 V DQ0-DQ3 = 0.2, Vcc - 0.2 V, or open			300	uA	5
V_{OL}	Output Low Voltage	I_{OL}= 4.2mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH} = -5mA		2.4	-	V	

NOTE

1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6}, and I_{CC7} depend on cycle rates.
2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading. Specified values are obtained with the output open.
3. Icc is specified as an average current. In I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while /RAS=VIL. In I_{CC4}, Address can be changed maximum once while /CAS=V_{IH}.
4. Only tRAS(max.) = 1us is applied to refresh of battery backup but tRAS(max.) = 10us is to applied to normal functional operation.
5. I_{CC5}(max.), I_{CC7} and I_{CC8} are applied to SL-part only.

AC CHARACTERISTICS

(T_A=0℃ to 70 ℃, Vcc=5V ± 10%, Vss=0V, unless otherwise noted.) NOTE : 1,2, 3,13

#	SYMBOL	PARAMETER	HY514404B						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	84	-	104	-	124	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	113	-	137	-	160	-	ns	
3	tHPC	EDO Page Mode Cycle Time	20	-	25	-	30	-	ns	
4	tHPRWC	EDO Page Mode Read-Modify-Write Cycle Time	61	-	70	-	78	-	ns	
5	tRAC	Access Time from /RAS	-	50	-	60	-	70	ns	4,9,10
6	tCAC	Access Time from /CAS	-	13	-	15	-	18	ns	4,9
7	tAA	Access Time from Column Address	-	25	-	30	-	35	ns	4,10
8	tCPA	Access Time from Column Precharge	-	30	-	35	-	40	ns	4,15
9	tCLZ	/CAS to Output Low Impedance	3	-	3	-	3	-	ns	4
10	tCEZ	Output Buffer Turn-off Delay Time from /CAS	3	10	3	13	3	15	ns	5
11	tT	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	3
12	tRP	/RAS Precharge Time	30	-	40	-	50	-	ns	
13	tRAS	/RAS Pulse Width	50	10k	60	10k	70	10k	ns	
14	tRASP	/RAS Pulse Width (EDO Page Mode)	50	200k	60	200k	70	200k	ns	
15	tRSH	/RAS Hold Time	13	-	15	-	18	-	ns	
16	tCSH	/CAS Hold Time	40	-	50	-	60	-	ns	
17	tCAS	/CAS Pulse Width	8	10k	11	10k	14	10k	ns	
18	tRCD	/RAS to /CAS Delay Time	18	37	20	45	20	52	ns	9
19	tRAD	/RAS to Column Address Delay Time	10	25	15	30	15	35	ns	10
20	tCRP	/CAS to /RAS Precharge Time	5	-	5	-	5	-	ns	15
21	tCP	/CAS Precharge Time	8	-	10	-	12	-	ns	17
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	14
25	tCAH	Column Address Hold Time	10	-	10	-	10	-	ns	14
26	tAR	Column Address Hold Time from /RAS	50	-	50	-	50	-	ns	
27	tRAL	Column Address to /RAS Lead Time	25	-	30	-	35	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	14
29	tRCH	Read Command Hold Time Referenced to /CAS	0	-	0	-	0	-	ns	6,14
30	tRRH	Read Command Hold Time Referenced to /RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	8	-	10	-	10	-	ns	14
32	tWCR	Write Command Hold Time from /RAS	40	-	50	-	55	-	ns	
33	tWP	Write Command Pulse Width	8	-	10	-	10	-	ns	
34	tRWL	Write Command to /RAS Lead Time	10	-	12	-	12	-	ns	
35	tCWL	Write Command to /CAS Lead Time	10	-	12	-	12	-	ns	16
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	10	-	10	-	ns	7
38	tDHR	Data-In Hold Time Referenced to /RAS	50	-	50	-	50	-	ns	

4M

AC CHARACTERISTICS

(Continued)

#	SYMBOL	PARAMETER	HY514404B						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
39	tREF	Refresh Period (1024cycles) (SL-part)	16 128	-	16 128	-	16 128	-	ms	12, 11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8,14
41	tCWD	/CAS to /WE Delay Time	30	-	34	-	40	-	ns	8
42	tRWD	/RAS to /WE Delay Time	67	-	79	-	92	-	ns	8
43	tAWD	Column Address to /WE Delay Time	42	-	49	-	57	-	ns	8
44	tCSR	/CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	14
45	tCHR	/CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	15
46	tRPC	/RAS to /CAS Precharge Time	5	-	5	-	5	-	ns	14
47	tCPT	/CAS Precharge Time (CBR Counter Test)	15	-	20	-	25	-	ns	17
48	tROH	/RAS Hold Time Reference to /OE	10	-	10	-	10	-	ns	
49	tOEA	/OE Access Time	-	13	-	15	-	18	ns	
50	tOED	/OE to Data Delay Time	13	-	15	-	18	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from /OE	3	13	3	15	3	18	ns	5
52	tOEH	/OE Command Hold Time	13	-	15	-	18	-	ns	
53	tCPWD	/WE Delay Time from /CAS Precharge	47	-	54	-	62	-	ns	8
54	tRHCP	/RAS Hold Time from /CAS Precharge	30	-	35	-	40	-	ns	
55	tWRP	/WE to /RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	/WE to /RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
57	tRASS	/RAS Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	ns	
58	tRPS	/RAS Precharge Time	90	-	110	-	130	-	ns	
59	tCHS	/CAS Hold Time (Self Refresh Cycle)	-50	-	-50	-	-50	-	ns	
60	tDOH	Output Data Hold Time	5	-	5	-	5	-	ns	
61	tREZ	Output Buffer Turn- off Delay from /RAS	3	13	5	15	5	18	ns	
62	tWEZ	Output Buffer Turn- off Delay from /WE	3	13	5	15	5	18	ns	
63	tWED	/WE to Data Delay Time	13	-	15	-	15	-	ns	
64	tOEP	/OE High Pulse Width	5	-	5	-	8	-	ns	
65	tWPE	/WE Pulse Width for Output Disable When /CAS High	5	-	5	-	8	-	ns	
66	tOCH	/OE to /CAS Hold Time	0	-	0	-	0	-	ns	
67	tCHO	/CAS Hold Time to /OE	5	-	5	-	8	-	ns	

NOTE

1. An initial pause of 200us is required after power-up followed by 8 /RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 /CAS-before-/RAS initialization cycles instead of 8 /RAS-only refresh cycles are required.
2. If /RAS=Vss during power-up, the HY514404B could begin an active cycle. This condition results in higher current than necessary current which is demanded from the power supply during power-up. It is recommended that /RAS and /CAS track with Vcc during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min.) and V_{IL}(max.), and are assumed to be 5ns for all inputs.
4. Measured at V_{OH}=2.0V and V_{OL}=0.8V with a load equivalent to 2 TTL loads and 100pF.
5. tCEZ(max.) and tOEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. These parameters are referenced to /CAS leading edge in early write cycles and to /WE leading edge in Read-Modify-Write cycles.
8. tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS ≥ tWCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tRWD ≥ tRWD(min.), tCWD ≥ tCWD(min.), tAWD ≥ tAWD(min.), and tCPWD ≥ tCPWD(min.), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. Operation within the tRCD(max.) limit ensures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit ensures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. tREF(max.)=128ms is applied to SL-parts only.
12. A burst of 1024 /CAS-before-/RAS refresh cycles must be executed within 16ms (128ms for SL-parts) after exiting self refresh.
13. When /CAS goes low, 4-bits data are written into the device.
14. These parameters are determined by the earlier falling edge of /CAS.
15. These parameters are determined by the later rising edge of /CAS.
16. tCWL must be satisfied by /CAS for 4-bits access cycles.
17. tCP and tCPT are measured when /CAS is high state.

CAPACITANCE

(T_A=25℃, Vcc=5V ± 10%, Vss=0V, If = 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0 - A9)	-	5	pF
C_{IN2}	Input Capacitance (/RAS, /CAS, /WE, /OE)	-	7	pF
C_{DQ}	Data Input /Output Capacitance (DQ0 - DQ3)	-	7	pF