

FEATURES

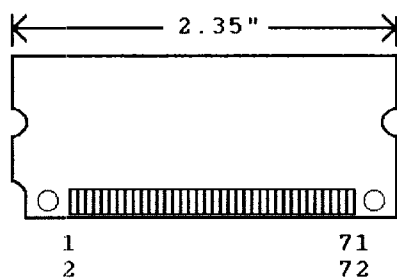
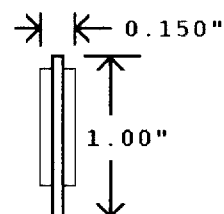
- 72-pin industry standard 4-byte small outline Dual-in-line memory module
- JEDEC compliant: 21-C, Fig. 4-15 A, C
: No. 95 MO-160
- High performance, CMOS
- Single $3.3 \pm 0.3V$ power supply
- LVTTTL-compatible inputs and outputs
- Fast Page Mode access cycle
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS, HIDDEN, SELF
- Refresh: 1024 refresh cycles every 128 ms
- Dimensions: 2.35" (length) x 1.00" (height) x 0.150" (max thickness)

PERFORMANCE RANGE

SYMBOL	PARAMETER	Rating	
		60 ns	70 ns
t_{RAC}	RAS Access Time	60 ns (max)	70 ns (max)
t_{CAC}	CAS Access Time	20 ns (max)	25 ns (max)
t_{AA}	Access Time from Column Address	35 ns (max)	40 ns (max)
t_{RC}	Random Read or Write Cycle Time	110 ns (min)	130 ns (min)
t_{PC}	Fast Page Mode Cycle Time	45 ns (min)	50 ns (min)

ORDERING INFORMATION

DESCRIPTION	PART NUMBER	ENGINEERING DESCRIPTOR
1M X 32, 60 ns, Gold Tabs, TSOP	20270C	CL001S01320LPAT-60
1M X 32, 70 ns, Gold Tabs, TSOP	20271C	CL001S01320LPAT-70

CARD OUTLINE

TOP VIEW

SIDE VIEW
GENERAL DESCRIPTION

The 1M x 32 SODIMM uses dynamic RAM devices and is designed for use as a general-purpose 4-byte wide memory assembly with 8 data bits per byte. The SODIMM is populated with eight 1M x 4 DRAMs.

During Read or Write Cycles, each byte may be uniquely addressed via 20 address bits, with the first 10 bits (A0~A9) latched on \overline{RAS} and the latter 10 bits (A0~A9) latched on \overline{CAS} . READ or WRITE cycles are selected with the \overline{WE} input, with a logic low indicating a WRITE cycle and a logic HIGH indicating a READ cycle. During a WRITE cycle, data-in is latched by the falling edge of \overline{WE} or \overline{CAS} , whichever occurs last.

FAST PAGE MODE operation allows for faster READs or WRITEs within a row-address-defined page boundary. A FAST PAGE MODE cycle is initiated with \overline{RAS} followed by \overline{CAS} , then strobing \overline{CAS} to latch different column addresses while holding \overline{RAS} LOW.

Returning \overline{RAS} and \overline{CAS} high terminates a memory cycle and returns the DRAMs to a reduced-current STANDBY state.

Memory cell data is retained in its correct state by maintaining power and executing any \overline{RAS} cycle (READ, WRITE) or \overline{RAS} refresh cycle (\overline{RAS} -ONLY, CBR, HIDDEN, and SELF REFRESH) so that all 1024 combinations of \overline{RAS} addresses (A0~A9) are executed at least every 128 ms. The CBR, HIDDEN, and SELF refresh cycles will invoke the on-chip refresh address counters for automatic \overline{RAS} addressing.

PIN DESCRIPTION

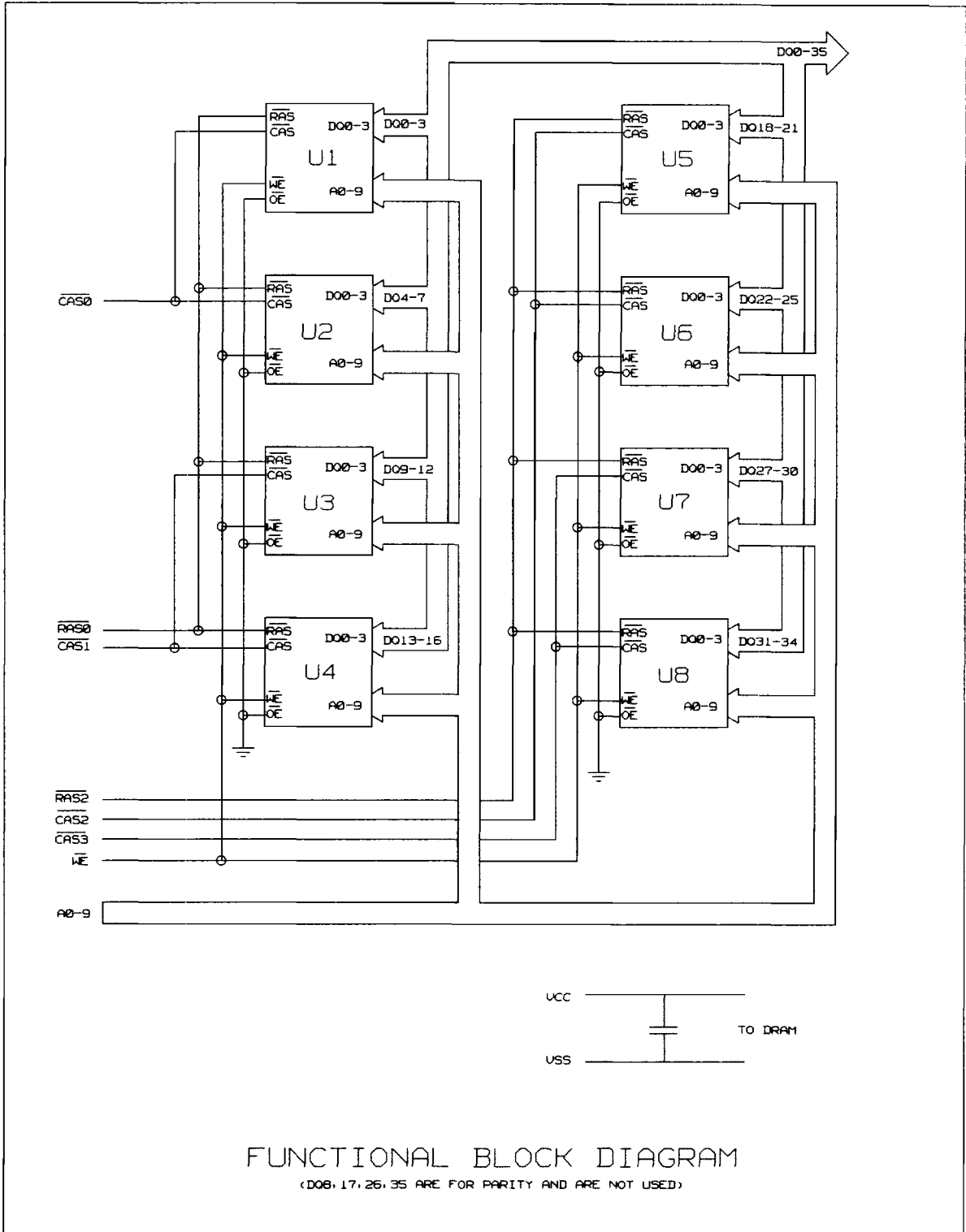
RAS0,RAS2	Row Address Strobe
CAS0~CAS3	Column Address Strobe
WE	Write Enable
A0~A9	Address Input
DQ0~7, DQ9~16, DQ18~25, DQ27~34	Data Input/Output
VCC	Power (+3.3V)
VSS	Ground
NC	No Connect
DU	Don't Use

PRESENCE DETECT

PIN SYMBOL	CONFIGURATION	
	60 ns	70 ns
PD1 (PD1~PD4: Addressing/Density)	NC	NC
PD2	VSS	VSS
PD3	VSS	VSS
PD4	NC	NC
PD5 (PD5~PD6: Speed)	NC	VSS
PD6	NC	NC
PD7 (PD7: Refresh)	VSS	VSS

PIN CONFIGURATION

Pin #	Front Side	Pin #	Front Side	Pin #	Back Side	Pin #	Back Side
1	VSS	37	DQ18	2	DQ0	38	DQ19
3	DQ1	39	VSS	4	DQ2	40	CAS0
5	DQ3	41	CAS2	6	DQ4	42	CAS3
7	DQ5	43	CAS1	8	DQ6	44	RAS0
9	DQ7	45	NC	10	VDD	46	NC
11	PD1	47	WE	12	A0	48	NC
13	A1	49	DQ20	14	A2	50	DQ21
15	A3	51	DQ22	16	A4	52	DQ23
17	A5	53	DQ24	18	A6	54	DQ25
19	NC	55	NC	20	NC	56	DQ27
21	DQ9	57	DQ28	22	DQ10	58	DQ29
23	DQ11	59	DQ31	24	DQ12	60	DQ30
25	DQ13	61	VDD	26	DQ14	62	DQ32
27	DQ15	63	DQ33	28	A7	64	DQ34
29	NC	65	NC	30	VDD	66	PD2
31	A8	67	PD3	32	A9	68	NC
33	NC	69	PD5	34	RAS2	70	PD6
35	DQ16	71	PD7	36	NC	72	VSS



TRUTH TABLE

FUNCTION	RAS	CAS	WE	OE	ROW ADDR	COL ADDR	DQx
Standby	H	X	X	X	X	X	Hi-Z
Read	L	L	H	L	ROW	COL	Valid D _{OUT}
Early-Write	L	L	L	X	ROW	COL	Valid D _{IN}
RMW	L	L	H-L	L-H	ROW	COL	Valid D _{OUT}
Fast Page Mode-Read 1st Cycle	L	H-L	H	L	ROW	COL	Valid D _{OUT}
Subsequent Cycles	L	H-L	H	L	N/A	COL	Valid D _{OUT}
Fast Page Mode-Write 1st Cycle	L	H-L	L	X	ROW	COL	Valid D _{IN}
Subsequent Cycles	L	H-L	L	X	N/A	COL	Valid D _{OUT}
Fast Page Mode-RMW 1st Cycle	L	H-L	H-L	H-L	ROW	COL	Valid D _{OUT}
Subsequent Cycles	L	H-L	H-L	H-L	N/A	COL	Valid D _{OUT}
RAS-Only Refresh	L	H	X	X	ROW	N/A	Hi-Z
CAS-Before-RAS Refresh	H-L	L	H	X	X	X	Hi-Z
Self Refresh	H-L	L	H	X	X	X	Hi-Z

X:"H" or "L" DIN:Data In DOUT:Data Out Hi-Z:High Impedance N/A:Not Applicable

ABSOLUTE MAXIMUM RATINGS (Note 1,22)

SYMBOL	PARAMETER	RATING	UNITS	NOTES
V _{CC}	Power Supply Voltage	-0.5 to 4.6	V	2
V _{IN}	Voltage on any Pin Relative to V _{SS}	-0.5 to 4.6	V	2
V _{OUT}		-0.5 to 4.6	V	2
T _{opr}	Operating Temperature	0 to 70	°C	
T _{stg}	Storage Temperature	-55 to 120	°C	
P _D	Power Dissipation	8.0	W	17,31
I _{OS}	Short Circuit Output Current	50	mA	17

RECOMMENDED OPERATING CONDITIONS ($T_A = 0$ to 70 °C) (Note 2)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	3	3.3	3.6	V	
V_{SS}	Ground	0	0	0	V	
V_{IH}	Input High Voltage	2		$V_{CC} + 0.3$	V	22
V_{IL}	Input Low Voltage	-0.3		0.8	V	22

 T_A : Ambient temperature

CAPACITANCE ($f = 1$ MHz; $T_A = 25$ °C) (Note 22)

SYMBOL	PARAMETER	MAX.	UNITS	NOTES
C_{I1}	Input Capacitance (A0-A9)	48	pF	
C_{I2}	Input Capacitance (RAS0,RAS2)	28	pF	
C_{I3}	Input Capacitance (CAS0~CAS3)	14	pF	
C_{I4}	Input Capacitance (WE)	56	pF	
C_{O1}	Output Capacitance (Data In/Out)	7	pF	

 T_A : Ambient temperature

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) (Note 18,22)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	NOTES	
I _{CC1}	OPERATING CURRENT: Average Power Supply Operating Current ($\overline{RAS}, \overline{CAS}$, Address Cycling @ $t_{RC} = t_{RC(min)}, V_{CC} = V_{CC(max)}$) (mA)	60 ns	-	640	3,4,5,6, 16	
		70 ns	-	560		
I _{CC2}	STANDBY CURRENT (TTL): Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC}$, Data out is disabled (Hi-Z), all other inputs = V_{CC} , $V_{CC} = V_{CC(max)}$) (mA)	Don't Care	-	16		
I _{CC3}	RAS-ONLY REFRESH CURRENT: Average Power Supply Current, RAS-Only Mode (\overline{RAS} , Address Cycling, $\overline{CAS} = V_{IH}$ @ $t_{RC} = t_{RC(min)}, V_{CC} = V_{CC(max)}$) (mA)	60 ns	-	640	3,4,5,6,16, 31	
		70 ns	-	560		
I _{CC4}	FAST PAGE MODE CURRENT: Average Power Supply Current, FPM ($\overline{RAS} = V_{IL}, \overline{CAS}$, Address Cycling @ $t_{PC} = t_{PC(min)}, V_{CC} = V_{CC(max)}$) (mA)	60 ns	-	560	3,4,5,7,16	
		70 ns	-	480		
I _{CC5}	STANDBY CURRENT (CMOS): Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$, Data Out is disabled (Hi-Z), $V_{CC} = V_{CC(max)}$) (mA)	Don't Care	-	4		
I _{CC6}	CAS-BEFORE-RAS, REFRESH CURRENT: Average Power Supply Current, CAS-Before-RAS Mode ($\overline{RAS}, \overline{CAS}$ Cycling @ $t_{RC} = t_{RC(min)}, V_{CC} = V_{CC(max)}$) (mA)	60 ns	-	560	3,4,5,6,16, 31	
		70 ns	-	480		
I _{LI}	INPUT LEAKAGE CURRENT: Input Leakage Current, any input ($0 \leq V_{IN} \leq V_{CC}$, all other pins not under test = 0V, $V_{CC} = V_{CC(max)}$) (μA)	A0~A9		-80	80	
		RAS0, RAS2		-40	40	
		CAS0~CAS3		-20	20	
		WE		-80	80	
I _{LO}	OUTPUT LEAKAGE CURRENT: (Data Out is disabled (Hi-Z), $0 \leq V_{OUT} \leq V_{CC}$) (μA)		-10	10		
V _{OH}	OUTPUT HIGH LEVEL: Output "H" Level Voltage ($I_{OUT} = -5mA$) (V)		2.4	-	2	
V _{OL}	OUTPUT LOW LEVEL: Output "L" Level Voltage ($I_{OUT} = +4.2mA$) (V)		-	0.4	2	

AC CHARACTERISTICS
READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES (COMMON PARAMETERS)

(Recommended operating conditions unless otherwise noted.) (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Random READ or WRITE Cycle Time (ns)	110	-	130	-	
t_{RP}	RAS Precharge Time (ns)	40	-	50	-	
t_{CP}	CAS Precharge Time (ns)	10	-	10	-	
t_{RAS}	RAS Pulse Width (ns)	60	10000	70	10000	23
t_{CAS}	CAS Pulse Width (ns)	20	10000	25	10000	23
t_{ASR}	Row Address Setup Time (ns)	0	-	0	-	22
t_{RAH}	Row Address Hold Time (ns)	10	-	10	-	
t_{ASC}	Column Address Setup Time (ns)	0	-	0	-	22
t_{CAH}	Column Address Hold Time (ns)	15	-	15	-	22
t_{RCD}	RAS to CAS Delay Time (ns)	20	45	20	50	10
t_{RAD}	RAS to Col. Address Delay Time (ns)	15	30	15	35	15
t_{RSH}	RAS Hold Time (ns)	15	-	20	-	22
t_{CSH}	CAS Hold Time (ns)	60	-	70	-	
t_{CRP}	CAS to RAS Precharge Time (ns)	5	-	5	-	22
t_{ODD}	OE to D _{IN} Delay Time (ns)	15	-	20	-	22,27
t_{DZO}	OE Delay Time from D _{IN} (ns)	0	-	0	-	22,28
t_{RPC}	RAS Precharge to CAS hold Time (ns)	10	-	10	-	22
t_T	Transition Time (Rise and Fall) (ns)	3	30	3	30	22
t_{AR}	Column Address Hold Time Referenced to RAS (ns)	50	-	55	-	22

READ CYCLES (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{RAC}	Access Time from \overline{RAS} (ns)	-	60	-	70	9,10,15,30
t_{CAC}	Access Time from \overline{CAS} (ns)	-	20	-	25	9,10,30
t_{AA}	Access Time from Address (ns)	-	35	-	40	9,15,30
t_{OEA}	Access Time from \overline{OE} (ns)	-	20	-	25	9
t_{RCS}	Read Command Setup Time (ns)	0	-	0	-	22
t_{RCH}	Read Command Hold Time to \overline{CAS} (ns)	0	-	0	-	14,22
t_{RRH}	Read Command Hold Time to \overline{RAS} (ns)	0	-	0	-	14,22
t_{RAL}	Column Address to \overline{RAS} Lead Time(ns)	30	-	35	-	22
t_{CLZ}	\overline{CAS} to Output in Low-Z (ns)	0	-	0	-	9,22
t_{OEZ}	Output Buffer Turn-off Delay from \overline{OE} (ns)	0	15	0	20	12,24
t_{DZC}	Data to \overline{CAS} Low Delay Time (ns)	0	-	0	-	28
t_{CDD}	\overline{CAS} High to Data Delay Time (ns)	13	-	15	-	27
t_{OFF}	Output Buffer Turn-Off Delay (ns)	0	15	0	20	12,24

WRITE CYCLES (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t_{WCS}	Write Command Set Up Time (ns)	0	-	0	-	13
t_{WCH}	Write Command Hold Time (ns)	10	-	15	-	
t_{WP}	Write Command Pulse Width (ns)	10	-	15	-	
t_{RWL}	Write Command to \overline{RAS} Lead Time (ns)	20	-	20	-	22
t_{CWL}	Write Command to \overline{CAS} Lead Time (ns)	15	-	20	-	
t_{DS}	D_{IN} Setup Time (ns)	0	-	0	-	25
t_{DH}	D_{IN} Hold Time (ns)	10	-	15	-	22,25
t_{WCR}	Write Command Hold Time Referenced to \overline{RAS} (ns)	50	-	55	-	22
t_{DHR}	Data in Hold Time Referenced to \overline{RAS} (ns)	50	-	55	-	22

FAST PAGE MODE CYCLES (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t _{PC}	Fast Page Mode Cycle Time (ns)	45	-	50	-	
t _{RASP}	Fast Page Mode RAS Pulse Width (ns)	60	100000	70	100000	22
t _{CPRH}	RAS Hold Time from CAS Precharge (ns)	35	-	40	-	22
t _{CPA}	Access Time from CAS Precharge (ns)	-	35	-	40	9,21,22,30
t _{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time (ns)	90	-	105	-	
t _{CPW}	WE Delay Time From CAS Precharge (ns)	60	-	70	-	13

REFRESH CYCLE (Note 8,18)

SYMBOL	PARAMETER	60 ns		70 ns		NOTES
		MIN.	MAX.	MIN.	MAX.	
t _{CHR}	CAS Hold Time (CAS-before-RAS Refresh Cycle) (ns)	10	-	15	-	22
t _{CSR}	CAS Setup Time (CAS-before-RAS Refresh Cycle) (ns)	10	-	10	-	22
t _{WRP}	WE Setup Time (CAS-before-RAS Refresh Cycle) (ns)	10	-	10	-	22
t _{WRH}	WE Hold Time (CAS-before-RAS Refresh Cycle) (ns)	10	-	10	-	22
t _{REF}	Refresh Period (1024 cycles) (ms)	-	16	-	16	
t _{RASS}	RAS Pulse Width (CAS-before-RAS Self Refresh Cycle) (us)	100	-	100	-	32
t _{RPS}	RAS Precharge Time (CAS-before-RAS Self Refresh Cycle) (ns)	110	-	130	-	32
t _{CHS}	CAS Hold Time (CAS-before-RAS Self Refresh Cycle) (ns)	-50	-	-50	-	32

NOTES

1. Permanent damage to the device may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages referenced to V_{SS} .
3. I_{CC} is specified as an average current.
4. This parameter depends on output loading and/or cycle rates.
5. Specified values are obtained with the output open.
6. Address can be changed a maximum of once while $\overline{RAS}=V_{IL}$.
7. Address can be changed a maximum of once while $\overline{CAS}=V_{IH}$.
8. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition time (t_T) is measured between $V_{IH(min)}$ and $V_{IL(max)}$, and is assumed to be 5ns for all inputs. All input signals must transit between V_{IH} and V_{IL} (or V_{IL} and V_{IH}) without slope reversal.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. Operation within the $t_{RCD(max)}$ limit ensures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC} .
11. Assumes that $t_{RAD} \leq t_{RAD(max)}$.
12. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
13. This is a non-restrictive operating parameter. It is included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out pins will remain high impedance (open circuit) for the duration of the cycle. If $t_{CWD(min)} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$, and $t_{CPW} \geq t_{CPW(min)}$ (for Fast Page Mode cycle only), then the cycle is a Read-Modify-Write cycle and the data output pins will hold the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out (at access time) is indeterminate.
14. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
15. Operation within the $t_{RAD(max)}$ limit ensures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled exclusively by t_{AA} .
16. Specified values are obtained with minimum cycle time.
17. Specified values are obtained with $T_A = 25^\circ\text{C}$.

18. An initial pause of 200 μ s is required after power-up followed by a minimum of eight initialization cycles (any 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ -only Refresh cycles with $\overline{\text{WE}}$ high) before proper device operation is assured. Also, any 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ -only Refresh cycles with $\overline{\text{WE}}$ high are required after prolonged periods (greater than t_{REF}) of $\overline{\text{RAS}}$ inactivity before proper device operation is assured.
19. Measured with a load equivalent to 50pF and 500 ohms.
20. Write cycle is applicable instead of read cycle. Timing requirements for $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and Address are the same for Hidden Refresh Write Cycle as that shown for Hidden Refresh Read Cycle. $\overline{\text{WE}}$, D_{IN} and D_{OUT} for Hidden Refresh Write Cycle are the same as for Write Cycle.
21. t_{CPA} is access time from $\overline{\text{CAS}}$ precharge (that is caused by changing $\overline{\text{CAS}}$ from "L" to "H"). Therefore, if t_{CP} is long, then t_{CPA} is longer than $t_{\text{CPA}(\text{max})}$.
22. Calculated based on data supplied by the DRAM manufacturer(s).
23. Maximum value is calculated based on data supplied by the DRAM manufacturer(s).
24. Minimum value is calculated based on data supplied by the DRAM manufacturer(s).
25. This parameter is referenced to the $\overline{\text{CAS}}$ leading edge in Early Write cycles and to the $\overline{\text{WE}}$ leading edge in Read-Modify-Write cycles.
26. $V_{\text{IN}} = 0$ Volt.
27. Either t_{CDD} or t_{ODD} must be satisfied.
28. Either t_{DZC} or t_{DZO} must be satisfied.
29. $t_{\text{RASP}(\text{MIN})}$ is specified as two cycles of $\overline{\text{CAS}}$ input are performed.
30. The access time is limited by all four parameters t_{RAC} , t_{CAC} , t_{AA} , t_{CPA} .
31. This assumes all $\overline{\text{RAS}}$ (and all $\overline{\text{CAS}}$ for CBR refresh) are active.
32. For all of the refresh modes except for distributed CBR refresh, 4K/2K refresh cycles of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification.

For Timing Diagrams see “**FPM Timing Diagrams**” (Document No. 20432C).

Available from fax-on-demand and Website: <http://www.celestica.com/memory/>

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