Consumer Microcircuits Limited

COMMUNICATION SEMICONDUCTORS

CMX880

Baseband Processor For Mixed Mode Land Mobile Radio

D/880/1 February 2001

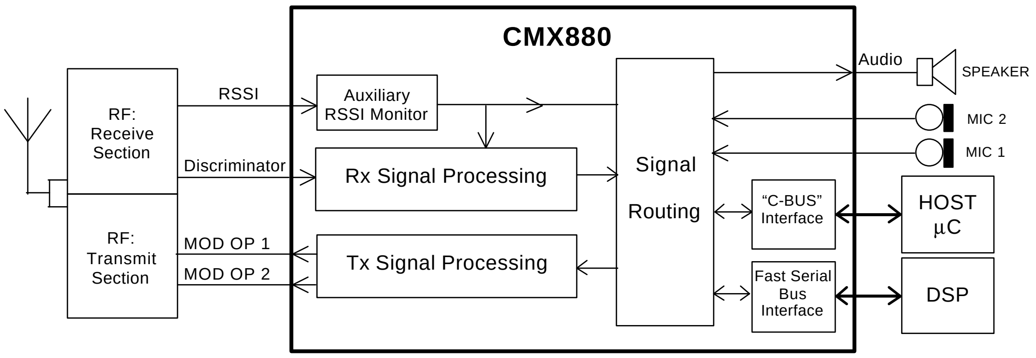
Advance Information

Features

- **CQPSK/C4FM Modem**
- **FFSK/MSK Modem, 1200/2400 bps**
- **CTCSS and Selcall Tone Codecs**
- **23/24 Bit DCS Codec**
- **DTMF Encoder**
- **Two Independent Serial Interface Ports**
- **Versatile 'Power-save' Modes**

Applications

- **APCO 25 LMR Terminals**
- **Multiple Analogue PMR Modes**
- **Dual Mode Analogue and Digital LMR**
- **Half Duplex Analogue Radio**
- **GMRS Radio**



2.7V LOW POWER OPERATION

1.1 Brief Description

The CMX880 is a signalling encoder/decoder intended to work in conjunction with a host micro-controller (µC) and a digital signal processor (DSP) in dual-mode analogue and digital, two-way land mobile radio equipment. It is particularly suited to APCO 25 LMR terminal designs.

The CMX880 incorporates A-to-D and D-to-A converters with signal processing for various radio signalling formats. The CMX880 automatically starts-up, issues a wake up notice to the host µC/DSP, identifies the type of incoming signal and then performs the appropriate signal decoding of that signal. It performs the transceiver baseband processing for CTCSS, DCS, Voice, Selcall, FFSK/MSK and C4FM signal formats. The CMX880 can also be used to transmit DTMF or CQPSK signal formats. If the CMX880 is receiving or transmitting C4FM or CQPSK, a DSP is required to perform the processing of some APCO 25 message protocols, such as error detection/correction, voice coding/decoding and station ID/data packet extraction. The CMX880 can be used without a DSP when operating in analogue PMR/LMR applications that exclude C4FM and CQPSK.

The CMX880 is ideal for low power applications, working down to 2.7V across the temperature range –40°C to +85°C. It features facilities that allow the device and DSP to be placed in low power mode when the terminal is in standby mode. The CMX880 is available in 28-pin SSOP and TSSOP package options.

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Figure Page

Note: This product is in development: Changes and additions will be made to this specification. Items marked TBD or left blank will be included in later issues.

Information in this data sheet should not be relied upon for final product design.

1.2 Block Diagram

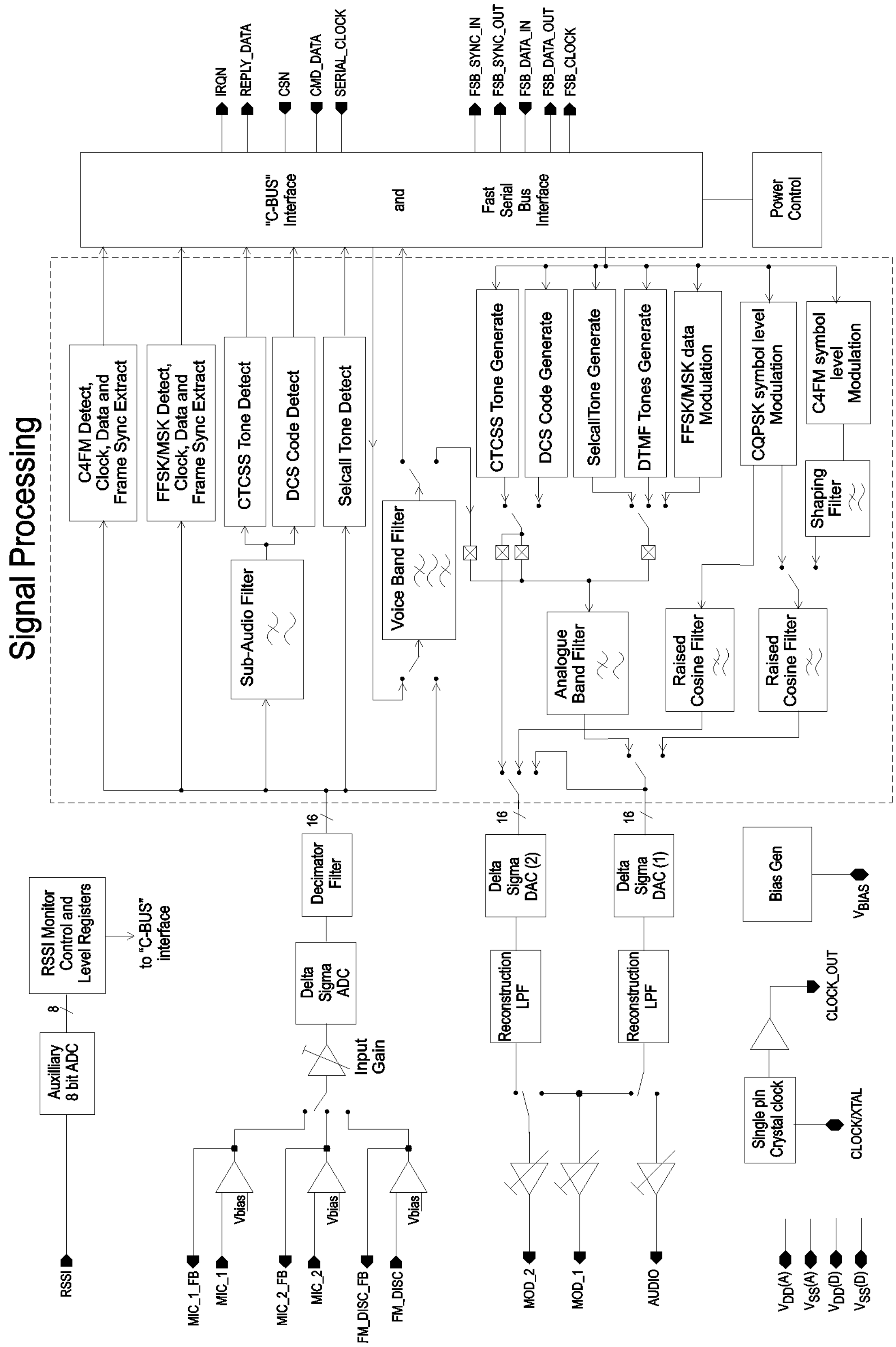


Figure 1 Block Diagram

1.3 Signal List

Package D6, E1	Signal		Description
Pin No.	**Name**	**Type**	
1	FSB_SYNC_OUT	O/P	Fast Serial Bus (FSB) Frame Sync for data transfer output to external DSP.
2	FSB_DATA_OUT	O/P	FSB Data output to external DSP.
26	FSB_DATA_IN	I/P	FSB Data input from external DSP.
27	FSB_SYNC_IN	O/P	FSB Frame Sync for data transfer input from external DSP.
28	FSB_CLOCK	O/P	FSB Clock output to external DSP.
3	IRQN	O/P	This output indicates an interrupt condition to the µC by going to a logic "0". This is a "wire-ORable" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µC. This pin has a low impedance pulldown to logic "0" when active and a high-impedance when inactive. An external pullup resistor is required. The conditions that cause interrupts are indicated in the ‘STATUS’ register and are effective if not masked out by a corresponding bit in the IRQ MASK register.
4	REPLY_DATA	T/S	The “C-BUS” serial data output to the µC. The transmission of REPLY_DATA bytes is synchronised to the SERIAL_CLOCK under the control of the CSN input. This 3-state output is held at high impedance when not sending data to the µC. See Figure 23 “C-BUS” Timing diagram.
6	SERIAL_CLOCK	I/P	The “C-BUS” serial clock input the µC, is used for transfer timing of commands and data to and from the device. See Figure 23 “C-BUS” Timing diagram.
7	CMD_DATA	I/P	The “C-BUS” serial data input from the µC. Data is loaded into this device in 8 or 16-bit words, MSB (B7 or B15) first and LSB (B0) last, synchronised to the SERIAL_CLOCK. See Figure 23 “C-BUS” Timing diagram.
8	CSN	I/P	The “C-BUS” data loading control function: this input is provided by the µC. Data transfer sequences are initiated, and completed by the CSN signal. See Figure 23 “C-BUS” Timing diagram.

1.3 Signal List (continued)

Package D6,E1	Signal		Description
Pin No.	**Name**	**Type**	
5	V_{SS}(D)	Power	The negative supply rail (digital ground).
9, 21	V_{SS}(A)	Power	The negative supply rail (analogue ground).
18	V_{DD}(A)	Power	The analogue positive supply rail. This pin should be decoupled to V_{SS}(A) by a capacitor.
23	V_{DD}(D)	Power	The digital positive supply rail. This pin should be decoupled to V_{SS}(D) by a capacitor.
10	V_{BIAS}	O/P	A bias line for the internal circuitry, held at approx. ½ V_{DD}(A). This pin must be decoupled to $V_{SS(A)}$ by a capacitor mounted close to the device pins.
11	FM_DISC	I/P	Input terminal of FM discriminator input amplifier.
12	FM_DISC_FB	O/P	Output/ feedback terminal of FM discriminator input amplifier.
13	MIC_1	I/P	Input terminal of Microphone 1 input amplifier.
14	MIC_1_FB	O/P	Output/feedback terminal of Microphone 1 input amplifier.
15	MIC_2	I/P	Input terminal of Microphone 2 input amplifier.
16	MIC_2_FB	O/P	Output/feedback terminal of Microphone 2 input amplifier.
17	RSSI	I/P	Received signal strength indicator input.
19	MOD_1	O/P	Modulator 1 drive output.
20	MOD_2	O/P	Modulator 2 drive output.
22	AUDIO	O/P	Output of the audio section.
24	CLOCK/XTAL	I/P	The input to the on-chip oscillator for an external crystal or a clock circuit.
25	CLOCK_OUT	O/P	Buffered (un-inverted) clock output available for use by other devices in the system.

Notes: I/P = Input
O/P = Output
T/S = 3-state Output

1.4 External Components

Figure 2 and Figure 3 show the recommended external component configuration and power supply de-coupling and connections.

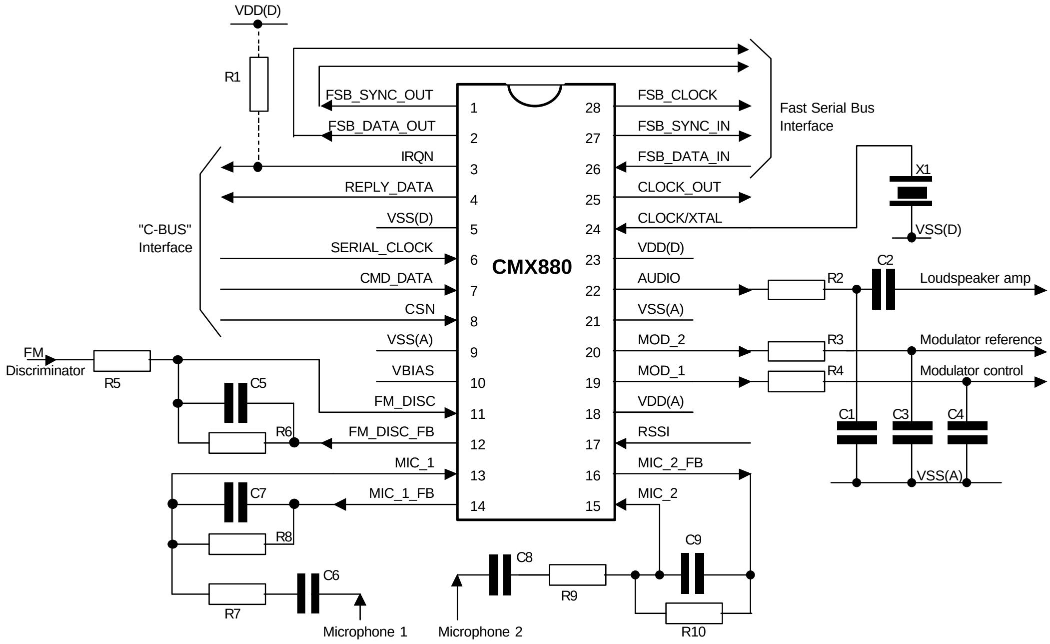


Figure 2 Recommended External Components

X1	15.36MHz See note 1				
R1	100kΩ	R5	See note 2	R9	See note 3
R2	100kΩ	R6	100kΩ	R10	100kΩ
R3	100kΩ	R7	See note 3		
R4	100kΩ	R8	100kΩ		
C1	100pF	C4	100pF	C7	200pF
C2	1nF	C5	100pF	C8	See note 4
C3	100pF	C6	See note 4	C9	200pF

Resistors ±5%, capacitors ±20% unless otherwise stated.

Notes

1. X1 can be a crystal or a temperature compensated clock generator; this will depend on the application. The clock drift requirement is defined in section 1.7.1. The tracks between the crystal pins and pin 24 and pin 5 should be as short as possible to ensure maximum achievable stability.
2. R5 should be selected to provide the desired dc gain of the FM discriminator input, as follows:
$$R5 = 100\text{k}\Omega \,/\, |GAIN_{FM\ Disc}|$$
The gain should be such that the resultant output at the FM_DISC_FB pin is within the FM discriminator input signal range specified in section 1.7.1.

3. R7 and R9 should be selected to provide the desired dc gain (assuming C6 and C8 are not present) of the microphone inputs as follows:
$$R7 = 100\text{k}\Omega \,/\, |GAIN_{Mic1}|$$
$$R9 = 100\text{k}\Omega \,/\, |GAIN_{Mic2}|$$
The gain should be such that the resultant outputs at the MIC_1_FB and MIC_2_FB pins are within the microphone input signal range specified in section 1.7.1.

4. C6 and C8 should be selected to maintain the lower frequency roll-off of the microphone inputs as follows:

$$C6 = 30nF \times \left|GAIN_{Mic1}\right| \text{ (and } C6 > 1000\mu F / |R7|)$$
$$C8 = 30nF \times \left|GAIN_{Mic2}\right| \text{ (and } C8 > 1000\mu F / |R9|)$$

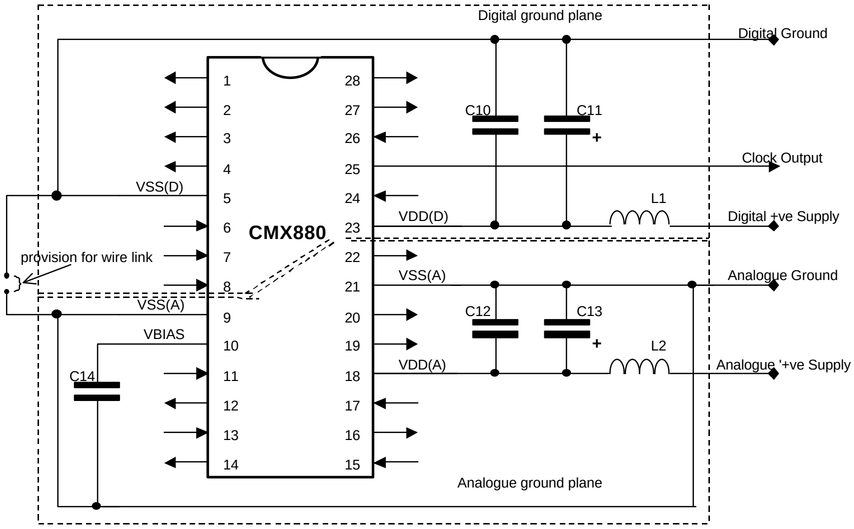


Figure 3 Power Supply Connections and De-coupling

L1	100nH (see note 5)	L2	100nH (see note 5)		
C10	10nF	C12	10nF	C14	100nF
C11	10µF	C13	10µF		

Resistors ±5%, capacitors ±20% unless otherwise stated.

Notes

5. The inductors L1 and L2 can be omitted but this may degrade system performance.

PCB Layout Guidelines and Power Supply Decoupling

It is important to protect the analogue pins from extraneous baseband noise and to minimise the impedance between the CMX880 and the supply and bias de-coupling capacitors. The de-coupling capacitors C10, C11, C12 and C13 should be as close as possible to the CMX880, particularly C10 and C12. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the V_{SS}(A) and V_{SS}(D) in the area of the CMX880, with provision to make a link between them close to the CMX880.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads are allowed. If V_{BIAS} needs to be used to set the FM discriminator mid-point reference, it must be buffered with a high input impedance buffer.

The single ended microphone inputs and audio output must be AC coupled as shown, so their return paths can be connected to V_{SS}(A) without introducing DC offsets. Further buffering of the audio output is advised.

If the CMX880 is being used for APCO 25 based applications, the crystal, X1, should be replace with a temperature compensated clock module with better than 10ppm accuracy. The internal clock generating circuit can be placed in power-save mode if the clock is provided externally.

Modulator Outputs

The combination of CMX880 and the modulator output components, R3/C3 and R4/C4, achieve roll-off rates better than –60dB/decade. This can be increased to better than –100dB/decade by replacing R3/C3 and R4/C4 with the active filter circuit shown in Figure 4.

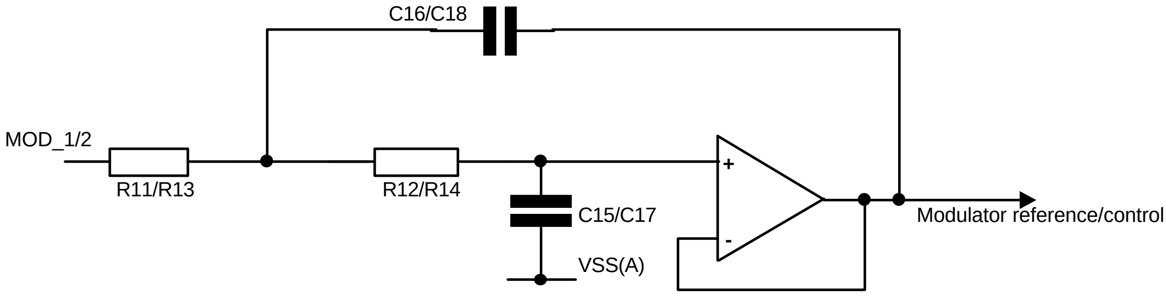


Figure 4 Modulator output components to achieve -100dB/decade roll-off

R11	120kΩ	C15	220pF	
R12	120kΩ	C16	440pF	(2 x C15)
R13	120kΩ	C17	220pF	
R14	120kΩ	C18	440pF	(2 x C17)

Resistors ±5%, capacitors ±20% unless otherwise stated.

The op amp must be chosen to ensure that the maximum possible signal output level can be driven without unacceptable distortion.

<***further notes tbd***>

1.5 General Description

The CMX880 works as a signalling encoder/decoder, in conjunction with a micro-controller (µC) and Digital Signal Processor (DSP). It is intended for use in half duplex, dual mode, analogue and digital two way land mobile radio (LMR) equipment and is particularly suited to APCO-25 LMR terminal designs. The DSP will perform the high level digital signal processing functions, such as forward error correction coding/decoding, voice coding/decoding, station ID and data packet extraction, whilst the CMX880 provides A-to-D and D-to-A conversion, plus a number of further radio signal encoder and decoder functions for Selcall, CTCSS, DCS, FFSK/MSK, DTMF, C4FM, CQPSK and voice. It can also be used in analogue only radio applications, without an external DSP. Power control facilities allow the device and external DSP to be placed in sleep mode, to conserve power when the terminal is in standby mode. The CMX880 includes a crystal (xtal) clock generator, with a buffered output to provide a common system clock if required. A block diagram of the CMX880 is shown in Figure 1.

Analogue Input Signal Processing Path

The analogue signal source is selected from either one of the two low noise microphone input amplifiers (for voice mode transmission) or the FM discriminator input amplifier (for signal reception). Analogue input selection is set by “C-BUS” command. The gain and frequency characteristics of the inputs are set by the external feedback networks shown in Figure 2. The configured input amplifiers act as anti-alias filters (AAF) for the ADC. The FM_DISC input must be DC coupled for receiving C4FM and DCS signals; the V_{BIAS} from the CMX880 can be used to set the FM discriminator reference, but it must be buffered as shown in Figure 2. The input signal is converted to a 16-bit word by the ADC before passing to the signal processing stage. The input stage gain can be adjusted within the range 0dB to 22.4dB in steps of 3.2dB, set by a “C-BUS” command.

Analogue Output Signal Processing Path

The output signals from the signal processing stage are converted from 16-bit words to analogue signals by the DACs. The signal outputs of each DAC pass through a reconstruction filter before being routed to the selected output ports. Signals are routed either to the audio port during reception of a voice message or to the modulator ports during transmit mode. The CMX880 has two modulator outputs, each with independently programmable gains that simplify implementation of two point modulation schemes. The output destination, the gain of the audio output amplifier and the gain of the modulator output amplifiers are set by “C-BUS” command.

Interfaces

The CMX880 has two digital interfaces, the “C-BUS” and the Fast Serial Bus (FSB). The “C-BUS” is used for command, status and data transfers between the CMX880 and the host µC. An interrupt signal notifies the host µC that a change in status has occurred. The µC should read the new status across the “C-BUS” and respond accordingly. **Note** Interrupts only occur if the appropriate mask bits have been set. See section 1.5.2.1.

The FSB provides an independent full duplex data transfer link with the DSP.

Signal Processing Functions

The signal processing unit performs the various voice, in-band, sub-audio, FFSK/MSK and C4FM receive and transmit processing tasks. A summary of these tasks is described here, with the detail provided in subsequent sections.

Processing of signal data from the ADC:

- Low pass filtering and decimation (by various function dependent ratios) of the signal from the FM discriminator or from the microphone inputs.
- Voice band filtering for analogue channel signals to suppress the sub-audio range (below 300Hz) and limit the upper frequency range.
- Voice band filtering for APCO 25 digital channel signals, prior to digital voice encoding (by the DSP).
- Low pass sub-audio filtering (0 to 300Hz) for CTCSS and DCS decoding.
- CTCSS tone detection.
- Selcall tone detection.
- DCS filtering, data slicing and decoding - detect the single, pre-programmed 23 or 24-bit DCS code. The polarity of the DCS code is set by the user.

- C4FM sin(x)/x filtering of the ADC output, 24 symbol frame sync pattern detection, clock and level extraction and tracking and symbol level decoding (without error correction). The decoded symbol data is formatted into 8 bits, comprising 2 bits of symbol code and 6 bits of quality data. This is transferred to the DSP over the FSB in 16-bit words (2 symbols) at 2400 words/s.
- FFSK/MSK filtering, clock extraction, bit extraction and frame sync detection. Three different frame sync patterns (SYNC and SYND are user programmable; SYNT is the inverse of SYNC) can be recognised.

Processing of signal data to the DACs:

- Initial stages of the receive audio output signal interpolation filtering.
- Generate CTCSS tone for transmission.
- Generate DTMF or Selcall tones for transmission.
- Generate DCS code for transmission.
- C4FM symbol level encoding.
- CQPSK symbol encoding.
- FFSK/MSK data modulation.
- Transmit output signal filtering - Raised Cosine and Shaping, plus interpolation.

Auxiliary (RSSI) analogue signal

The CMX880 includes an RSSI input level sensing facility. This acts as an 8-bit successive approximation ADC and a two level signal sensor. The two level sensor facility can be used in conjunction with the power saving mode to wake up powered down blocks, and issue an interrupt on the IRQN line when the RSSI exceeds the preset threshold level. The auxiliary ADC voltage reference is taken directly from the V_{DD}(A) supply, so the RSSI signal level should be derived from this same voltage.

1.5.1 Operation

1.5.1.1 Sleep Mode

Power-on reset or a “C-BUS” general reset places the CMX880 into sleep mode, which results in all internal blocks, except the xtal clock circuit, being placed in power-saved mode. The xtal clock circuit can be power-saved but this must be done by an explicit “C-BUS” command. Power saving is achieved by turning off bias current sources or disabling local clocks, as appropriate.

During system standby periods, parts of the device can be put into sleep mode by the µC to conserve power. The RSSI input level detector can be programmed so that when the RSSI exceeds a threshold, an interrupt can be issued over the “C-BUS” and the receiver mode enabled (“woken up”) within 400µs. Power-on of the Bias generator is of the order of 10’s off milliseconds, so for auto-start-up mode, Bias must be on. If this time is too long to ensure no message data is lost, the FM disc. input and ADC path can be kept powered up whilst in standby mode. The receive modes and transmit modes can also be activated by commands from the “C-BUS”. On wake up, activation of the various signal path stages are phased appropriately to avoid causing unwanted transients. More details are provided in section 1.5.1.5 on Configuration Options.

Associated Control and Status

- Power down control

Mic 1 amp	Mic 2 amp	FM Disc	(inputs)
SD ADC	SD DAC 1	SD DAC 2	(converters)
Mod 1 amp	Mod 2 amp	Audio amp	(outputs)
RSSI monitor	Signal processing block	Xtal oscillator	
Bias			

- Power down status

1.5.1.2 RSSI Monitoring

The RSSI monitoring facility comprises an 8-bit ADC, a comparator, an 8-bit result data word and two 8-bit threshold registers, one defining the 'RSSI high' level and the other the 'RSSI low' level. The two threshold registers are combined into one 16-bit "C-BUS" register word. The ADC measures the RSSI signal at intervals that are set by "C-BUS" command. It is advised that the interval be set to < 120µs while waiting for a new incoming signal, so that the CMX880 and the DSP can be powered up and put into receive mode in time to avoid missing any message data. The default interval period following a reset is 12.5µs. Power dissipation of the RSSI monitor can be reduced by increasing the conversion interval. RSSI monitoring should be disabled during transmit.

The result of the most recent RSSI measurement can be read by "C-BUS" command at any time.

The RSSI monitor continuously compares the conversion results with the values in the 'RSSI high' or the 'RSSI low' threshold registers. The CMX880 issues an interrupt to the host µC to wake up the receive path when the RSSI signal exceeds the 'high' level threshold. The CMX880 issues an interrupt to the host µC to indicate a weak or absent received signal when it falls below the 'low' level threshold. The value in the 'low' register must be less than that of the 'high' register. This provides a user programmable hysteresis facility. The options for issuing interrupts and for automatic start-up are selected by "C-BUS" command.

The CMX880 can be programmed to wake up its receive path automatically (automatic start-up) when the RSSI signal exceeds the 'high' level threshold. While the CMX880 is in automatic start-up mode the FM Discriminator must be selected as the input signal path. When not in automatic start-up mode, it is recommended that the FM Discriminator be selected as the input signal during RSSI monitoring (in anticipation of receiving a message), to avoid subsequent switching of the input signal source.

The RSSI Monitoring options are controlled by the $B2, $B3 and $C0 "C-BUS" registers.

Associated Control and Status

- Enable/disable RSSI monitoring.
- Read the most recent RSSI level measurement.
- Select two level monitoring-select.
- Enable "Rx Wake Up" mode - used in conjunction with two level monitoring mode to automatically wake up the device's powered down receive path and identify the type of the incoming signal when the RSSI exceeds the 'high' threshold. Other paths are woken by µC command, as needed.
- High threshold level register; Low threshold level register.
- ADC measurement data/result.
- Interrupts: mask/status - (1) RSSI risen above level, (2) RSSI fallen below level.

1.5.1.3 Receive Mode

The CMX880 is designed to receive and decode both digital and analogue types of coded signal format. This facilitates meeting the basic requirement of the APCO Project 25 to provide an orderly migration to digital communications, whilst maintaining backward compatibility with existing analogue systems. The CMX880 can receive C4FM digitally encoded voice or Data signals or analogue voice or Data signal formats, covering CTCSS tone, Selcall tone, DCS code and FFSK/MSK. Reception of each of these signal types can be independently enabled/disabled by "C-BUS" command. The CMX880 continuously monitors the incoming signal for each enabled signal type. When one is detected, the operating mode changes to track the detected signal type only. By disabling all the decoding modes, the device can be configured to receive voice only signals with no decoding of the Selcall or CTCSS tone or DCS code. This will result in reception of all signals as if they are voice, including digital transmissions. In this case it is up to the user/host µC to respond appropriately to incoming signals.

Following a receive mode enable from the RSSI level detector, if receive mode is enabled, the CMX880 performs a sequence of signal type identification processes to determine what type of signal is being received. Once identified, the CMX880 continues to process the received signal in accordance with the protocol appropriate to that signal type.

If enabled, a "C-BUS" interrupt will be issued to notify the host µC of the presence and type of the incoming signal. Signal type status information can be read by the µC over the "C-BUS". The decoded voice or data can be routed to the external DSP over the Fast Serial Bus, to the host µC over the "C-BUS" or to the audio output port. The Fast Serial Bus protocols and timing are defined in section 1.5.1.7. The "C-BUS" protocols and timing are defined in section 1.5.1.6. Control of the routing options is defined in section 1.5.1.5. Suggested routing is shown in Table 1.

Table 1 Suggested Routing of Data

Data origin	Route	Destination
C4FM Data	FSB	External DSP
FFSK/MSK Data	"C-BUS"	Host µC
FFSK/MSK Data	FSB	External DSP
Analogue Channel voice	Internal	Audio Output Port

The audio output amplifier gain can be adjusted by the µC, via "C-BUS" command, to provide output volume control.

The output signal levels are all equalised (to V_{BIAS}) before switching between the audio port and the modulator ports, to prevent generation of frequency components outside the radio transmission band and to minimise unwanted audible transients. The Off/Power-save level of the modulator outputs is V_{BIAS}, so the audio output level must also be at this level before switching.

The CMX880 operates in half duplex, so whilst in receive mode the transmit path (microphone input and modulator output amplifiers) can be disabled and powered down.

<u>Receiving Voice Band Signals on Analogue Channels</u>

When a voice based signal is being received, it is up to the µC, in response to signal status information provided by the CMX880, to control muting/enabling of the voice band signal to the AUDIO output, or to route the digitised signal via the FSB or "C-BUS". When the signal type has been identified as an analogue voice signal, the digitised 16-bit samples are filtered and output at a sample rate of 8k samples/second (S/s). If data routed across the "C-BUS" is not read within 125µs *(the sample period)* of the interrupt, it will become overwritten by subsequent data.

If a voice plus CTCSS or DCS signal is detected, or the device is set to receive all signals as voice, the incoming signal is filtered, as shown in Figure 5 to remove sub-audio components and to minimise high frequency noise. The digitised voice data can then either be routed directly to the AUDIO output or read over the "C-BUS".

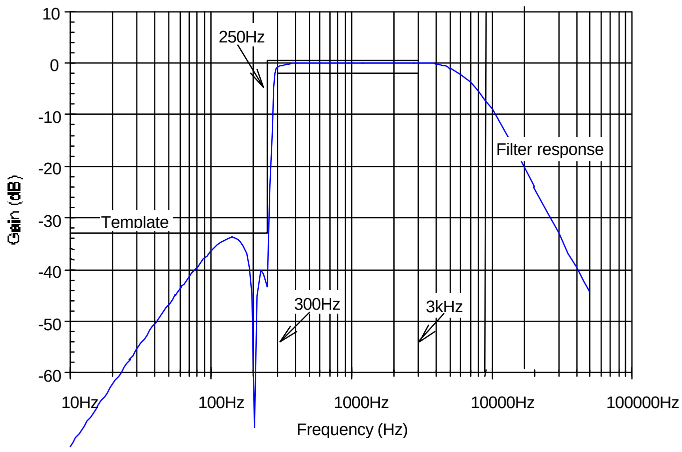


Figure 5 Analogue Channel, RX Audio Filter Frequency Response

The FM Discriminator path through the Delta-Sigma ADC has a programmable gain stage. Whilst in receive mode this should be set to full (the default) gain. This gain adjustment facility can be used, under host µC software control, to provide vogad capability when transmitting voice band from either of the microphone inputs, but is not intended for use whilst in receive mode.

De-emphasis at -6dB per octave from 300Hz to 3000Hz (shown in Figure 6) can be selected to facilitate compliance with TIA/EIA-603.

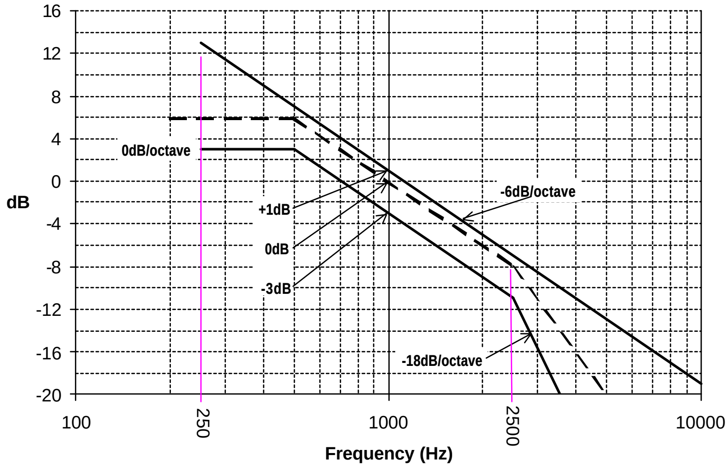


Figure 6 De-emphasis Curve for TIA/EIA-603 Compliance

Associated Control and Status

- Digitised voice data word.
- 'Data word present' flag and (interrupt) mask. Flag set if data is present and interrupt issued if appropriate mask bit is set.
- Audio output gain.
- Enable/ Mute/Power-save audio output.
- Enable De-emphasis.
- Data destination - to an external processor (µC/DSP) or direct to speaker output.

Receiving and Decoding CTCSS Tones

The CMX880 is able to accurately detect valid CTCSS tones quickly to avoid losing the beginning of voice transmissions, and is also able to continuously monitor the detected tone with minimal probability of falsely dropping out. The signal is filtered in accordance with the template shown in Figure 7, to prevent signals outside the sub-audio range from interfering with the sub-audio tone detection.

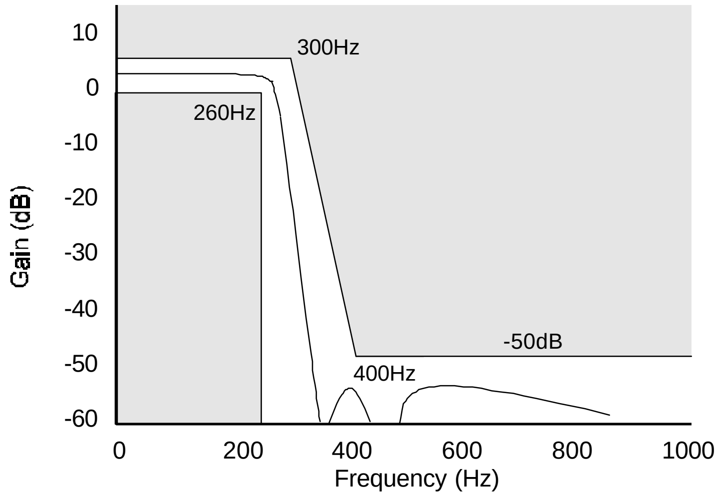


Figure 7 Low Pass Sub-Audio Band Filter for CTCSS and DCS

Once a valid CTCSS tone has been detected, the digitised voice band data is passed either to the µC/DSP or to the audio output. The destination is set by the µC. The voice band is extracted from the received input signal by band pass filtering as shown in Figure 5.

To decode received CTCSS tones, the CTCSS decoder should first be set up according to the desired characteristics. This entails setting the TONE decoder bandwidth and level in the 'CTCSS TONE BW AND LEVEL' word (B2.4) of the 'PROGRAMMING REGISTER' ($C8) and programming the centre frequencies of the desired tones in the 'RX CTCSS TONE' and 'RX CTCSS POLE COEFF' words (B2.6 to B2.37) of the 'PROGRAMMING REGISTER', which holds up to 16 different tones. Any tone can be in any location. When the device is decoding, the tones are scanned in the sequence of their location, i.e. tone 0 first and tone 15 last. Once a tone is detected the remaining tones are not checked. Therefore if two tones are close enough in frequency for their bandwidths to overlap then the one programmed in the lowest location will be detected.

The facility to decode any of up to 16 programmed tones allows the use of tones for various signalling functions such as masking a free channel or identifying sub groups within a user's groups.

Adjustable decoder bandwidths and threshold levels permit decode certainty and signal to noise performance to be traded when congestion or range limits the system performance.

Associated Control and Status

- Reset.
- Enable CTCSS Tone Detection - enables the tone detection and identification.
- 1-16 programmed tones.
- Set decoder bandwidth.
- Set tone detection threshold level.
- Interrupt masks - Fast Tone Detected; Tone Detected, Lost Tone.
- Interrupt flag - Fast Tone Detected; Tone Detected, Lost Tone. Flags set on change of associated status and interrupt issued if appropriate mask bit is set.
- Interrupt status - CTCSS Tone detected; Identification of tone frequency (one of the 15 pre-programmed tones); valid CTCSS (sub-audio) tone but not one of the preset frequencies; mode of tone detection - standard, fast or fast predictive, Lost Tone.

Table 2 lists the commonly used CTCSS tones together with the values for programming the ‘RX CTCSS TONE’ and ‘RX CTCSS POLE COEFF’ words. This does not preclude other tones being programmed. More details for programming CTCSS tones are provided in section 1.5.2.

Table 2 CTCSS Rx Tone Programming

Freq. (Hz)	Tone Code (hex)	Pole Coeff Code (hex)	Freq. (Hz)	Tone Code (hex)	Pole Coeff Code (hex)	Freq. (Hz)	Tone Code (hex)	Pole Coeff Code (hex)
67.0	41F2	490A	**114.8**	4361	4FB0	**186.2**	4567	5A4D
69.3	4207	495A	**118.8**	4380	5042	**189.9**	4586	5AE2
71.9	4214	49B5	**123.0**	43A0	50DC	**192.8**	45A3	5B58
74.4	422B	4A0D	**127.3**	43C0	517A	**196.6**	45C3	5BF2
77.0	4243	4A69	**131.8**	43E1	5220	**199.5**	45E0	5C69
79.7	424F	4AC8	**136.5**	4402	52CF	**203.5**	4600	5D0E
82.5	4268	4B2B	**141.3**	4423	5383	**206.5**	4605	5D8B
85.4	4282	4B91	**146.2**	4445	543B	**210.7**	4625	5E3A
88.5	428F	4BFF	**151.4**	4467	5500	**218.1**	4663	5F73
91.5	42A9	4C6A	**156.7**	4489	55CA	**225.7**	46A1	60B9
94.8	42C5	4CE0	**159.8**	44A6	5641	**229.1**	46C0	614D
97.4	42CF	4D3D	**162.2**	44C2	569D	**233.6**	46E0	6212
100.0	42E8	4D9A	**167.9**	44E5	577A	**241.8**	4720	637F
103.5	4306	4E18	**173.8**	4520	5861	**250.3**	4760	6500
107.2	4324	4E9D	**179.9**	4543	5952	**254.1**	4765	65AF
110.9	4342	4F23	**183.5**	4562	59E1			
134.4	43E8	5281						

(134.4Hz is the DCS end identification tone.)

Receiving and Decoding Selcall Tones

The CMX880 detects the Selcall tones that match the pre-programmed frequencies defined in the 'RX SELCALL TONES' words (B1.12 to B1.27) of the 'PROGRAMMING REGISTER' ($C8). The tone bandwidth and signal level threshold are set in the 'SELCALL TONE BW AND LEVEL' word of the 'PROGRAMMING REGISTER'. Table 3 lists the commonly used Selcall tones together with the values for programming the 'RX SELCALL TONES' words. This does not preclude other tones being programmed. More details for programming Selcall tones are provided in section 1.5.2.

Table 3 Selcall Tone Sets and Corresponding Rx Programming Codes

	EIA		EEA		CCIR	
Tone Address	Freq. (Hz)	Tone Code (hex)	Freq. (Hz)	Tone Code (hex)	Freq. (Hz)	Tone Code (hex)
0	600	4226	1981	4741	1981	4741
1	741	42A6	1124	4420	1124	4420
2	882	4340	1197	4461	1197	4461
3	1023	43C1	1275	44A2	1275	44A2
4	1164	4441	1358	4500	1358	4500
5	1305	44C2	1446	4542	1446	4542
6	1446	4542	1540	45A1	1540	45A1
7	1587	45C3	1640	4601	1640	4601
8	1728	4643	1747	4661	1747	4661
9	1869	46E0	1860	46C2	1860	46C2
A (10)	2151	47E1	1055	43E0	2400	48C1
B (11)	2435	48E2	930	4362	930	4362
C (12)	2010	4760	2247	4840	2247	4840
D (13)	2295	4861	991	43A1	991	43A1
E (14)	459	41A7	2110	47C0	2110	47C0
F (15)	NoTone	-	2400	48C1	1055	43E0

	ZVEI 1		ZVEI 2	
	Freq. (Hz)	Tone Code (hex)	Freq. (Hz)	Tone Code (hex)
0	2400	48C1	2400	48C1
1	1060	43E1	1060	43E1
2	1160	4441	1160	4441
3	1270	44A2	1270	44A2
4	1400	4521	1400	4521
5	1530	45A0	1530	45A0
6	1670	4620	1670	4620
7	1830	46A3	1830	46A3
8	2000	4760	2000	4760
9	2200	4802	2200	4802
A (10)	2800	4A41	885	4340
B (11)	810	42E6	810	42E6
C (12)	970	4383	740	42A6
D (13)	885	4340	680	4280
E (14)	2600	4981	970	4383
F (15)	680	4280	2600	4981

Selcall tones can be used to flag the start and end of a call. They may also occur during a call in which case the tone will be audible at the receiver. If enabled, an interrupt will be issued when a signal matching a valid Selcall tone is detected and when a present Selcall tone turns off (i.e. at the start and at the finish of each Selcall tone). It is up to the user/host µC to turn the audio path on and off at the appropriate times. Adjustable decoder bandwidths and threshold levels permit certainty and signal to noise performance to be traded when congestion or range limits the system performance.

The voice signal is derived from the received input signal by the band pass filtering shown in Figure 5.

Associated Control and Status
- Reset.
- Enable Selcall Tone Detection.
- Set decoder bandwidth.
- Set tone detection threshold level.
- Interrupt masks - Tone Detected, Lost Tone.
- Interrupt flag - Tone Detected, Lost Tone.
  Flags set on change of associated status and interrupt issued if appropriate mask bit is set.
- Interrupt status - Tone detected, Lost Tone.

Receiving and Decoding DCS Codes

DCS Code is in NRZ format and transmitted at 134.4 ±0.4bps. The CMX880 is able to decode either of the two DCS modulation modes defined by TIA/EIA-603 and described in Table 4. The CMX880 can detect a valid DCS Code quickly enough to avoid losing the beginning of voice transmissions.

Table 4 DCS Modulation Modes

Modulation Type	Data Bit	Frequency Change
A	0 1	Minus frequency shift Plus frequency shift
B	0 1	Plus frequency shift Minus frequency shift

The CMX 880 detects the DCS code that matches the pre-programmed code defined in the 'DCS CODE (UPPER)/(LOWER)' words (B2.2, B2.3) in the 'PROGRAMMING REGISTER' ($C8).

To detect the pre-programmed DCS code the signal is low pass filtered to suppress all but the sub-audio band. Further equalisation filtering, signal slicing and level detection are done to extract the code being received. The extracted code is then matched with the pre-programmed 23 or 24-bit DCS code to be recognised, in the order least significant first through to most significant DCS code bit last. Table 5 shows valid 23-bit DCS codes and the programming data needed to select the desired code. This does not preclude other codes being programmed. Recognition of a valid DCS Code will be flagged if the decode is successful (3 or fewer errors). A failure to decode is indicated by a "0" flag. This flag is updated after every 4 bits of the incoming signal is decoded.

Once a valid DCS Code has been detected, the digitised voice band data is passed, either to the µC/DSP or to the AUDIO loudspeaker output. The destination is set by the µC. The voice band is extracted from the received input signal by band pass filtering; see Figure 5.

The end of a DCS transmission is indicated by a continuous 134.4 ±0.5Hz tone for 150-200ms. In order to detect the DCS turn-off code, the CTCSS Tone Decoder should also be enabled and programmed with the corresponding value. Once detected this will cause a CTCSS tone decode interrupt; the receiver audio output should then be muted by the µC.

More details for programming DCS Codes are provided in section 1.5.2.

Associated Control and Status

- Reset.
- Enable DCS (Modulation type A) Code detection [0 -> -ve freq shift; 1 -> +ve freq shift].
- Enable DCS (Modulation type B) Code detection [0 -> +ve freq shift; 1 -> -ve freq shift].
- Select 23 or 24-bit DCS Code.
- DCS Code to be recognised.
- Interrupt mask - DCS Code Detected.
- Interrupt flag - DCS Code Detected (≤3 bit errors). Flag set on change of associated status and interrupt issued if mask bit is set.
- Interrupt status - DCS Code detected.

Table 5 DCS 23 Bit Codes

DCS Code	DCS CODE (UPPER) (hex)	DCS CODE (LOWER) (hex)
023	5763	4813
025	56B7	4815
026	565D	4816
031	551F	4819
032	55F5	481A
043	55B6	4823
047	50FD	4827
051	57CA	4829
054	56F4	482C
065	55D1	4835
071	5679	4839
072	5693	483A
073	52E6	483B
074	5747	483C
114	535E	484C
115	572B	484D
116	57C1	484E
125	507B	4855
131	53D3	4859
132	5339	485A
134	52ED	485C
143	537A	4863
152	51EC	486A
155	544D	486D
156	54A7	486E
162	56BC	4872
165	531D	4875
172	505F	487A
174	518B	487C
205	56E9	4885
223	568E	4893
226	57B0	4896
243	545B	48A3
244	51FA	48A4
245	558F	48A5
251	5627	48A9
261	5177	48B1
263	55E8	48B3
265	543C	48B5
271	5794	48B9
306	50CF	48C6
311	538D	48C9

DCS Code	DCS CODE (UPPEr) (hex)	DCS CODE (LOWER) (hex)
315	56C6	48CD
331	523E	48D9
343	5297	48E3
346	53A9	48E6
351	50EB	48E9
364	5685	48F4
365	52F0	48F5
371	5158	48F9
411	5776	4909
412	579C	490A
413	53E9	490B
423	54B9	4913
431	56C5	4919
432	562F	491A
445	57B8	4925
464	527E	4934
465	560B	4935
466	56E1	4936
503	53C6	4943
506	52F8	4946
516	541B	494E
532	50E3	495A
546	519E	4966
565	50C7	4975
606	55D9	4986
612	5671	498A
624	50F5	4994
627	501F	4997
631	5728	4999
632	57C2	499A
654	54C3	49AC
662	5247	49B2
664	5393	49B4
703	522B	49C3
712	50BD	49CA
723	5398	49D3
731	51E4	49D9
732	510E	49DA
734	50DA	49DC
743	514D	49E3
754	520F	49EC

Receiving C4FM Signals

The CMX880 C4FM signalling scheme is intended to comply with the requirements of APCO 25 C4FM signalling, in accordance with:

- TSB102.BAAA, APCO-25 Recommended Common Air Interface;
- TSB102.CAAB, Digital C4FM/CQPSK Transceiver Performance Recommendations.

APCO 25 messages, whether data or digitised speech, are formed into packets comprising frame sync (FS), network ID (NID), header information and further coded data fields. The format of the data is dependent on the type of message, as identified by the header.

The over-air signal is transmitted as C4FM ('Phase 1' implementation, 12.5kHz channel spacing) or CQPSK ('Phase 2', 6.25kHz channel spacing). In either case the output of a receiving device's FM discriminator is a 4-level 4800 symbol/s signal. The 4-level signal is Raised Cosine (RC) and shape filtered before transmission, as shown in Figure 8.

The CMX880 device extracts the symbols and clock and detects the 24-symbol FS pattern from the demodulated C4FM/CQPSK signal. It does not perform error correction or extraction of the remaining data packet fields, etc. These tasks must be done by an external DSP.

Symbol data is transferred over the Fast Serial Bus to the external DSP. The DSP must be capable of processing the symbol data at the incoming symbol rate of 4800 symbols/s.

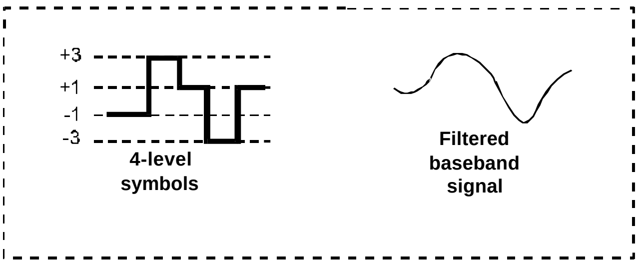


Figure 8 The 4-Level Symbols, Unfiltered and RC Filtered

The demodulated signal (without noise) at the receiver corresponds to that shown as the filtered waveform of Figure 8. The signal is 'integrate and dump' filtered to reject HF noise and to equalise the signal to a form suitable for extracting the 4-level symbols. The filter has a linear phase, sinc(π.f/4800) response up to 2880Hz. The response is shown in Figure 9. The filter is followed by a stochastic gradient clock recovery device, which is capable of extracting the symbol clock from a received signal that has up to ±40ppm deviation from the local symbol rate clock. This allows for ±10ppm symbol rate accuracy of the transmitter and ±10ppm accuracy of the local clock, plus a margin of ±20ppm for radio channel effects.

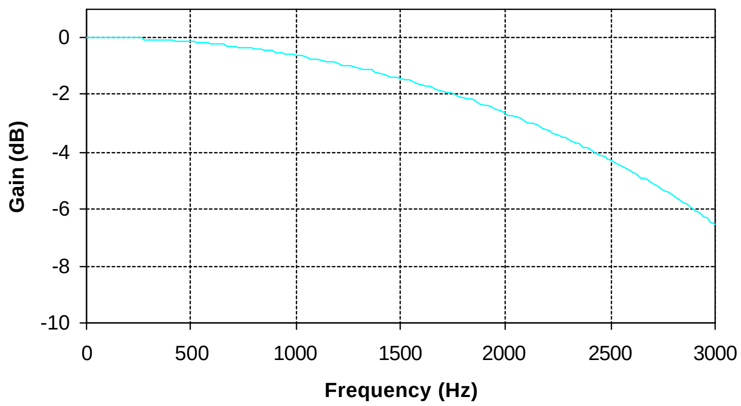


Figure 9 Receiver Filter Frequency Response

Rx Data Level, Frame Sync and Clock Extraction

The C4FM receiver function takes the 24kS/s output from the ADC, performs sin(x)/x filtering and searches for the Frame Sync pattern shown in Table 6.

Table 6 Frame Sync Pattern

<table>
<tr><td colspan="12">1st symbol sent</td><td colspan="12">last symbol sent</td></tr>
<tr><td>+3</td><td>+3</td><td>+3</td><td>+3</td><td>+3</td><td>-3</td><td>+3</td><td>+3</td><td>-3</td><td>-3</td><td>+3</td><td>+3</td><td>-3</td><td>-3</td><td>-3</td><td>-3</td><td>+3</td><td>-3</td><td>+3</td><td>-3</td><td>-3</td><td>-3</td><td>-3</td><td>-3</td></tr>
</table>

The frame sync pattern contains only +3 and -3 symbols, so FS is detected by cross-correlation of NRZ patterns. The Frame Sync detection level is set by writing an appropriate value in the ‘RX C4FM FRAME SYNC THRESHOLD’ register to set the cross-correlation detection threshold. The frame sync detection tolerance can also be set in terms of bit error allowance; see the Associated Control and Status sub-section of the C4FM section. The combination of threshold level and bit error limit, provide good FS recognition integrity in high noise.

Initial acquisition of symbol levels and symbol clock timing are derived automatically from the received Frame Sync. Subsequent symbol clock tracking is done by a stochastic gradient recovery technique.

Once symbol levels and clock timing have been acquired, symbols are extracted and converted to a normalised symbol representation. Extracted symbol levels are translated into an 8-bit code comprising 2 symbol code bits and 6 ‘quality’ bits encoded as a 2’s complement number. The quality bits represent the deviation of the sampled symbol level from the acquired optimum symbol levels. The optimum symbol levels are initially derived from levels extracted during the frame sync detection period, then updated in accordance with the selected level tracking mode. The closer the value is to zero, the better the indicated signal decode quality. Two symbols are formed into a 16-bit word for transfer over the FSB to the external DSP. The format of the symbol encoding and data transfer word is shown in Table 7.

The CMX880 does not perform any other symbol decoding, data packet processing or forward error correction (FEC) etc. If required, these operations must be done by an external DSP.

Table 7 Symbol Word Encoding

2 symbols per word:

<table>
<tr><td></td><td>msb</td><td colspan="14"></td><td>lsb</td></tr>
<tr><td>Bits:</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Symbol</td><td colspan="8">1 (previous symbol)</td><td colspan="8">0 (most recently received symbol)</td></tr>
<tr><td></td><td>Bit 7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>Bit 0</td><td>Bit 7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>Bit 0</td></tr>
<tr><td></td><td colspan="2">Symbol code</td><td colspan="6">Symbol level quality
(2’s complement format)</td><td colspan="2">Symbol code</td><td colspan="6">Symbol level quality
(2’s complement format)</td></tr>
</table>

2-bit symbol encoding:

Bit 7	Bit 6	Symbol	Freq. deviation
0	1	+3	+1.8kHz
0	0	+1	+0.6kHz
1	0	-1	-0.6kHz
1	1	-3	-1.8kHz

Decoded Voice Signal Processing for APCO-25

If the C4FM signal being received is digitally encoded voice, this must be decoded by the external DSP. The decoded voice signal can be routed to the AUDIO output of the CMX880 to drive a loudspeaker. The decoded 16-bit voice data word is transferred to the CMX880 from the DSP over the FSB or “C-BUS” at 8000words/s. The voice data is filtered and interpolated to 24kS/s, then D-to-A converted to drive the audio output port. The filter fits the output filter mask recommended in ‘Speech Input/Output Requirements’ of the ‘APCO Project 25 Vocoder Description, Standard IS102BABA, 1/11/95’, shown in Figure 10.

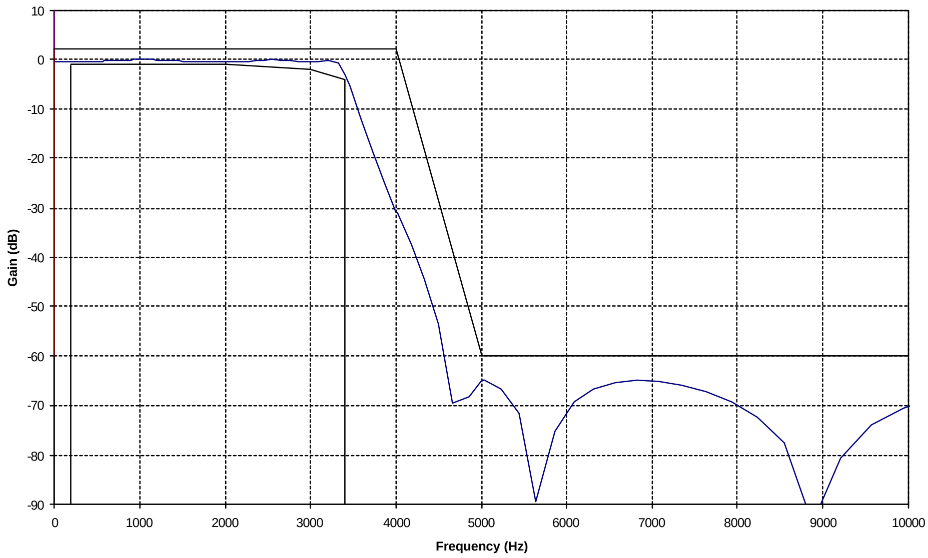


Figure 10 Filter Characteristics for Decoded C4FM Voice Signals

Data Quality

The CMX880 decodes C4FM signals at each symbol sample point. The decoded value corresponds to the valid symbol level that the sampled signal level is closest to. ‘Loss of data’ can be associated with the number of decoded symbol errors, or some other measure of data quality, exceeding a threshold, which may be detected by the external [DSP] error detection and correction function. ‘Loss of data’ may also occur if the RSSI falls below the minimum signal strength threshold; to detect this the appropriate RSSI interrupt flag must be enabled.

Associated Control and Status

- Reset.
- Enable C4FM signal reception.
- Received data.
- Data quality.
- Interrupt masks - C4FM data word present; frame sync detected; FS tolerance data ready.
- Interrupt flag - C4FM data word present; frame sync detected; FS tolerance data ready. Flags set on change of associated status and interrupt issued if appropriate mask bit is set.
- Interrupt status - C4FM data word present; frame sync detected; FS tolerance and bit error count.

- Frame Sync Threshold / Tolerance
  The frame sync threshold defines the level that the cross-correlation of signal with the frame sync pattern must exceed before the CMX880 will detect a FS. The FS Cross-correlation Peak value can be read by "C-BUS" command.
  The frame sync tolerance code defines the maximum number of mismatches allowed during a search for the Frame Sync pattern. The FS Mismatch count can be read by "C-BUS" command.
  A single 'mismatch' is defined as the difference between two adjacent symbol levels, thus if the symbol '+1' were expected, then received symbol values of '+3' and '-1' would count as 1 mismatch and a received symbol value of '-3' would count as 2 mismatches.
- Select Clock Tracking Mode
  allows the µC to change the symbol clock tracking mode if it perceives the Data Quality as deteriorating. Modes: (1) Stochastic Gradient Clock Tracking Algorithm; or (2) Fixed Clock.
- Select Level Tracking Mode
  allows the µC to the change the symbol level tracking mode if it perceives the Data Quality to be deteriorating. Modes: (1) Fast tracking; (2) Slow Tracking; (3) Partial Response Tracking; or (4) Fixed Level.

Receiving FFSK Signals

The device can decode incoming FFSK signals at either 1200 or 2400 baud data transfer rates. It can achieve this by deriving the baud rate from the received signal, or a control word may set the baud rate and the device only responds to signals operating at that rate. The form of FFSK signals for these baud rates, excluding noise, is shown in Figure 11.

The received signal is filtered and data is extracted. A PLL is used to extract the clock from the recovered serial data stream. The recovered data is grouped into 16-bit words and an interrupt issued to indicate received data is ready. Data can be transferred over the "C-BUS" or the FSB, controlled by µC instructions. If this data is not read within 16 bit periods it will be overwritten. The FFSK clock is not directly output on either external bus. It is up to the user to ensure that the data is transferred at an adequate rate following data ready being flagged.

The extracted data is compared with the up to 3 pre-programmed frame sync patterns, SYNC, SYNT and SYND. The SYNC and SYND patterns are user programmable. SYNT is the bit complement of SYNC. SYNC and SYND are preset to $C4D7 following a reset. The user can individually enable any combination of the 3 patterns. An interrupt will be flagged when a frame sync pattern is detected.

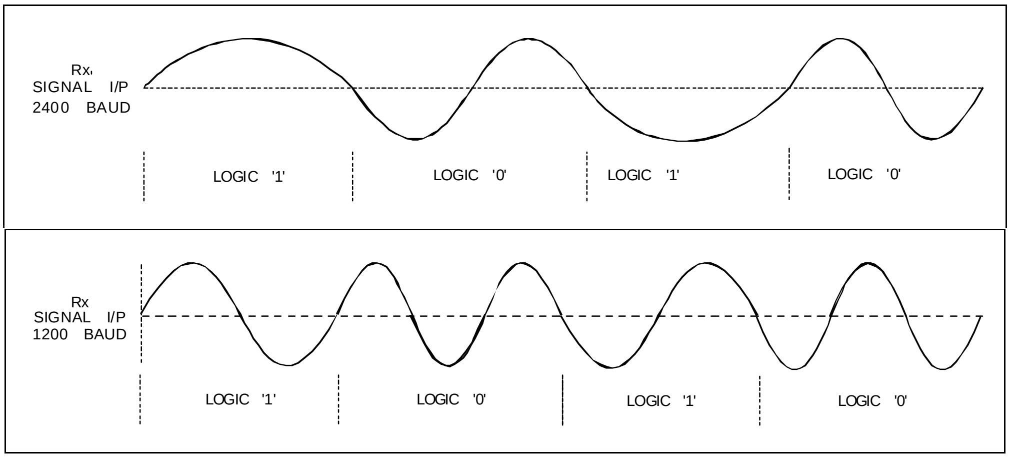


Figure 11 Modulating Waveforms for 1200 and 2400 Baud FFSK Signals

Table 8 shows the combinations of frequencies and number of cycles to represent 'bits' of data, for both baud rates.

Table 8 Data Frequencies For Each Baud Rate

Baud Rate	Data	Frequency	Number of Cycles
1200 baud	1	1200Hz	one
	0	1800Hz	one and a half
2400 baud	1	1200Hz	half
	0	2400Hz	one

FFSK/MSK may be transmitted in conjunction with a CTCSS or DCS sub-audio component. The device will handle the sub-audio signals as already described. If a sub-audio signal turns off during reception of FFSK/MSK, it is up to the µC to turn off the FFSK/MSK decoding. The device will continue receiving and processing the incoming signal until commanded otherwise by the µC.

Associated Control and Status

- Reset.
- Enable FFSK signal reception.
- Select baud rate: 1200 or 2400. Both rates can be enabled at the same time. The CMX880 will identify the baud rate from the received signal.
- Set access port, "C-BUS" or FSB.
- Select frame sync patterns to be recognised (SYNC, SYNT and SYND); set SYND pattern.

- Interrupt masks - FFSK data word present; frame sync detected.
- Interrupt flag - FFSK data; frame sync. Flags set on change of associated status and interrupt issued if appropriate mask bit is set.
- Interrupt status - FFSK data; frame sync.

1.5.1.4 Transmit Mode

The device only operates in half duplex, so when the device is in transmit mode the receive path (FM disc and audio output amplifiers) should be disabled, and can be powered down, by the host µC.

Two modulator outputs with independently programmable gains are provided to facilitate two-point FM modulation. If this is not used, either of the modulator outputs can be disabled to conserve power.

The output of the Delta-Sigma DACs can be switched between either the audio output or the RF modulator outputs. To avoid erroneous transmission of out of band frequencies when changing the output path destination, the DAC outputs are ramped to the quiescent modulator output level, V_{BIAS} before switching. Similarly, when starting a transmission, the transmitted signal strength is ramped up from the quiescent V_{BIAS} level and when ending a transmission the transmitted signal strength is ramped down to the quiescent V_{BIAS} level. The ramp rates are set by "C-BUS" command. When the modulator outputs are disabled, their outputs will be at the V_{BIAS} quiescent level. When the modulator output drivers are powered down, their outputs will be floating, so the RF modulator will need to be turned off.

The CMX880 supports various transmit options operating concurrently. These are shown in Table 9.

Table 9 Concurrent Tx Modes Supported by the CMX880

Analogue Channel Modes		**Digital Channel Modes**	
Sub-Audio	**Voice band**		
	Voice	C4FM	(Data)
CTCSS		C4FM	(Voice from MIC input)
CTCSS +	Voice	CQPSK	(Data)
CTCSS +	Selcall	CQPSK	(Voice from MIC input)
CTCSS +	DTMF		
CTCSS +	FFSK/MSK		
DCS			
DCS +	Voice		
DCS +	Selcall		
DCS +	DTMF		
DCS +	FFSK/MSK		
	Selcall		
	DTMF		
	FFSK/MSK		

The following paragraphs describe the types of signal transmission modes the CMX880 can perform.

Processing Voice Data For Transmitting On Analogue Channels

One of two microphone inputs can be selected as the voice input source. The selected microphone input signal is A-to-D converted and band pass filtered as described below. The digitised signal can then be routed directly to the D-to-A converter and modulator outputs for analogue signal transmission, or over the "C-BUS" to an external processor for further encoding.

If the voice signal from the microphone input is routed over the "C-BUS", the µC must read it within 125µs of notification (interrupt) of availability of the data sample to maintain throughput at 8000S/s, otherwise the data will be overwritten. Similarly, voice data must be written back to the CMX880 at the 8000S/s rate.

A programmable gain stage in the microphone input path facilitates µC controlled VOGAD capability.

Two analogue mode audio filters are provided, one for 25kHz channel spacing and the other for 12.5kHz channel spacing. These are designed for use in ETS-300-086 and/or TIA/EIA-603 compliant applications. Both filters attenuate sub-audio frequencies below 250Hz by more than 33dB wrt the signal level at 1kHz.

The filter characteristics of the 25kHz channel filter fits the filter template shown in Figure 12. This filter facilitates implementation of systems compliant with ETS-300-086 (25kHz channel spacing).

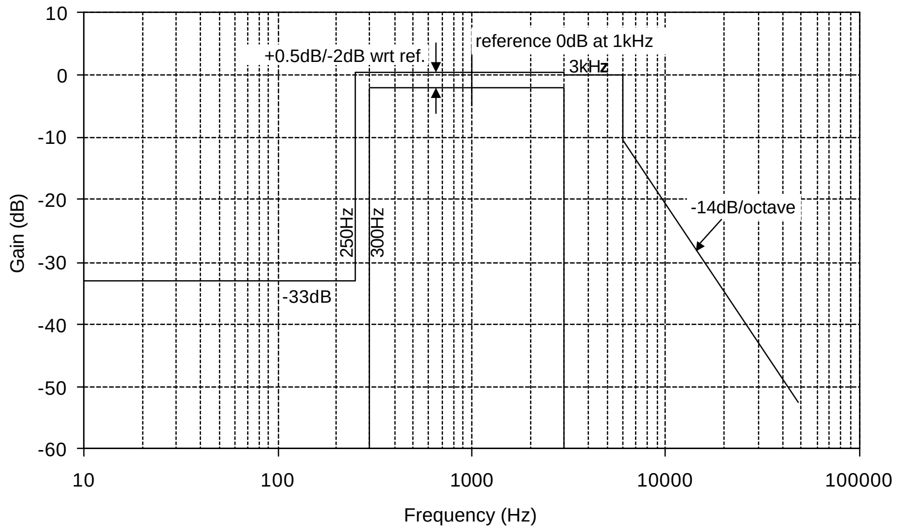


Figure 12 25kHz Channel Audio Filter Response Template

The filter characteristics of the 12.5kHz channel filter fits the filter template shown in Figure 13 (solid outline). This filter facilitates implementation of systems compliant with ETS-300-086 (12.5kHz channel spacing) and TIA/EIA-603 'A' and 'B' bands. To achieve attenuation above 3kHz of better than –100dB/decade for TIA/EIA-603 'C' bands (dashed outline), additional external circuitry is required, such as suggested in section 1.4.

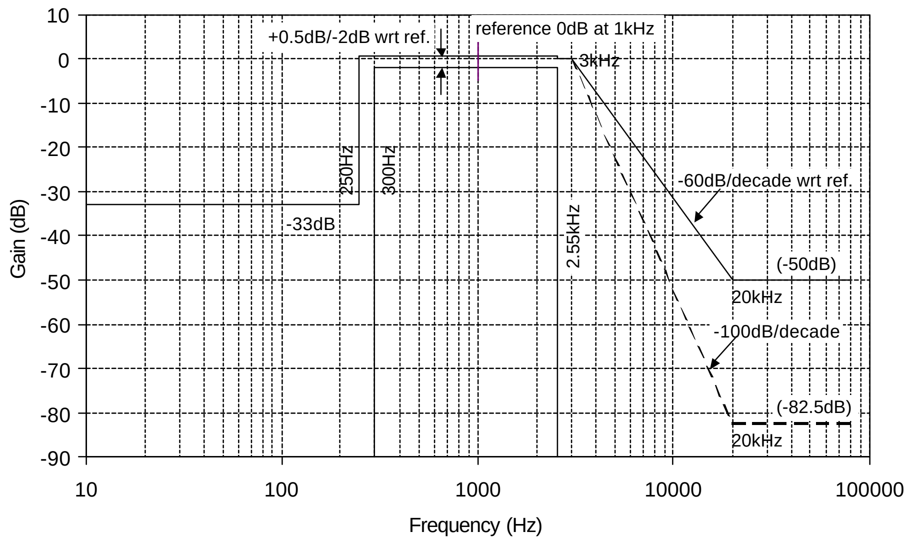


Figure 13 12.5kHz Channel Audio Filter Response Template

The CMX880 provides selectable pre-emphasis filtering of +6dB per octave from 300Hz to 3000Hz, matching the template shown in Figure 14.

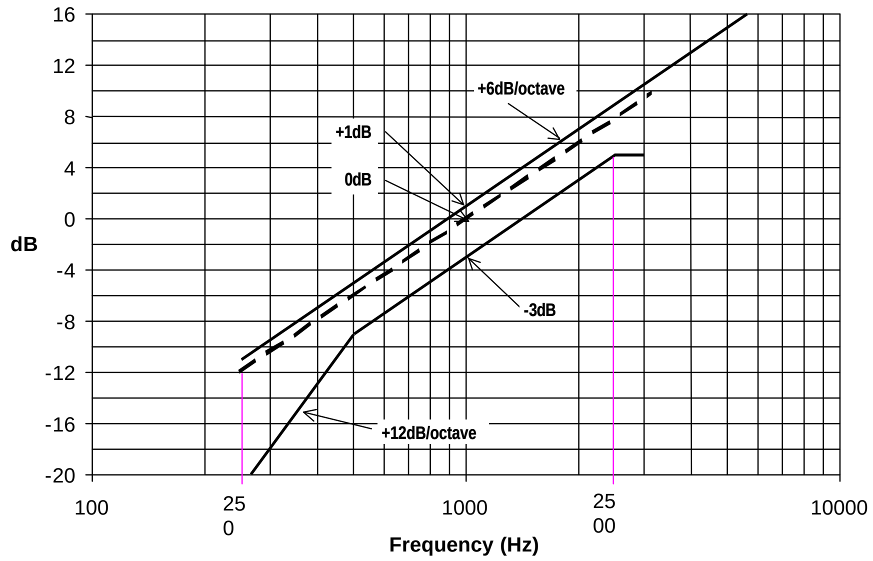


Figure 14 Audio Frequency Pre-emphasis Template

Transmitting Signals On Analogue Channels

Modulator Output Routing:

The sub-audio component can be combined with the voice band signal and this composite signal routed to both MOD_1 and MOD_2 outputs, or the sub-audio and voice band signal can be output separately (sub-audio to MOD_2 and voice band to MOD_1), in accordance with the settings of the 'ANALOGUE OUTPUT PATH CONFIGURATION' register ($B1).

CTCSS Tone:

The sub-audio CTCSS tone generated is defined by the 'TX CTCSS TONE' word (B2.1) in the 'PROGRAMMING REGISTER'' ($C8). Table 10 lists the commonly used CTCSS tones and the corresponding values for programming the 'TX CTCSS TONE' word. This does not preclude other tones being programmed.

Table 10 CTCSS TX Tone Programming

Freq. (Hz)	Tone Code (hex)	Freq. (Hz)	Tone Code (hex)	Freq. (Hz)	Tone Code (hex)
67.0	C224	114.8	C3AC	186.2	C5F5
69.3	C237	118.8	C3CD	189.9	C613
71.9	C24C	123.0	C3EF	192.8	C62B
74.4	C261	127.3	C412	196.6	C64A
77.0	C276	131.8	C437	199.5	C662
79.7	C28C	136.5	C45E	203.5	C683
82.5	C2A3	141.3	C485	206.5	C69B
85.4	C2BB	146.2	C4AD	210.7	C6BE
88.5	C2D4	151.4	C4D8	218.1	C6FA
91.5	C2ED	156.7	C503	225.7	C738
94.8	C308	159.8	C51D	229.1	C754
97.4	C31D	162.2	C530	233.6	C779
100.0	C333	167.9	C55F	241.8	C7BC
103.5	C34F	173.8	C58F	250.3	C802
107.2	C36E	179.9	C5C1	254.1	C821
110.9	C38C	183.5	C5DF		
134.4	C44D				

(134.4Hz is the DCS end identification tone.)

DCS Code:

A 23 or 24-bit sub-audio DCS Code can be generated, as defined by the 'DCS Code' words (B2.2, B2.3) of the 'PROGRAMMING REGISTER' ($C8); the same DCS Code register is used for Rx detection and transmission. The DCS Code is NRZ encoded at 134.4±0.4bits/s, low pass filtered and added to the digitised voice signal, prior to passing the signal to the interpolation and Delta-Sigma DAC and modulator output stages. The valid 23-bit DCS codes and the corresponding settings for the DCS Code Register are shown in Table 5. This does not preclude other codes being programmed. The least significant bit of the DCS code is transmitted first and the most significant bit is transmitted last. The CMX880 is able to encode and transmit either of the two DCS modulation modes defined by TIA/EIA-603 and described in Table 4.

To signal the end of the DCS transmission, the µC should set the CTCSS Tx tone register to 134.4Hz, disable DCS code transmit and turn on the CTCSS tone transmit for 150ms to 200ms. The CMX880 has specific capability to ensure a smooth transmission from DCS code to CTCSS tone so that the 'turn off' tone is issued in phase with the last DCS code bit transmitted.

Selcall Tone:
The Selcall tone to be generated is defined by the 'TX SELCALL TONE' register ($CB). The tone level is set by the 'Tone Level' field of the 'DTMF TX AND TONE LEVEL' register ($CD). The Selcall tone must be transmitted on its own, so the user/host µC must disable the voice path prior to initiating transmission of a Selcall tone, and restore the voice path after the Selcall tone transmission is complete. Table 11 shows valid Selcall tones for commonly used Selcall tone sets, together with the values for programming the 'TX SELCALL TONE' register. This does not preclude other tones being programmed.

Table 11 Selcall Tone Sets and Corresponding Tx Programming Codes

	EIA		EEA		CCIR	
Tone Address	**Freq. (Hz)**	**Tone Code (hex)**	**Freq. (Hz)**	**Tone Code (hex)**	**Freq. (Hz)**	**Tone Code (hex)**
0	600	C666	1981	D521	1981	D521
1	741	C7E7	1124	CBFD	1124	CBFD
2	882	C968	1197	CCC4	1197	CCC4
3	1023	CAE9	1275	CD99	1275	CD99
4	1164	CC6A	1358	CE7C	1358	CE7C
5	1305	CDEB	1446	CF6C	1446	CF6C
6	1446	CF6C	1540	D06D	1540	D06D
7	1587	D0ED	1640	D17E	1640	D17E
8	1728	D26E	1747	D2A2	1747	D2A2
9	1869	D3EF	1860	D3D6	1860	D3D6
A (10)	2151	D6F1	1055	CB40	2400	D999
B (11)	2435	D9F9	930	C9EB	930	C9EB
C (12)	2010	D570	2247	D7F7	2247	D7F7
D (13)	2295	D87A	991	CA92	991	CA92
E (14)	459	C4E5	2110	D681	2110	D681
F (15)	NoTone	-	2400	D999	1055	CB40

	ZVEI 1		ZVEI 2	
Tone Address	**Freq. (Hz)**	**Tone Code (hex)**	**Freq. (Hz)**	**Tone Code (hex)**
0	2400	D999	2400	D999
1	1060	CB4E	1060	CB4E
2	1160	CC5F	1160	CC5F
3	1270	CD8B	1270	CD8B
4	1400	CEEE	1400	CEEE
5	1530	D051	1530	D051
6	1670	D1D0	1670	D1D0
7	1830	D385	1830	D385
8	2000	D555	2000	D555
9	2200	D777	2200	D777
A (10)	2800	DDDD	885	C970
B (11)	810	C8A3	810	C8A3
C (12)	970	CA58	740	C7E4
D (13)	885	C970	680	C740
E (14)	2600	DBBB	970	CA58
F (15)	680	C740	2600	DBBB

DTMF Tones:
The DTMF tone pairs to be generated and tone levels are defined by the 'DTMF TX AND TONE LEVEL' register ($CD). The DTMF tones must be transmitted on their own, so if a voice signal is being transmitted, this must be disabled for the duration of the DTMF tones transmission. The user/host µC must disable the voice path prior to initiating transmission of the DTMF tones, and restore the voice path after the DTMF transmission is complete. Table 12 shows valid DTMF tone pairs, together with the values for programming the 'Tone Pair' field of the 'DTMF TX AND TONE LEVEL' register. No other tone pair combinations are programmable.

Table 12 DTMF Tone Pairs and Corresponding Tx Programming Codes

Tone Pair Programming Code (Hex)	Key Pad Position	Low Tone	High Tone
1	1	697Hz	1209Hz
2	2	697Hz	1336Hz
3	3	697Hz	1477Hz
4	4	770Hz	1209Hz
5	5	770Hz	1336Hz
6	6	770Hz	1477Hz
7	7	852Hz	1209Hz
8	8	852Hz	1336Hz
9	9	852Hz	1477Hz
A	0	941Hz	1336Hz
B	*	941Hz	1209Hz
C	#	941Hz	1477Hz
D	A	697Hz	1633Hz
E	B	770Hz	1633Hz
F	C	852Hz	1633Hz
0	D	941Hz	1633Hz

Transmitting C4FM and CQPSK Signals

The CMX880 generates filtered symbol levels at the 4800 symbols/s symbol rate in accordance with the APCO 25 Recommended Common Air Interface, TSB102.BAAA. The frame sync pattern insertion, forward error correction and other data encoding and message formatting, must be performed by the external DSP, before symbols are transferred to the CMX880.

The symbol codes of the symbols to be transmitted are transferred to the CMX880 over the FSB. The format of the symbol word transferred over the FSB and symbol levels are defined in Table 13. A single 16-bit word buffer enables 8 symbol codes (2 octets) to be transferred from the DSP to the CMX880 by a single FSB transaction. The DSP must be able to provide successive symbol words at 600words/s to ensure the symbol rate of 4800 symbols/s is maintained.

Table 13 C4FM Symbol Word Encoding

	msb															lsb
Bits:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	7 (first)		6		5		4		3		2		1		0 (last)	
	Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0

2-bit symbol encoding

Bit 1	Bit 0	Symbol	C4FM Freq. Deviation	CQPSK Phase
0	1	+3	+1.8kHz	+135 deg.
0	0	+1	+0.6kHz	+45 deg.
1	0	-1	-0.6kHz	-45 deg.
1	1	-3	-1.8kHz	-135 deg.

For C4FM transmitted signals the symbol levels are decoded and passed as scaled impulses to the input of a Raised Cosine, H(f) and Shaping, P(f) filter, D-to-A converted, then output to the FM Modulator as shown in Figure 15. The symbol levels need to be defined prior to the CMX880 transmitting a C4FM signal. The symbol levels are defined by writing the +1 unit symbol level into the 'TX C4FM/CQPSK UNIT LEVEL' word of the 'PROGRAMMING REGISTER' ($C8). The CMX880 will formulate the other two symbol levels from this data before transmission.

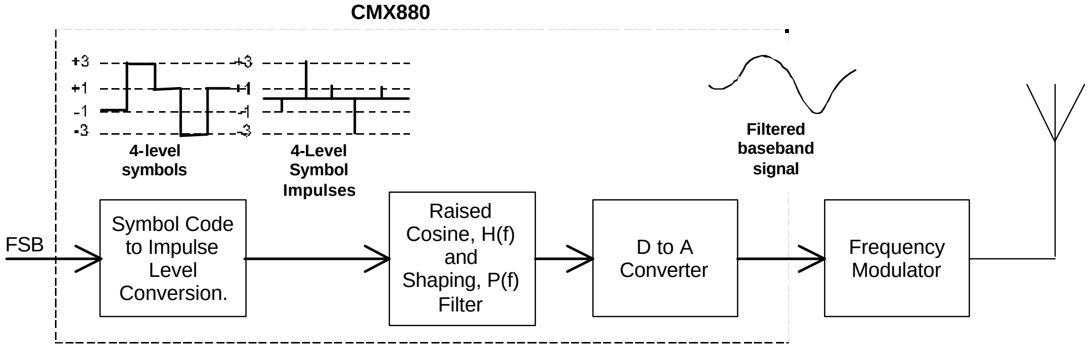


Figure 15 C4FM Transmitter Processing Path

The RC filter transfer characteristic has a flat group delay over the pass band for |f|<2880Hz, with a magnitude response of approximately:

$|H(f)| = 1$ for $|f|<1920$Hz;
$|H(f)| = 0.5 + 0.5\cos(2\pi f/1920)$ for $1920\text{Hz}<|f|<2880$Hz;
$|H(f)| = 0$ for $|f|>2880$Hz.

The shaping filter transfer characteristic has a flat group delay over the pass band for |f|<2880Hz, with a magnitude response of approximately:

$$|P(f)| = (\pi f/4800) / \sin(\pi f/4800) \qquad \text{for } |f|<2880\text{Hz}.$$

For CQPSK transmitted signals the symbols are decoded into separate I and Q levels in accordance with Table 14. The I and Q signals are Raised Cosine, H(f) filtered, D-to-A converted and output to their respective modulator output ports, I to MOD_1 and Q to MOD_2, as shown in Figure 16. The symbol decoder includes a state memory that is used in conjunction with the symbol code to select the I and Q levels. The maximum output range, corresponding to the levels of +1 and -1 of Table 14, need to be defined prior to the CMX880 transmitting a CQPSK signal. The default range is defined by writing the '+1' and '-1' limits by "C-BUS" command.

Table 14 I and Q Level Encoding

Current Phase State	Symbol Code Bits	Next Phase State	I Level	Q Level
0	00	1	+0.7071	+0.7071
0	01	3	-0.7071	+0.7071
0	11	5	-0.7071	-0.7071
0	10	7	+0.7071	-0.7071
1	00	2	0.0	+1.0
1	01	4	-1.0	0.0
1	11	6	0.0	-1.0
1	10	0	+1.0	0.0
2	00	3	-0.7071	+0.7071
2	01	5	-0.7071	-0.7071
2	11	7	+0.7071	-0.7071
2	10	1	+0.7071	+0.7071
3	00	4	-1.0	0.0
3	01	6	0.0	-1.0
3	11	0	+1.0	0.0
3	10	2	0.0	+1.0
4	00	5	-0.7071	-0.7071
4	01	7	+0.7071	-0.7071
4	11	1	+0.7071	+0.7071
4	10	3	-0.7071	+0.7071
5	00	6	0.0	-1.0
5	01	0	+1.0	0.0
5	11	2	0.0	+1.0
5	10	4	-1.0	0.0
6	00	7	+0.7071	-0.7071
6	01	1	+0.7071	+0.7071
6	11	3	-0.7071	+0.7071
6	10	5	-0.7071	-0.7071
7	00	0	+1.0	0.0
7	01	2	0.0	+1.0
7	11	4	-1.0	0.0
7	10	6	0.0	-1.0

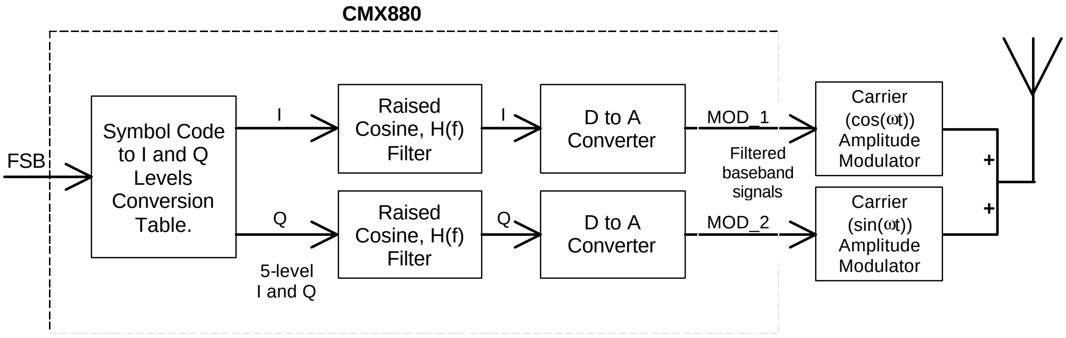


Figure 16 CQPSK Transmitter Processing Path

Processing Voice Signals for APCO-25

If the C4FM or CQPSK transmission is of digitally encoded voice, the voice signal from the microphone inputs is A-to-D converted, filtered and decimated to 8000S/s. The filter characteristics (including the filtering due to the recommended external components) meet the output filter template recommended in the 'Speech Input/Output Requirements', section 4 of the 'APCO Project 25 Vocoder Description, Standard IS102BABA, 1/11/95', shown in Figure 17, including the high pass filter $H(z) = (1 - z^{-1}) / (1 - 0.99 z^{-1})$ at 8000S/s, specified in 'Speech Analysis', section 5 of the same standard. Thus the voice data provided to the DSP over the FSB at 8000S/s corresponds to signal denoted as s(n) throughout that standard.

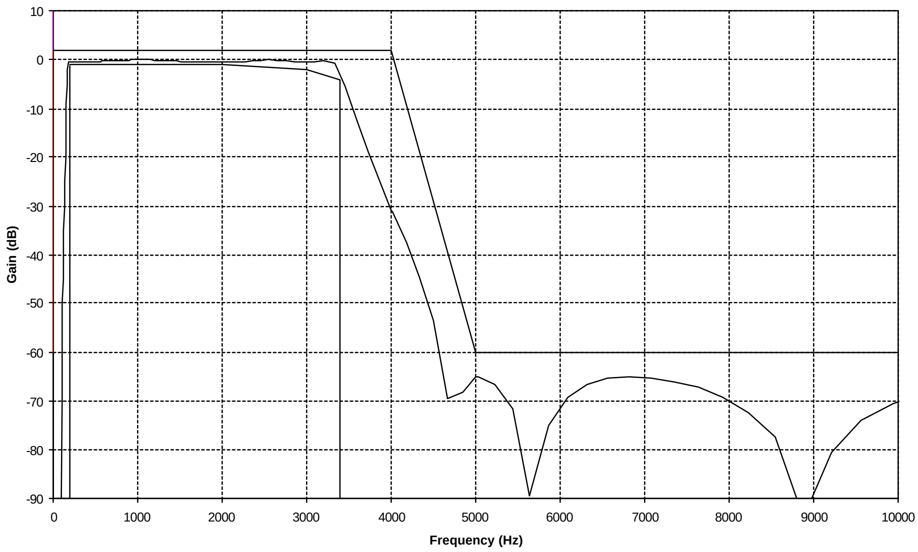


Figure 17 Voice Filter Template for C4FM and CQPSK Transmission

Transmitting FFSK/MSK Signals

The FFSK/MSK transmit operates continuously in a free-flow mode, so preamble and frame sync need to be programmed as normal data bytes. The CMX880 generates the data clock and converts the binary data stream into the appropriately phased frequencies, as shown in Table 8 and Figure 11. The binary data stream is taken from a 16-bit data buffer, most significant bit first. The next 16-bit data word must be provided over the "C-BUS" (or FSB) within 13.2ms (at 1200baud), or 6.6ms (at 2400baud) of notification (interrupt) of start of transmission of the previous data word, to ensure the selected baud rate is maintained.

The FFSK/MSK signal can be pre-emphasis filtered, by setting the required filter options in the 'TRANSMIT MODE CONTROL' register ($C1). FFSK/MSK modes can be transmitted in conjunction with a sub-audio tone or code.

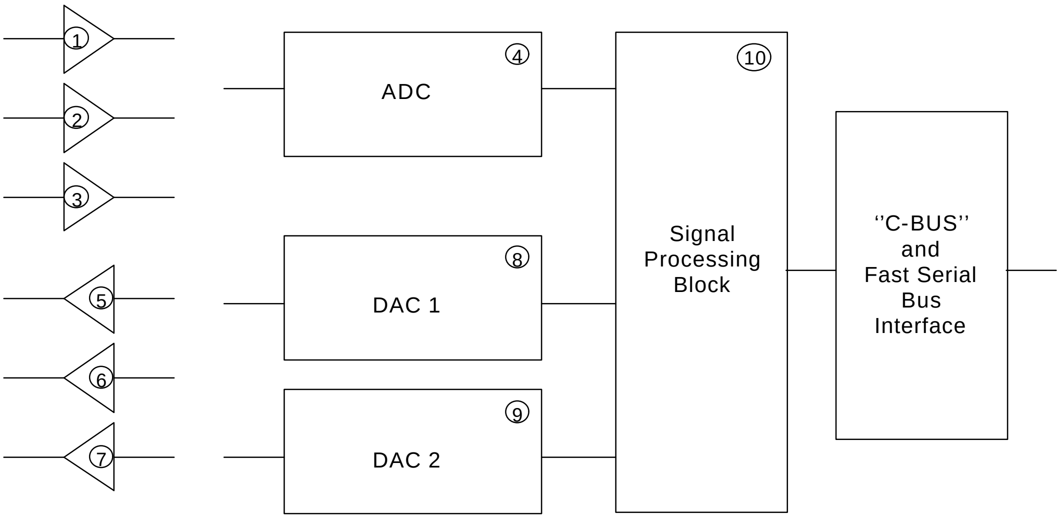
Transmit Mode Associated Control and Status

- Reset.
- Microphone select.
- Microphone gain.
- Microphone destination - internal; "C-BUS"; FSB.
- Modulators drive source -
  direct from microphone, (no external processing);
  from "C-BUS";
  from FSB.
- Transmit mode select:
  Voice band (select analogue channel width, 12.5kHz or 25kHz)
  Selcall
  DTMF
  C4FM - voice or data
  FFSK/MSK @ 1200 baud.
  FFSK/MSK @ 2400 baud.
- Signal levels.
- C4FM unit +1 symbol level value.
- Modulator and audio output amplifiers control - independent enable and gain control.
- Modulators and audio outputs - ramp all outputs to/from bias (1) prior to switching between outputs or (2) at beginning or end of a transmission.
- Define output ramp rate.
- Enable CTCSS Tone generation and add to voice band signal. ⎫ mutually exclusive modes.
- Enable DCS Code generation and add to voice band signal. ⎭
- Transmit Enable
- Transmit Data Buffer, 1x16-bit word.
- Data transmission start flag - indicates that new data is required within the time specified in Table 17 Maximum Data Transfer Latency, to ensure transmission continues at correct rate.
- Interrupt masks - Data word/buffer transmission complete, as above.
- Interrupt flag - Data word/buffer transmission complete. Flags set on change of associated status and interrupt issued if appropriate mask bit is set.
- Interrupt status - Data word/buffer transmission complete

1.5.1.5 Configuration Options

The CMX880 is designed to be extremely versatile, with extensive control of the configuration of signal/data paths is available to the host µC.

Following a reset command, the device is placed into power-save mode, with only the clock/xtal circuit and the "C-BUS" interface active. The various functional blocks that can be individually placed into power save/standby modes are shown in Figure 18. Valid receive and transmit signal/data path configurations that can be selected are shown in Table 15. The options for configuring signal paths, block power-save and gains are shown in Table 16.



1	Mic 1 input amp	6	Mod 1 output amp
2	Mic 2 input amp	7	Mod 2 output amp
3	FM discriminator input amp	8	Sigma Delta DAC 1
4	Sigma Delta ADC	9	Sigma Delta DAC 2
5	Audio output amp	10	Signal Processing block

Figure 18 Power-Save Blocks

Table 15 Receive and Transmit Path Configurations.

Receive Paths					
From		To	From		To
FM_DISC	→	"C-BUS"	"C-BUS"	→	AUDIO
FM_DISC	→	FSB	FSB	→	AUDIO
FM_DISC	→	Internal	Internal	→	AUDIO
OFF			OFF		

Transmit Paths					
From		To	From		To
MIC_1/2	→	"C-BUS"	"C-BUS"	→	MOD_1/2
MIC_1/2	→	FSB	FSB	→	MOD_1/2
MIC_1/2	→	Internal	Internal	→	MOD_1/2
OFF			OFF		

Table 16 Gain, Path Selection And Power Save Options

Input Selection	1. All inputs off (power-saved). 2. MIC_1 (all other inputs power-saved). 3. MIC_2 (all other inputs power-saved). 4. FM_DISC (all other inputs power-saved).
Delta-Sigma ADC Control	1. Enable ADC (power saved when disabled). 2. ADC input gain.
Delta-Sigma DAC Control	1. Enable DAC (power-saved when disabled).
Output Amplifier Controls and Selection	1. Enable Audio output (power-saved when disabled) + gain control. 2. Enable MOD_1 output (power-saved when disabled) + gain control. 3. Enable MOD_2 output (power-saved when disabled) + gain control. 4. Set up ramp rate for switching between outputs or starting/ending transmissions. MOD_1 and MOD_2 outputs can be selected individually or both together. Audio and modulator outputs cannot be selected at the same time, so if the Audio output is enabled, the output is routed to it, irrespective of the Modulator selection state. Thus to minimise power, the Modulators should be disabled by the user when the Audio output is enabled. Before switching from Modulator to Audio output, or powering down the Modulator outputs, the Modulator signal is ramped to V_{BIAS}. Before switching from Audio output to Modulator output, the Audio output level is ramped to V_{BIAS}. Before the Audio output is powered down, the Audio output level is ramped down to V_{BIAS} to avoid audible transient noise. On power down, the outputs become high impedance (floating).
Signal Processing (SP) Block Control	The power save should only occur when the SP Block has reached a suitable stage in whatever operation it might be performing, so disabling of the clock must wait until the SP Block signals that it is in a quiescent state. No data or register status will be lost by disabling the clock. If the ADC and DAC are both in power-save mode, the SP Block will have nothing to do and can therefore be placed in power-save mode by disabling its local clock source.
Input Signal Destination	1. OFF. 2. Digitised signal data to “C-BUS”. 3. Digitised signal data to FSB. 4. Digitised signal data to output signal path..
Output Signal Source	1. OFF. 2. Digitised signal data from “C-BUS”. 3. Digitised signal data from FSB. 4. Digitised signal data from input signal path.
TEST ONLY MODES	RESERVED MODES NOT AVAILABLE FOR CUSTOMER USE

1.5.1.6 "C-BUS" Operation

Instructions, status and data are transferred between the CMX880 and the µC over the "C-BUS". The "C-BUS" protocol, shown in Figure 19, complies with CML's "C-BUS" Hardware Interface specification. Instruction and data transfers to and from the CMX880 consist of an Address/Command (A/C) byte followed by either:

(i) a further instruction,
(ii) 1 or 2 bytes of data (write) or
(iii) 1 or 2 bytes of status or received data reply (read).

The number of data bytes following an A/C byte is dependent on the value of the A/C byte. The most significant bit of the address or data are sent first. The "C-BUS" SERIAL_CLOCK input to the CMX880 originates from the µC.

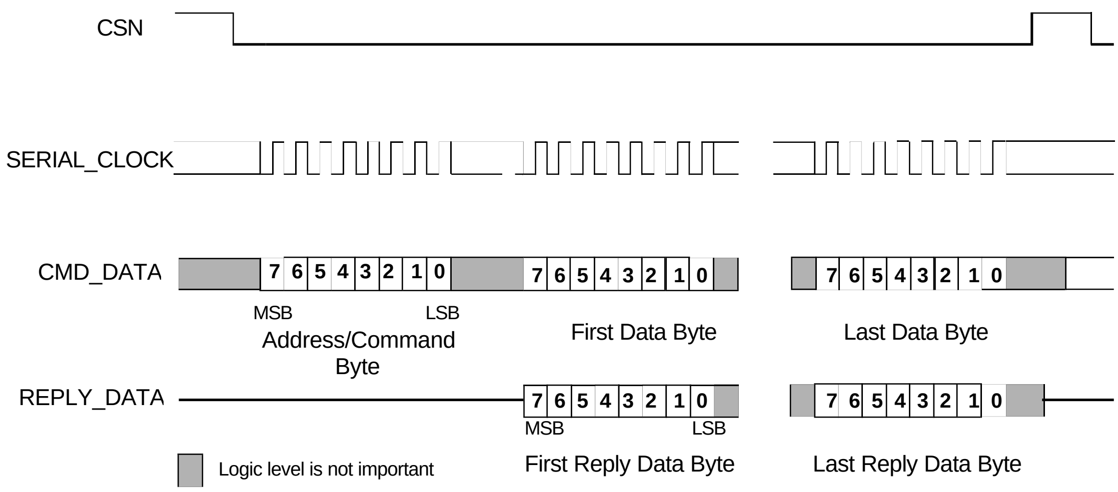


Figure 19 "C-BUS" Protocol

Signal data must be transferred at the rate appropriate to the signal type. The CMX880 buffers signal data in 16-bit word registers, one for data from the CMX880 (REPLY_DATA) and one for data from the host µC (CMD_DATA). All signal data is transferred as 16-bit words. If the "C-BUS" is being used to transfer signal data, the CMX880 will issue interrupts to indicate when data is available or required. The µC must respond to these interrupts within the maximum allowable latency for the signal type. Table 17 shows the maximum latencies for transferring signal data over the "C-BUS", to maintain appropriate data throughput.

Table 17 Maximum Data Transfer Latency

Signal type	Max time to replenish 16-bit data buffer	Effective data size	Baseband rate
Analogue voice band (from Mic or to Audio)	125µs	1 word/buffer	8000 words/s
C4FM/CQPSK	1.66ms	8 symbols/buffer	4800 symbols/s
FFSK - 1200baud	13.2ms	16 bits/buffer	1200 bits/s
FFSK - 2400baud	6.6ms	16 bits/buffer	2400 bits/s

1.5.1.7 Fast Serial Bus Operation

The Fast Serial Bus is provided to maximise throughput when transferring data between the CMX880 and an external DSP. It is based on the industry standard three wire serial interface, to allow communication with standard DSP ICs using a minimum of external components. This interface is capable of full duplex operation, so that data can be transferred to and from a DSP concurrently. This facilitates transferring data at different word rates corresponding (for example) the received C4FM symbol rate of 4800 symbols/s to the DSP and the digitised voice sample rate to the audio output path at 8000S/s from the DSP.

The Fast Serial Bus comprises 5 signals

1. FSB_CLOCK [output from the CMX880]
2. FSB_SYNC_OUT [output from the CMX880]
3. FSB_DATA_OUT [output from the CMX880]
4. FSB_SYNC_IN [output from the CMX880]
5. FSB_DATA_IN [input to the CMX880]

Data is transferred from the CMX880 to the DSP over the FSB_DATA_OUT port. Data is transferred from the DSP to the CMX880 over the FSB_DATA_IN port. The FSB_CLOCK is driven by the CMX880 and is common for both ports. The data transfer protocol is shown in Figure 20. Data is transferred over the Fast Serial Bus as 16-bit words. The Sync signals flag the start of a transfer. The most significant bit of the data to be transferred follows on the next clock cycle after the Sync pulse. If the sync pulse is on FSB_SYNC_OUT, the data will be transferred from the CMX880 to the DSP on FSB_DATA_OUT. If the sync pulse is on FSB_SYNC_IN, the data will be transferred from the DSP to the CMX880 on FSB_DATA_IN.

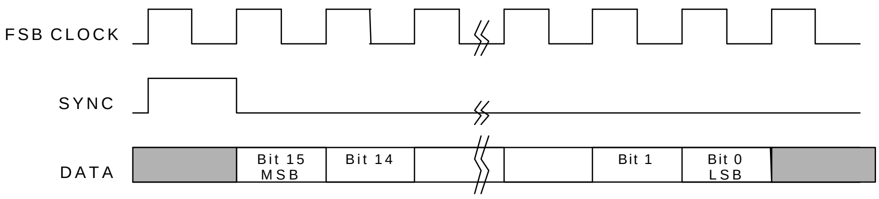


Figure 20 Fast Serial Bus Data Transfer Protocol

Two 16-bit registers form part of the CMX880 Fast Serial Bus interface; a serial to parallel register (RI) for data transfers from the DSP to the CMX880 and a parallel to serial register (RO) for transferring data from the CMX880 to the DSP.

The CMX880 takes data from RI to be processed for the output path, either to drive the modulator outputs or the audio outputs. Whenever RI is read by the device a new FSB In transfer is initiated. Thus the input word transfer rate is determined by the type of signal being processed (voice, C4FM symbol or FFSK bit stream); see Table 17.

Processed input path data, either from the FM Discriminator input (FM_DISC) or from one of the Microphone inputs (MIC_1 or MIC_2), is placed in RO by the CMX880 when it is available. Whenever RO is loaded by the device a new FSB Out transfer is initiated. Thus the output word transfer rate is determined by the type of signal being processed (voice, C4FM symbol or FFSK bit stream).

1.5.2 Software Description

1.5.2.1 "C-BUS" Register Description

Summary of "C-BUS" Write Only Registers

ADDR. (hex)	REGISTER	Word Size (bits)
$01	RESET	0
$B0	ANALOGUE INPUT PATH CONFIGURATION	16
$B1	ANALOGUE OUTPUT PATH CONFIGURATION	16
$B2	RSSI THRESHOLDS	16
$B3	RSSI TIMING	8
$C0	POWER DOWN	16
$C1	TRANSMIT MODE CONTROL	16
$C2	RECEIVE MODE CONTROL	16
$C3	TX DATA	16
$C7	FFSK/MSK SYND	16
$C8	'PROGRAMMING REGISTER'	16
$CA	FFSK/MSK SYNC	16
$CB	TX SELCALL TONE	16
$CD	DTMF TX AND TONE LEVEL	16
$CE	INTERRUPT MASK	16
$CF	RESERVED REGISTER ADDRESS	16

The "C-BUS" address $CF is allocated for production testing and must not be accessed in normal operation.

Summary of "C-BUS" Read Only Registers

ADDR (hex)	REGISTER	Word Size (bits)
$B4	RSSI MEASUREMENT DATA	8
$C5	RX DATA	16
$C6	STATUS	16
$C9	C4FM FS CROSS-CORRELATION PEAK	16
$CC	SUB-AUDIO AND SELCALL STATUS	16

Interrupt Operation

The CMX880 will issue an interrupt on the IRQN line when the IRQ bit (bit 15) of the 'Status' register and the 'IRQ Mask' bit (bit 15) are both set to '1'. The IRQ bit is set when the state of the interrupt flag bits in the 'Status' register change and the corresponding mask bit(s) in the 'Interrupt Mask' register is(are) set.

All interrupt flag bits in the 'Status' register except the 'Programming Flag' (bit 0) are cleared and the interrupt request is cleared following the command/address phase of a "C-BUS" read of the flag register. The 'Programming Flag' bit is cleared only when it is permissible to write a new word to the 'PROGRAMMING REGISTER'.

$01 GENERAL RESET: address only.
The reset command has no data attached to it. It sets the device registers into the states listed below.

Addr.	REG.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$B0	ANALOGUE INPUT PATH CONFIGURATION	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B1	ANALOGUE OUTPUT PATH CONFIGURATION	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$B2	RSSI THRESHOLDS	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
$B3	RSSI TIMING									0	0	0	0	0	0	0	0
$B4	RSSI MEASUREMENT DATA									X	X	X	X	X	X	X	X
$C0	POWER DOWN AND RAMP RATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C1	TRANSMIT MODE CONTROL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C2	RECEIVE MODE CONTROL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C3	TX DATA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C5	RX DATA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C6	STATUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C7	FFSK/MSK SYND (RX SYNC)	1	1	0	0	0	1	0	0	1	1	0	1	0	1	1	1
	(preset to MPT1327 SYNC)																
$C8	‘PROGRAMMING REGISTER’	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$C9	C4FM FS CROSS-CORRELATION PEAK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CA	FFSK/MSK SYNC	1	1	0	0	0	1	0	0	1	1	0	1	0	1	1	1
	(preset to MPT1327 SYNC)																
$CB	TX SELCALL TONE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CC	SUB-AUDIO AND SELCALL STATUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CD	DTMF TX AND TONE LEVEL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CE	INTERRUPT MASK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$CF	Reserved Register Address	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

$B0 ANALOGUE INPUT PATH CONFIGURATION: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Input Select		0	Data Destination		0	0	0	0	Input Gain			Audio Output Attenuation			

Bit 15	Bit 14	Input select
0	0	No input selected (ADC input ≡ V_{BIAS})
0	1	Microphone 1 (MIC1)
1	0	Microphone 2 (MIC2)
1	1	FM Discriminator (FMdisc)

Bit 12	Bit 11	Data destination
0	0	Internal only
0	1	Internal and “C-BUS”
1	0	Internal and FSB
1	1	Internal, FSB and “C-BUS”

Bit 6	Bit 5	Bit 4	Input Gain
0	0	0	0dB
0	0	1	3.2dB
0	1	0	6.4dB
0	1	1	9.6dB
1	0	0	12.8dB
1	0	1	16.0dB
1	1	0	19.2dB
1	1	1	22.4dB

The input path provides a user programmable gain stage to amplify low power voice signals from the microphone inputs, thus allowing a vogad facility to be implemented by software control. Finer gain control can be achieved with the ‘FINE INPUT GAIN’ control register.

Bit 3	Bit 2	Bit 1	Bit 0	Audio Output Attenuation
0	0	0	0	>60dB
0	0	0	1	44.8dB
0	0	1	0	41.6dB
0	0	1	1	38.4dB
0	1	0	0	35.2dB
0	1	0	1	32.0dB
0	1	1	0	28.8dB
0	1	1	1	25.6dB
1	0	0	0	22.4dB
1	0	0	1	19.2dB
1	0	1	0	16.0dB
1	0	1	1	12.8dB
1	1	0	0	9.6dB
1	1	0	1	6.4dB
1	1	1	0	3.2dB
1	1	1	1	0dB

The output path provides a user programmable attenuation stage to adjust the volume of the audio output signal. Finer volume control can be achieved with the ‘FINE OUTPUT GAIN 1’ control register.

Bits 7 to 10 and 13 reserved - set to 0.

$B1 ANALOGUE OUTPUT PATH CONFIGURATION: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Source		DAC1 Dest	MOD2 Source	SA Dest	0	0	0	0	0	MOD 1 Attenuation			MOD 2 Attenuation		

Bit 15	Bit 14	**Data source (to DAC 1)**
0	0	No output data source selected
0	1	C-BUS
1	0	FSB
1	1	Internal (from ΣΔ ADC)

Bit 13	**DAC 1 destination**
0	Audio output port
1	Modulator output ports (MOD_1 and, if Bit 12 = 0, MOD_2)

Bit 12	**MOD 2 source**
0	DAC 1
1	DAC 2

Bit 11	**Sub-Audio destination**
0	Composite Sub-audio + in-band signal to both DACs
1	In-band signal to DAC 1; Sub-audio to DAC 2

Fine output gain control 2 is only available when bit 12 is set to 1. To utilise the independent fine output attenuation controls, when transmitting using two point modulation, bit 12 should be set to 1. If the coarse adjustment is sufficiently accurate, then clearing bit 12 to 0 can save power.

When transmitting ‘CQPSK’ bit 12 must be set to 1. During ‘CQPSK’ transmission the ‘I’ component is routed to the MOD_1 output via DAC 1 and the ‘Q’ component is routed to the MOD_2 output via DAC 2. The state of bit 11 does not affect operation of CQPSK transmission.

When transmitting ‘voice + sub-audio’ with voice and sub-audio routed to separate modulator output ports, bit 12 must be set to 1. During ‘voice + sub-audio’ transmission the voice can be routed to the MOD_1 output via DAC 1 and the sub-audio signal routed to the MOD_2 output via DAC 2, or the voice and sub-audio can be combined and either routed to both MOD_1 and MOD_2 via DAC 1 or MOD_1 via DAC 1 and MOD_2 via DAC 2. The facility to merge sub-audio with voice or to keep them separate is controlled by ‘SA Dest’ bit (bit 11).

<u>NOTE</u>: voice in this context refers to any of the ‘ín-band’ signals; voice, Selcall tone, DTMF tones or FFSK/MSK.

Bits 6 to 10 reserved - set to 0.

Bit 5	Bit 4	Bit 3	**MOD 1 Output Attenuation**
0	0	0	>40dB
0	0	1	12dB
0	1	0	10dB
0	1	1	8dB
1	0	0	6dB
1	0	1	4dB
1	1	0	2dB
1	1	1	0dB

Bit 2	Bit 1	Bit 0	**MOD 2 Output Attenuation**
0	0	0	>40dB
0	0	1	12dB
0	1	0	10dB
0	1	1	8dB
1	0	0	6dB
1	0	1	4dB
1	1	0	2dB
1	1	1	0dB

Note:
The output paths provide user programmable attenuation stages to independently adjust the modulators’ output levels. Finer level control of the ‘MOD 1’ output can be achieved with the ‘FINE OUTPUT GAIN 1’ control register and fine level control of the ‘MOD 2’ output can be achieved with the ‘FINE OUTPUT GAIN 2’ control register.

$B2 RSSI THRESHOLDS: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	High Threshold [Range: 0 to 255]								Low Threshold [Range: 0 to 255]							

If the RSSI level exceeds the High Threshold, the 'RSSI Present' bit of the 'STATUS' register will be set to 1. If the RSSI level falls below the Low Threshold, the 'RSSI Absent' bit of the 'STATUS' register will be set to 1. For each condition, if the corresponding interrupt bit is enabled, a "C-BUS" interrupt will be generated. These status bits are cleared when the 'Status' register is read. The behaviour of the CMX880 is not defined if the high threshold is less than the low threshold.

Threshold resolution: V_{DD}(A)/256 V per LSB.
Threshold accuracy: ±2 LSB.
Differential Linearity: ±1 LSB [monotonic].

The 'RSSI THRESHOLD' register must not be updated whilst RSSI monitoring is enabled.

$B3 RSSI TIMING: 8-bit write-only

Bit:	7	6	5	4	3	2	1	0
	0	0	Conversion Interval					

The 'Conversion Interval' defines the time between measurements of the RSSI input level whilst in 'RSSI Monitor' mode. This allows the user to trade-off device power consumption with receiver response time.

RSSI Monitor mode power	= 0.5mW/V_{DD}(A)/conversion	(approximate)
Conversion Interval resolution	= 12µs/conversion per LSB.	(approximate)
Recommended Maximum Conversion Interval	= 120µs	(for auto start-up)

The Recommended Maximum Conversion Interval is recommended for automatic receiver start-up on RSSI level exceeding the 'RSSI High Threshold'. The user should set an interval to ensure that none of the start of a received signal is missed, so that the signal type can be correctly identified.

The 'RSSI TIMING' register must not be updated whilst RSSI monitoring is enabled.

$B4 RSSI MEASUREMENT DATA: 8-bit read-only

Bit:	7	6	5	4	3	2	1	0
	RSSI Level							

This data holds the result of the last RSSI level measurement performed by the auxilliary ADC.

$C0 POWER DOWN AND RSSI MONITORING CONTROL: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8
	MIC 1	MIC 2	FM Disc	ADC	DAC 1	DAC 2	MOD 1	MOD 2

Bit:	7	6	5	4	3	2	1	0
	Audio Op	BIAS	Signal Processor	0	Xtal_N	Clock_Out_N	EN RSSI Monitor	RSSI Auto start-up

Bits 15-5 provide the power control of the specified blocks. If a bit is 1, the corresponding block is on, else it is powered down. Bits 4 is reserved; set to 0. Bit 5 resets the internal signal processing block and places it into power-save mode. The clock output is disabled by setting 'Clock_Out_N' (bit 2) to '1'. On reset, bit 2 is cleared to '0', so that clock output is enabled.

The xtal clock circuit is powered down by setting bit 3 to 1. On reset, bit 3 is cleared to 0, which enables the xtal clock circuit. The CLOCK/XTAL pin can be driven by an external clock source, whether the clock circuit is powered-up or powered-down.

If ‘EN RSSI Monitor’ bit 1 is set to 1, RSSI monitoring is enabled. The RSSI monitor will generate interrupts in accordance with the settings of the interrupt mask bits. If ‘EN RSSI Monitor’ bit is cleared to 0, RSSI monitoring is disabled and the auxilliary ADC is powered down.

If ‘RSSI Auto start-up’ bit 0 is set to 1, when the RSSI input rises above the ‘RSSI High Threshold’, the CMX880 will automatically start up the receiver and initiate received signal type identification. If ‘RSSI Auto start-up’ is cleared to 0 the CMX880 will not automatically start-up, so it is up to the user to respond accordingly to RSSI interrupts.

$C7 FFSK/MSK RX SYND: 16-bit write-only
$CA FFSK/MSK RX SYNC/SYNT: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SYND Pattern															
	SYNC/SYNT Pattern															

The SYNC, SYNT and SYND define three programmable 16-bit synchronisation words that can be compared with incoming RX data. The SYNT bit pattern is the inverse of the SYNC bit pattern which is programmed into the ‘FFSK/MSK SYNC/SYNT’ register. The SYND pattern is programmed into the ‘FFSK/MSK SYND’ register. When a match is found with an enabled sync pattern the signal is identified as an FFSK/MSK signal and the start of an FFSK/MSK data transfer is indicated. Both these registers are set to correspond to the MPT1327 sync pattern following a reset. The most significant bit (bit 15) of the sync pattern is received first.

$CB TX SELCALL TONE: 16-bit write only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	Notone	Selcall Frequency Code												

The ‘Selcall Tone Frequency’ bits define the tone in accordance with the formula below. If the tone frequency is programmed with 0, or if the ‘Notone’ bit (bit 13) is set to 1, no Selcall tone will be transmitted.

When the ‘Notone’ bit is set to 0 and Selcall transmit mode is enabled, the Selcall tone is transmitted along with the signal source defined by the ‘ANALOGUE OUTPUT PATH CONFIGURATION’ register and ‘TX MODE’ register settings.

The frequency of the transmitted Selcall tone is define according to the formula:

$$\text{Frequency Code} = (\text{integer})(2.730625 \times \text{frequency})$$

It is up to the user/host µC to suppress voice data before initiating a Selcall tone transmit and to re-enable voice data on completion of the Selcall tone transmit. Timing of the intervals between voice suppression, Selcall transmit and re-enable voice is also controlled by the user/host µC.

$CD DTMF TX AND TONE LEVEL: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Tone Level (range 0 to 255)								HI	LO	0	2dB	TonePair			

Bit 7 (HI)		
	0	Disable transmit High Tone
	1	Enable transmit High Tone

Bit 6 (LO)		
	0	Disable transmit Low Tone
	1	Enable transmit Low Tone

Bit 3	Bit 2	Bit 1	Bit 0	Key Pad Position	Low Tone	High Tone
0	0	0	1	1	697Hz	1209Hz
0	0	1	0	2	697Hz	1336Hz
0	0	1	1	3	697Hz	1477Hz
0	1	0	0	4	770Hz	1209Hz
0	1	0	1	5	770Hz	1336Hz
0	1	1	0	6	770Hz	1477Hz
0	1	1	1	7	852Hz	1209Hz
1	0	0	0	8	852Hz	1336Hz
1	0	0	1	9	852Hz	1477Hz
1	0	1	0	0	941Hz	1336Hz
1	0	1	1	*	941Hz	1209Hz
1	1	0	0	#	941Hz	1477Hz
1	1	0	1	A	697Hz	1633Hz
1	1	1	0	B	770Hz	1633Hz
1	1	1	1	C	852Hz	1633Hz
0	0	0	0	D	941Hz	1633Hz

Bit 4 enables twist between the high and low tone groups. If Bit 4, the 2dB control bit, is set to ‘0’, the High and Low Tone levels are set to the same level. If Bit 4 is set to ‘1’, the Low Tone level is set to -2dB below the High Tone level.

The ‘Tone Level’ bits 15 (MSB) to 8 (LSB) set the ‘non-voice’ in-band analogue levels (DTMF High Tone; Selcall tone and FFSK/MSK) with a resolution of V_{DD}/512 (1.94mV at V_{DD}(A)=5V) per LSB.

$C3 TX DATA: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFSK/MSK	MS Data Byte								LS Data Byte							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C4FM/ CQPSK	Symbol 7		Symbol 6		Symbol 5		Symbol 4		Symbol 3		Symbol 2		Symbol 1		Symbol 0	
	Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0
VOICE	2’s complement encoded voice data															

This word holds either the next 2 bytes of FFSK/MSK data, the next 8 C4FM/CQPSK symbols or the next Voice level data to be transmitted. Outgoing data is treated as continuous. If new data is not provided before the current data has been transmitted, the current data will be re-transmitted, until new data is provided. Transmission of the current word of data will be completed before transmission of the new data begins.

The most significant bit of FFSK/MSK data is transmitted first. The most significant symbol of C4FM/CQPSK data is transmitted first. Bits or symbols beyond the actual data message length should be padded with innocuous values (system dependent). In the C4FM case an innocuous symbol sequence may be “+3, +3, -3, -

3, …" and in the FFSK case an innocuous bit sequence may be all '1's. The modulator outputs can be ramped down whilst transmitting this data padding.

Voice data is the sampled voice data to be output to the audio output during a voice based signal reception or is the sampled voice data to drive the modulator outputs during a voice based signal transmission.

It is recommended that the symbol stream for transmitting C4FM or CQPSK utilises the Fast Serial Bus interface, rather than the "C-BUS" interface.

$C5 RX DATA: 16-bit read-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFSK/MSK	MS Data Byte								LS Data Byte							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C4FM/	Symbol 1		2s complement						Symbol 0		2s complement					
CQPSK	Bit 1	Bit 0	Symbol sample quality data						Bit 1	Bit 0	Symbol sample quality data					
VOICE	2's complement encoded voice data															

This word holds either the last 16 bits of received and decoded FFSK/MSK data, the last 2 decoded C4FM symbols or the most recently received Voice signal level. The MS bit of the FFSK/MSK data is received first. The most significant symbol of C4FM data is received first.

FFSK/MSK is transferred synchronously, so incoming FFSK/MSK data is decoded as a continuous stream of bits, with no detection of start, stop or parity bits and no CRC checking. If data is not read before the next 16 bits of data are received and decoded, the old data will be overwritten with the new data.

Voice data is the voice input from the selected microphone input during transmission, or the extracted (by band pass filtering) voice signal from the FM discriminator input during receive.

It is recommended that the symbol stream from the C4FM receiver utilises the Fast Serial Bus interface, rather than the "C-BUS" interface.

$CE INTERRUPT MASK: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8
	IRQ MASK	RX FFSK/MSK SYNC EN	RX FFSK/MSK SYNT EN	RX FFSK/MSK SYND EN	Unlisted Tone MASK	C4FM FS Tolerance MASK	RX CTCSS MASK	RX DCS MASK

Bit:	7	6	5	4	3	2	1	0
	RX C4FM detected MASK	RX Selcall MASK	RX FFSK/MSK MASK	TX data MASK	RX data MASK	RSSI High MASK	RSSI Low MASK	Prog Flag MASK

Bit		**Function**
15	1	Enable selected interrupts
	0	Disable all interrupts.
12,13,14	1	Enable corresponding FFSK/MSK sync pattern detection
	0	Disable corresponding FFSK/MSK sync pattern detection
11	1	Enable interrupts for 'Unlisted Tone' detection status changes. See 'INTERRUPT MASK' register bit 9 and bit 6.
	0	Disable 'Unlisted Tone' detection status changes from issuing interrupts.
10	1	Enable interrupt when C4FM FS tolerance data is available
	0	Disabled
9	1	Enable interrupt when a change to a programmed CTCSS tone is detected, by a change of state on bit 7 of the 'SUB-AUDIO AND SELCALL STATUS' register. Also, if bit 11 of the 'INTERRUPT MASK' register is set to 1, enable interrupt when a change to a valid but unlisted CTCSS tone is detected, by a change of state on bit 4 of the ' SUB-AUDIO AND SELCALL STATUS' register.
	0	Disabled
1,2,5,8	1	Enable interrupt when corresponding status changes
	0	Disabled
7	1	Enable interrupt when received C4FM signal is detected
	0	Disabled
6	1	Enable interrupt when a change to a programmed Selcall tone is detected by a change of state on bit 15 of the ' SUB-AUDIO AND SELCALL STATUS' register. Also, if bit 11 of the 'INTERRUPT MASK' register is set to 1, enable interrupt when a change to a valid but unlisted Selcall tone is detected, by a change of state on bit 12 of the ' SUB-AUDIO AND SELCALL STATUS' register.
	0	Disable
4	1	Enable interrupt when TX data required
	0	Disabled
3	1	Enable interrupt when RX data is available
	0	Disabled
0	1	Enable interrupt when Prog Flag bit of 'STATUS' register changes (see 'PROGRAMMING REGISTER' $C8)
	0	Disabled

$C6 STATUS: 16-bit read-only

Bit:	15	14	13	12	11	10	9	8
	IRQ	FFSK/MSK Sync Type		C4FM FS Tolerance			CTCSS state change	DCS state change

Bit:	7	6	5	4	3	2	1	0
	C4FM FS detected	Selcall state change	FFSK/MSK detected	TX data required	RX data available	RSSI High	RSSI Low	Programming Flag

This word holds the current status of the CMX880. Changes in the state of the 'STATUS' register will cause the IRQ bit (bit 15) to be set to 1, if the corresponding interrupt mask is enabled. An interrupt request is issued on the IRQN line when IRQ is set to 1, if the IRQ MASK bit (bit 15) in the 'INTERRUPT MASK' register ($CE) is set to 1.

If the status indicates that a sub-audio or Selcall event caused the interrupt, the host should then read the 'SUB-AUDIO AND SELCALL STATUS' register for further information.

Bits 1 to 15 of the 'STATUS' register are cleared to 0 after the 'STATUS' register is read. Bit 0 is not cleared by reading the 'STATUS' register.

The 'PROGRAMMING REGISTER' should only be written to when the Programming Flag (bit 0) is set to 1. Writing to the 'PROGRAMMING REGISTER' clears the Programming Flag to 0. The Programming Flag is restored to 1 when the programming action is complete, normally within 250µs**,** when it is safe to write to the 'PROGRAMMING REGISTER'. See 'PROGRAMMING REGISTER' $C8.

The C4FM FS Tolerance bits 10 to 12 identify the number of level mismatches detected during a C4FM frame sync pattern. If 'C4FM FS Tolerance MASK' bit (bit 10) of the 'INTERRUPT MASK' register is set to 1, an interrupt will be generated when the value of bits 12 to 10 become non-zero.

Bit 12	Bit 11	Bit 10		
0	0	0		Tolerance Value Not Available
0	0	1		0 mismatches
0	1	0	≤	2 mismatches
1	0	0	≤	4 mismatches
1	1	0	≤	6 mismatches
1	1	1	≥	7 mismatches

Bit 4 indicates that new transmit data is required and should be provided within the time appropriate for the signal type (see section 1.5.1.6).

Bit 3 indicates that new receive data is available and should be read within the time appropriate for the signal type (see section 1.5.1.6).

RSSI High (bit 2) and RSSI Low (bit 1) reflect the state of the RSSI level, with respect to the RSSI high and low thresholds.

RSSI High	RSSI Low	
X	1	RSSI Level below RSSI Low Threshold
1	X	RSSI Level above RSSI High Threshold

$CC SUB-AUDIO AND SELCALL STATUS: 16-bit read-only

Bit:	15	14	13	12	11	10	9	8
	Listed Selcall tone present	0	0	Unlisted Selcall tone present	Detected Selcall Tone Frequency			

Bit:	7	6	5	4	3	2	1	0
	Listed CTCSS tone present	DCS Code present	DCS Inverted	Unlisted Sub-Audio Tone present	Detected CTCSS Tone Frequency			

This word holds the current status of the CMX880 sub-audio and Selcall sections. This word should be read by the host, following an interrupt caused by a sub-audio or Selcall event.

If bit 15 = 1 a Listed (pre-programmed) Selcall tone has been detected. The detected Selcall frequency is indicated by the content of bits 8 to 11. The value in bits 8 to 11, 'Detected Selcall Tone Frequency', identifies the frequency by its position in the Selcall tone table (see 'PROGRAMMING REGISTER', address $C8). If bit 15 = 0 there is no Selcall tone being detected. A change in the state of bit 15 will cause bit 6 of the 'STATUS' register ($C6), 'Selcall State Change', to be set to 1.

If a Selcall tone is detected but is not in the Selcall Tone table, bit 12 will be set to 1; zero otherwise. A change in the state of bit 12 will cause the 'CTCSSS State Change' bit (bit 6) of the 'STATUS' register ($C6) to be set to 1.

If bit 7 = 1 a Listed (pre-programmed) CTCSS tone has been detected. The detected CTCSS frequency is indicated by the content of bits 0 to 3. The value in bits 0 to 3, 'Detected CTCSS Tone Frequency', identifies the frequency by its position in the CTCSS tone table (see 'PROGRAMMING REGISTER', address $C8). If bit 7 = 0 there is no CTCSS tone being detected. A change in the state of bit 7 will cause bit 9 of the 'STATUS' register ($C6), 'CTCSS State Change', to be set to 1.

If a CTCSS tone is detected in the sub-audio range, but is not in the CTCSS Tone table, bit 4 will be set to 1; zero otherwise. A change in the state of bit 4 will cause bit 9 of the 'STATUS' register ($C6), 'CTCSS State Change', to be set to 1.

If bit 6 = 1 the DCS code has been detected. If bit 6 = 0 there is no DCS code being detected. A change in the state of bit 6 will cause bit 8 of the 'STATUS' register ($C6), 'DCS State Change', to be set to 1. Bit 5 indicates whether the DCS code was detected as 'True' or 'Inverse' coding. If bit 5 is 0, the coding is 'True', corresponding to +ve frequency deviation representing a 1 and -ve frequency deviation representing a 0 in the RF band. If bit 5 is 1, the coding is 'Inverse', corresponding to -ve frequency deviation representing a 1 and +ve frequency deviation representing a 0 in the RF band. This bit is only applicable if bit 6 = 1.

$C9 C4FM FS CROSS-CORRELATION PEAK: 16-bit read only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FS Cross-Correlation Peak															

The value in this register provides quality information on the C4FM Frame Sync pattern recognition. Figure 21 shows how the FS cross-correlation peak value is affected by the signal to noise ratio.

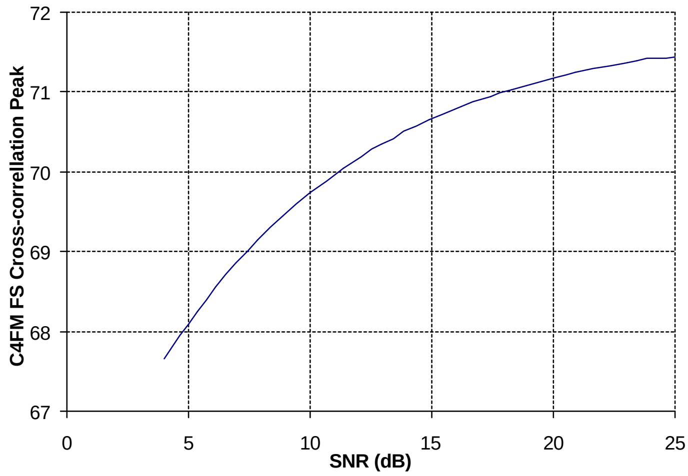


Figure 21 SNR vs Nominal C4FM Frame Sync Cross-Correlation Peak

This curve assumes no FS pattern level mismatches. If the FS threshold level is programmed sufficiently low to accommodate low signal to noise, there is a risk that a false FS pattern may be detected under less noisy signal conditions. To minimise the risk of false FS detection, the user should also programme the FS tolerance control of the RX Mode control register accordingly, or validate the FS detection by reading the FS tolerance status of the 'STATUS' register.

$C1 TRANSMIT MODE CONTROL: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8
	DCS Inverse	Voice EN	CTCSS TX	DCS TX	Selcall TX	DTMF TX	FFSK/MSK TX	2400 Baud

Bit:	7	6	5	4	3	2	1	0
	CQPSK TX	C4FM TX	Voice Filter Mode Select			Enable Ramp down	Enable Ramp up	TX EN

The Sub-Audio select bits determine what if any sub-audio is to be added to the signal before it is transmitted.

Bit 13	Bit 12	
0	0	No Sub-Audio Transmitted
0	1	DCS Code Transmit
1	0	CTCSS Tone Transmit
1	1	Reserved – do not use.

The In-Band select bits determine what if any in band tones are to be added to the signal before it is transmitted. The voice signal must be disabled, by clearing 'Voice Enable' bit 14 to 0, before transmitting Selcall, DTMF or FFSK tones.

If DCS Inverse bit 15 = 1, DCS will be transmitted such that a DCS ‘1’ will generate a –ve voltage swing (below V_{BIAS}) and a DCS ‘0’ will generate a +ve voltage swing (above V_{BIAS}). If DCS Inverse bit 15 = 0, DCS will be transmitted such that a DCS ‘1’ will generate a +ve voltage swing (above V_{BIAS}) and a DCS ‘0’ will generate a -ve voltage swing (below V_{BIAS}). See Table 4 DCS Modulation Modes.

Bit 11	Bit 10	Bit 9	
0	0	0	No In-Band (Voice) Signalling Transmitted
0	0	1	FFSK/MSK Transmit
0	1	0	DTMF Tones Transmit
1	0	0	Selcall Tone Transmit
X	X	X	Do not use other code combinations.

If FFSK/MSK is enabled, the baud rate is controlled by bit 8, ‘2400baud’. If bit 8 = 0, 1200baud will be selected; if bit 8 = 1, 2400baud will be selected.

The voice filter control bits determine the filter mode applied to the voice or In-Band tone signal before it is transmitted. Pre-emphasis can be applied without other filtering by setting bits 5, 4, 3 = 0, 0, 1.

Bit 5	Bit 4	Bit 3	
0	0	0	No filtering.
X	X	1	Enable pre-emphasis.
0	1	X	12.5kHz channel filtering.
1	0	X	25.0kHz channel filtering.
1	1	0	APCO 25.
1	1	1	Reserved – do not use.

The C4FM/CQPSK select bits determine which digital transmit mode is to be transmitted, if any. If voice is being encoded and transmitted, bit 14, ‘Voice Enable’ should be set to 1, bits 5 to 7 should select APCO 25. If data is being transmitted ‘Voice Enable’ should be cleared to 0.

Bit 7	Bit 6	
0	0	C4FM AND CQPSK TX OFF
0	1	C4FM
1	0	CQPSK
1	1	Reserved – do not use.

If transmitting using C4FM or CQPSK, bits 9 to 13 <u>must</u> all be 0. Likewise if transmitting on an analogue channel, bits 6 and 7 <u>must</u> both be 0.

$C2 RECEIVE MODE CONTROL: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8
	En C4FM	En FFSK 1200b	En FFSK 2400b	En CTCSS	En DCS True	En DCS Inverse	En Selcall	Auto Detect Mode

Bit:	7	6	5	4	3	2	1	0
	Voice Filter			Voice EN	C4FM RX Mode			RX EN

Bit	Name		Function:
0	Rx Enable	0 1	Disable all receiver functions. Enable selected receiver functions. Processing of enabled signals continues until the receiver is disabled.
1,2,3	C4FM Rx Mode		These bits select the clock and level tracking modes.
4	Voice Enable	0 1	Disable voice signal routing to the AUDIO output. Decoded voice data can still be read over the “C-BUS”or FSB. Enable routing of voice signal to AUDIO ouput.
5,6,7	Voice Filter Mode		These bits select the type of filtering (including de-emphasis) that is applied to the voice band signal prior to outputting to the AUDIO output, “C-BUS”or FSB.
8	Auto Detect Mode		This bit controls the transition from the signal type identification phase to the signal decoding phase.
9	En Selcall	0 1	Disable Selcall detection. Enable detect and receive Selcall signals.
10	En DCS Inverse	0 1	Disable DCS Modulation Type B detection. Enable detect and receive DCS Modulation Type B signals.
11	En DCS True	0 1	Disable DCS Modulation Type A detection. Enable detect and receive DCS Modulation Type A signals.
12	En CTCSS	0 1	Disable CTCSS detection. Enable detect and receive CTCSS signals.
13	En FFSK 2400b	0 1	Disable FFSK 2400b detection. Enable detect and receive FFSK 2400b signals.
14	En FFSK 1200b	0 1	Disable FFSK 1200b detection. Enable detect and receive FFSK 1200b signals.
15	En C4FM	0 1	Disable C4FM detection. Enable detect and receive C4FM/CQPSK signals.

Auto Detect Mode:
The CMX880 has two receive phases; (1) signal type identification and (2) continuous signal processing. Phase 1 monitors the incoming signal and identifies the signal type, if that type has been enabled. Following signal type identification, phase 2 processes the incoming signal in accordance with the identified signal type. The Auto Detect Mode bit controls the action following identification of a signal type.

Bit 8	
0	Mode 0: CMX880 will process the detected signal and also continue searching for the presence of other enabled signal types. If a second signal type is found this also will be processed by the CMX880.
1	Mode 1: CMX880 will process the detected signal and cease searching for other signal types. Selcall is excluded from this mode.

Mode 0 can be used for processing analogue 'in-band' data signalling, allowing sub-audio detection to be followed by Selcall or FFSK detection and processing. Mode 0 can cause the CMX880 to become overloaded if too many signal types are enabled. Voice processing is not affected by the Auto Detect Mode bit.

C4FM processing requires the full capacity of the CMX880. If C4FM is enabled, the CMX880 must be placed in Mode 1 either before enabling receive mode (bit 0) or immediately after detection of a C4FM signal.

If additional signalling schemes need to be enabled after auto detection in mode 1, these can be individually enabled by setting the appropriate bits in the 'RECEIVE MODE CONTROL' register, including the detected scheme, and setting the Auto Detect Mode bit to '0'.

Voice Filter Control:
The voice filter control bits determine the filter mode applied to the voice signal before it is output to the 'Audio' port. De-emphasis can be applied without other filtering by setting bits 7, 6, 5 = 0, 0, 1.

Bit 7	Bit 6	Bit 5	
0	0	0	No filtering.
X	X	1	Enable de-emphasis.
0	1	X	12.5kHz channel filtering.
1	0	X	25.0kHz channel filtering.
1	1	0	APCO 25.
1	1	1	Reserved – do not use.

C4FM RX Modes:

The C4FM RX Mode encodings are specific to receiving C4FM. When writing a new C4FM RX Mode after the signal type has been detected, in addition to setting the task code bits, the applicable receive mode, C4FM should be enabled and the other receive modes disabled.

Bit 3	Bit 2	Bit 1	
0	0	0	DEFAULT TRACKING MODES.
X	X	0	Stochastic Gradient symbol clock tracking.
X	X	1	Fixed symbol clock.
0	0	X	Slow symbol level tracking.
0	1	X	Fast symbol level tracking.
1	0	X	Partial Response symbol level tracking.
1	1	X	Fixed symbol levels.

Symbol Clock Extraction Modes:

1. Stochastic Gradient Clock Tracking mode is able to extract the symbol clock in the presence of relative clock drift between the transmitter and the receiver in excess of 40ppm. This is the default clock tracking mode following a reset.
2. Fixed Symbol Clock mode fixes the symbol sample point relative to the last tracked symbol sample point, using only the local receiver clock. This mode can be selected to override the clock tracking mode in circumstances where excessive noise could cause the tracking to shift to an inappropriate sampling phase.

When a C4FM signal is detected, by recognising the frame sync pattern, the optimum symbol sample timing is extracted from the received FS signal. This is irrespective of the selected clock tracking mode.

Symbol Level Tracking Modes:

1. Slow Symbol Level Tracking mode adjusts the symbol level thresholds to minimise the average symbol sample level errors (ie. the deviation of the sampled level from the optimum level). This is the default level tracking mode following a reset.
2. Fast Symbol Level Tracking mode adjusts the symbol level thresholds in the same way as Slow Symbol Level Tracking, but applies a larger level adjustment at each level change period.
3. Partial Response Symbol Level Tracking mode filters the received signal (after the sin(x)/x filtering) and tracks the peaks, from which the symbol levels are derived. The peak values decay slowly whilst the PR filtered signal is within these peak levels. This mode is particularly effective when receiving a noisy signal, but will not work well with certain long sequences of repeated symbol patterns.
4. Fixed Symbol Levels mode sets the symbol levels and thresholds to the last tracked symbol level. This mode can be selected to override the other level tracking modes in circumstances where excessive noise could cause the tracking to shift to inappropriate sample levels.

When a C4FM signal is detected, by recognising the frame sync pattern, the optimum symbol sample levels are extracted from the received FS signal. This is irrespective of the selected level tracking mode.

$C8 PROGRAMMING REGISTER: 16-bit write-only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	First Word	Block Number	Programming Data													

This register is used to programme various gains, levels, offset compensations, tones and codes. The programmed values are cleared by Reset or the ‘Signal Processing Block’ power-save.

The ‘PROGRAMMING REGISTER’ should only be written to when the Programme Flag bit (bit 15) of the ‘STATUS’ register is set to 1. The Programme Flag is cleared when the ‘PROGRAMMING REGISTER’ is written to. When the corresponding programming action has been completed (normally within 250µs) the CMX880 will set the flag back to 1 to indicate that it is now safe to write the next programming value. Do not write to the ‘PROGRAMMING REGISTER’ while the Programme Flag bit is 0. Programming is done by writing a sequence of 16-bit words to the ‘PROGRAMMING REGISTER’, in the order shown in Table 18. The ‘PROGRAMMING REGISTER’ should only be written whilst RX and TX modes are disabled; bit 0 of TX Mode register and bit 0 of RX Mode register both 0. Writing data to the ‘PROGRAMMING REGISTER’ must be performed in the order shown for each of the blocks, however the order in which the blocks are written is not critical.

Bits 14 and 15 of each word define which block the word belongs to and if it is the first word of that block.

Bit 15	Bit 14		
1	0	First word of block 1.	(B1.1)
0	0	Following words of block 1.	(B1.2 to B1.27)
1	1	First word of block 2.	(B2.1)
0	1	Following words of block 2.	(B2.2 to B2.37)

Table 18 PROGRAMMING REGISTER Functions Summary

Programming Block 1		Programming Block 2	
Reference	Programming Function	Reference	Programming Function
B1.1	FINE INPUT GAIN	B2.1	TX CTCSS TONE
B1.2	INPUT OFFSET	B2.2	DCS CODE (UPPER)
B1.3	FINE OUTPUT GAIN 1	B2.3	DCS CODE (LOWER)
B1.4	FINE OUTPUT GAIN 2	B2.4	CTCSS TONE BW AND LEVEL
B1.5	OUTPUT 1 OFFSET	B2.5	TX SUB-AUDIO LEVEL
B1.6	OUTPUT 2 OFFSET	B2.6	RX CTCSS TONE 0
B1.7	RAMP RATE CONTROL	B2.7	RX CTCSS POLE COEFF 0
B1.8	RX C4FM UNIT LEVEL	B2.8	RX CTCSS TONE 1
B1.9	RX C4FM FRAME SYNC	B2.9	RX CTCSS POLE COEFF 1
	THRESHOLD	B2.10	RX CTCSS TONE 2
B1.10	TX C4FM/CQPSK UNIT LEVEL	B2.11	RX CTCSS POLE COEFF 2
B1.11	SELCALL TONE BW AND	B2.12	RX CTCSS TONE 3
	SIGNAL LEVEL	B2.13	RX CTCSS POLE COEFF 3
B1.12	RX SELCALL TONES 0	B2.14	RX CTCSS TONE 4
B1.13	RX SELCALL TONES 1	B2.15	RX CTCSS POLE COEFF 4
B1.14	RX SELCALL TONES 2	B2.16	RX CTCSS TONE 5
B1.15	RX SELCALL TONES 3	B2.17	RX CTCSS POLE COEFF 5
B1.16	RX SELCALL TONES 4	B2.18	RX CTCSS TONE 6
B1.17	RX SELCALL TONES 5	B2.19	RX CTCSS POLE COEFF 6
B1.18	RX SELCALL TONES 6	B2.20	RX CTCSS TONE 7
B1.19	RX SELCALL TONES 7	B2.21	RX CTCSS POLE COEFF 7
B1.20	RX SELCALL TONES 8	B2.22	RX CTCSS TONE 8
B1.21	RX SELCALL TONES 9	B2.23	RX CTCSS POLE COEFF 8
B1.22	RX SELCALL TONES 10	B2.24	RX CTCSS TONE 9
B1.23	RX SELCALL TONES 11	B2.25	RX CTCSS POLE COEFF 9
B1.24	RX SELCALL TONES 12	B2.26	RX CTCSS TONE 10
B1.25	RX SELCALL TONES 13	B2.27	RX CTCSS POLE COEFF 10
B1.26	RX SELCALL TONES 14	B2.28	RX CTCSS TONE 11
B1.27	RX SELCALL TONES 15	B2.29	RX CTCSS POLE COEFF 11
		B2.30	RX CTCSS TONE 12
		B2.31	RX CTCSS POLE COEFF 12
		B2.32	RX CTCSS TONE 13
		B2.33	RX CTCSS POLE COEFF 13
		B2.34	RX CTCSS TONE 14
		B2.35	RX CTCSS POLE COEFF 14
		B2.36	RX CTCSS TONE 15
		B2.37	RX CTCSS POLE COEFF 15
		B2.38	Reserved Word

The user must not exceed the defined word counts for each block. The word B2.38 is allocated for production testing and must not be accessed in normal operation.

PROGRAMMING REGISTER Block 1

$C8 (B1.1) FINE INPUT GAIN

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	0	Fine Input Gain (unsigned integer)													

Gain = 20 × log(IG/16384) [IG is the unsigned integer value in the 'Fine Input Gain' field]

Fine input gain adjustment should be kept within the range 0dB to -3.5dB.

Bits 15 must be set to '1' and bit 14 cleared to '0'.

$C8 (B1.2) INPUT OFFSET

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	2's complement offset, resolution = V_{DD}(A)/16384 per LSB													

Used to compensate for inherent offsets in the FM discriminator signal input. It is recommended that the offset is kept within the range +/-50mV.

Bits 15 and 14 must both be cleared to 0.

$C8 (B1.3) FINE OUTPUT GAIN 1

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	Fine Output Gain 1 (unsigned integer)													

$C8 (B1.4) FINE OUTPUT GAIN 2

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	Fine Output Gain 2 (unsigned integer)													

Gain = 20 × log(OG/16384) [OG is the unsigned integer value in the 'Fine Output Gain' field]

Fine output gain adjustment should be kept within the range 0dB to -3.5dB.

Bits 15 and 14 must both be cleared to 0.

$C8 (B1.5) OUTPUT 1 OFFSET

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	2's complement offset, resolution = V_{DD}(A)/16384 per LSB													

$C8 (B1.6) OUTPUT 2 OFFSET

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	2's complement offset, resolution = V_{DD}(A)/16384 per LSB													

Used to compensate for inherent offsets in the output path via DAC 1 (Output 1 Offset) and DAC 2 (Output 2 Offset). It is recommended that the offset is kept within the range +/-50mV.

Bits 15 and 14 must both be cleared to 0.

$C8 (B1.7) RAMP RATE CONTROL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	Ramp UP Rate Control (RRU) [Range: 0 to 127]							Ramp DOWN Rate Control (RRD) [Range: 0 to 127]						

The ramp-up rate and ramp-down rates can be independently programmed. The ramp rates apply to all the analogue output ports. They only affect those ports being turned on (ramp-up) or turned off (ramp down). The ramp rates should be programmed before ramping any outputs.

Ramp-up rate	= 0.833ms/LSB	Time to ramp-up to full gain =	(RRU $\times$ 0.833)ms
Ramp-down rate	= 0.833ms/LSB	Time to ramp down to zero gain =	(RRD $\times$ 0.833)ms

Bit 15 and bit 14 must be cleared to 0.

$C8 (B1.8) RX C4FM UNIT LEVEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	Unit Level (unsigned integer)												

The CMX880 derives the 4 C4FM symbol levels from the unit level programmed into the ‘RX C4FM UNIT LEVEL’ register. These levels are used to decode received C4FM signals and to monitor signal quality.

Symbol level	
+3	Unit level $\times$ +3
+1	Unit level $\times$ +1
–1	Unit level $\times$ –1
–3	Unit level $\times$ –3

The value programmed into the ‘RX C4FM UNIT LEVEL’ register is derived using the formula:

65336 $\times$ ‘Unit Level’ (V) / V_{DD}

For optimum performance it is recommended that the FM discriminator be set up so that the value programmed in the ‘RX C4FM UNIT LEVEL’ register is close to 2048 and the p-p signal level for a repeated symbol sequence of “+3, +3, –3, –3, +3, +3, –3, –3 …” is less than V_{DD}, with minimal distortion.

$C8 (B1.9) RX C4FM FRAME SYNC THRESHOLD

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	FS Tol		Tol En	0	0	0	Frame Sync Threshold							

This register has no affect in transmit mode. In receive mode, this register defines the accuracy with which the CMX880 identifies a C4FM signal and the Frame Sync pattern matching tolerance.

The Frame Sync Threshold defines the level that the cross-correlation of signal with the frame sync pattern must exceed before the CMX880 will detect a C4FM FS. The resultant FS cross-correlation peak value is made available in the FS Cross-Correlation Peak register. The value to be programmed into the ‘RX C4FM Frame Sync Threshold’ field is obtained using the formula:

‘Frame Sync Threshold’ $\times$ 2 [range 0 to255]

The maximum possible cross-correlation peak is 72 ‘units’, which corresponds to a programmed value of 144. The cross-correlation level achieved is affected by internal rounding and by the SNR, as shown in Figure 21. It is advised that the level be set to at least 5 (programmed value 10) less than the nominal level shown in Figure 21 for the minimum SNR in which the system will be expected to operate.

Tol En (bit 11) enables the tolerance checking facility, but does not affect availability of the C4FM FS Tolerance status. Frame Sync Tolerance (bits 13,12) defines the maximum number of mismatches allowed during a search for the Frame Sync pattern. The FS Mismatch count is made available in the ‘STATUS’ register.

B13	B12	B11	Mismatches allowed
X	X	0	No predefined limit (reliant only on threshold)
0	0	1	0
0	1	1	2
1	0	1	4
1	1	1	6

Note: A single 'mismatch' is defined as the difference between two adjacent symbol levels, thus if the symbol '+1' were expected, then received symbol values of '+3' and '-1' would count as 1 mismatch, a received symbol value of '-3' would count as 2 mismatches. A setting of '2 mismatches' is recommended for normal use.

$C8 (B1.10) TX C4FM/CQPSK UNIT LEVEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	Unit Level (+ve)												

The CMX880 derives the 4 C4FM symbol levels to be transmitted from the unit level programmed into the ‘TX C4FM Unit Level’ register.

Symbol level	
+3	Unit level $\times$ +3
+1	Unit level $\times$ +1
–1	Unit level $\times$ –1
–3	Unit level $\times$ –3

The value programmed into the ‘TX C4FM Unit Level’ register is derived using the formula:

$$65336 \times \text{‘Unit Level’ (V)} / V_{DD}$$

For optimum performance it is recommended that the FM modulator be set up so that the value programmed in the TX C4FM Unit Level register is close to 2048.

$C8 (B1.11) SELCALL TONE BW AND SIGNAL LEVEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	Signal Detection Level [range: 0 - 63]						Selcall Tone BW			

The ‘Signal Detection Level’ bits (bits 9 to 4) set the minimum Selcall and/or FFSK signal level that will be detected. The levels are set according to the formula:

‘Signal Detection Level’ $\times$ V_{DD}(A)/1024 [4.88mV per LSB at V_{DD}(A)=5V]

The detected tone bandwidth is set in accordance with the following table:

					BANDWIDTH	
	Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Will Decode**	**Will Not Decode**
	1	0	0	0	±1.1%	±2.4%
Recommended for CCIR	1	0	0	1	±1.3%	±2.7%
	1	0	1	0	±1.6%	±2.9%
	1	0	1	1	±1.8%	±3.2%
	1	1	0	0	±2.0%	±3.5%
	1	1	0	1	±2.2%	±3.7%
Recommended for ZVEI	1	1	1	0	±2.5%	±4.0%
	1	1	1	1	±2.7%	±4.2%

$C8 (B1.12 to B1.27) RX SELCALL TONES

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	Frequency Code											
					N (defined below)							R (defined below)				

The ‘RX SELCALL TONES’ data word is used to program the frequencies of up to 16 tones in the audio band that will be decoded by the receiver.

Each tone is identified by the ‘Tone Address’ address, which is determined by the order in which the tones are programmed. ‘Tone Addresses’ range from 0(hex) for the first tone to be programmed, through to F(hex) for the sixteenth tone to be programmed. If a Selcall tone is not required the ‘RX SELCALL TONES’ word should be set to zero.

The ‘Frequency Code’ bits of ‘RX SELCALL TONES’ contain the data representing the tone frequency according to the formula:

In-band Selcall tone formula:

N = (integer) (0.0295 × frequency)

R = (0.0295 × frequency − N) × 6000/frequency

PROGRAMMING REGISTER Block 2

$C8 (B2.1) TX CTCSS TONE

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	1	Notone	CTCSS Frequency Code												

The ‘CTCSS Tone Frequency’ bits define the tone in accordance with the formula below. If the tone frequency is programmed with 0, or if the ‘Notone’ bit (bit 13) is set to 1, no CTCSS tone will be transmitted.

When the ‘Notone’ bit is set to 0 and CTCSS transmit mode is enabled, the CTCSS tone is transmitted along with the signal source defined by the ‘ANALOGUE OUTPUT PATH CONFIGURATION’ register and ‘TX MODE’ register settings.

The frequency of the transmitted CTCSS tone is define according to the formula:

Frequency Code = (integer)(8.191875 × frequency)

$C8 (B2.2) DCS CODE (UPPER)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	1	0	DCS 23/24	DCS Bit 23	DCS Data (bits 22-12)										

$C8 (B2.3) DCS CODE (LOWER)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	1	0	0	DCS Data (bits 11-0)											

This data defines the DCS code for both transmit and receive modes.

‘DCS 23/24’ (bit 14 of upper word)

0 : 24-bit DCS code Set ‘DCS Bit 23’ (bit 11 of upper word) to the value required for the DCS code MSB.

1 : 23-bit DCS code Set ‘DCS Bit 23’ to 0.

The least significant bit (bit 0) of the DCS code is transmitted first and the most significant bit is transmitted last.

The following table lists the DCS codes, with the corresponding values (in Hex), which should be programmed into the 'DCS Data' fields for a 23-bit DCS sequence. This does not preclude other codes being programmed.

DCS Code	DCS Data B22-12	DCS Data B11-0	DCS Code	DCS Data B22-12	DCS Data B11-0	DCS Code	DCS Data B22-12	DCS Data B11-0
023	763	813	174	18B	87C	445	7B8	925
025	6B7	815	205	6E9	885	464	27E	934
026	65D	816	223	68E	893	465	60B	935
031	51F	819	226	7B0	896	466	6E1	936
032	5F5	81A	243	45B	8A3	503	3C6	943
043	5B6	823	244	1FA	8A4	506	2F8	946
047	0FD	827	245	58F	8A5	516	41B	94E
051	7CA	829	251	627	8A9	532	0E3	95A
054	6F4	82C	261	177	8B1	546	19E	966
065	5D1	835	263	5E8	8B3	565	0C7	975
071	679	839	265	43C	8B5	606	5D9	986
072	693	83A	271	794	8B9	612	671	98A
073	2E6	83B	306	0CF	8C6	624	0F5	994
074	747	83C	311	38D	8C9	627	01F	997
114	35E	84C	315	6C6	8CD	631	728	999
115	72B	84D	331	23E	8D9	632	7C2	99A
116	7C1	84E	343	297	8E3	654	4C3	9AC
125	07B	855	346	3A9	8E6	662	247	9B2
131	3D3	859	351	0EB	8E9	664	393	9B4
132	339	85A	364	685	8F4	703	22B	9C3
134	2ED	85C	365	2F0	8F5	712	0BD	9CA
143	37A	863	371	158	8F9	723	398	9D3
152	1EC	86A	411	776	909	731	1E4	9D9
155	44D	86D	412	79C	90A	732	10E	9DA
156	4A7	86E	413	3E9	90B	734	0DA	9DC
162	6BC	872	423	4B9	913	743	14D	9E3
165	31D	875	431	6C5	919	754	20F	9EC
172	05F	87A	432	62F	91A			

$C8 (B2.4) CTCSS TONE BW AND LEVEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	1	Sub-Audio Monitor Timeout [range: 0 - 15]				Sub-Audio Detection Level [range: 0 - 63]						CTCSS Tone BW			

The 'Sub-Audio Detection Level' bits (bits 9 to 4) set the minimum CTCSS or DCS signal level that will be detected. The levels are set according to the formula:

'Sub-Audio Detection Level' $\times$ V_{DD}(A)/8192 [0.61mV per LSB at V_{DD}(A)=5V]

The 'Sub-Audio Monitor Timeout' defines maximum time that the sub-audio signal detection can drop out before loss of sub-audio is asserted. The period is set according to the formula:

'Sub-Audio Monitor Timeout' $\times$ (8.0ms per LSB) [range 0 to 120ms]

The detected tone bandwidth is set in accordance with the following table:

	Bit 3	Bit 2	Bit 1	Bit 0	BANDWIDTH Will Decode	BANDWIDTH Will Not Decode
Recommended for CTCSS	1	0	0	0	±1.1%	±2.4%
	1	0	0	1	±1.3%	±2.7%
	1	0	1	0	±1.6%	±2.9%
	1	0	1	1	±1.8%	±3.2%
	1	1	0	0	±2.0%	±3.5%
	1	1	0	1	±2.2%	±3.7%
	1	1	1	0	±2.5%	±4.0%
	1	1	1	1	±2.7%	±4.2%

$C8 (B2.5) TX SUB-AUDIO LEVEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	1	0	0	0	0	Sub-Audio Level (range 0 to 1023)									

The 'Sub-Audio Level' bits 15 (MSB) to 8 (LSB) set the transmitted CTCSS or DCS sub-audio signal level (p-p) with a resolution of V_{DD}(A)/8192 per LSB (0.61mV per LSB at V_{DD}(A)=5V, giving a range 0 to 624.4mV).

$C8 (B2.6 to B2.36, even) RX CTCSS TONE

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	1	0	0	Frequency Code											
					N (defined below)							R (defined below)				

$C8 (B2.7 to B2.37, odd) RX CTCSS POLE COEFF

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	1	Pole Coefficient													

The 'RX CTCSS TONE' and 'RX CTCSS POLE COEFF' data are used to program the frequencies of up to 16 tones in the sub-audio band, that will be decoded by the receiver.

Each tone is identified by the 'Tone Address' address, which is determined by the order in which the tones are programmed. 'Tone Addresses' range from 0 for the first tone to be programmed, through to 15 for the sixteenth tone to be programmed.

The 'Frequency Code' bits (bits 11 to 0) of 'RX CTCSS TONE' contain the data representing the tone frequency according to the formula below. If a tone is not required these 12 bits should be set to zero.

Sub-audio CTCSS tone formula:

N = (integer) (0.236 $\times$ frequency)

R = (0.236 $\times$ frequency – N) $\times$ 1500/frequency

The remaining 14 bits of 'RX CTCSS POLE COEFF' contain the data representing the pole coefficient according to the formula below. For every programmed tone frequency, the corresponding pole coefficient must be programmed at the same tone address. If a tone is not required these 14 bits should be set to zero.

Pole Coefficient = 16383 $\times$ Tan(0.0020944 $\times$ frequency) [the value in brackets is in radians]

The 'Tone Address' (0 through to 15) is used as the code to indicate which tone has been decoded. This code appears in the 'RX Tone' field of the 'STATUS' register.

1.5.2.2 FSB Register Description

The FSB Data Word Format is dependent on the CMX880 mode of operation. The six main applications of the FSB are to transfer data between the CMX880 and the DSP:

- 'transmit C4FM/CQPSK symbol data' from the DSP to the CMX880,
- 'received C4FM symbol data' from the CMX880 to the DSP,
- 'Voice data (from Microphone or FM Discriminator input ports)' from the CMX880 to the DSP,
- 'Voice data (to Modulator or Audio output ports)' from the DSP to the CMX880,
- 'FFSK data' from the CMX880 to the DSP,
- 'FFSK data' from the DSP to the CMX880.

.

C4FM/CQPSK Transmit Symbol Data

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Symbol 7		Symbol 6		Symbol 5		Symbol 4		Symbol 3		Symbol 2		Symbol 1		Symbol 0	
	Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0

This word holds the next 8 C4FM/CQPSK symbols to be transmitted. The most significant symbol of C4FM/CQPSK data is transmitted first. Symbols beyond the actual data message length should be padded with innocuous values. The modulator outputs can be ramped down whilst transmitting this data padding.

C4FM Receive Symbol Data

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Symbol 1		2s complement Symbol sample quality data						Symbol 0		2s complement Symbol sample quality data					
	Bit 1	Bit 0							Bit 1	Bit 0						

This word contains the last 2 decoded C4FM symbols. The MS bit is received first.

Sampled Symbol Level	Bit 1	Bit 0
+3	0	1
+1	0	0
-1	1	0
-3	1	1

The 2s complement 'Symbol Sample Quality Data' represents the deviation of the sampled level from the perceived ideal sample level.

Range : –1.0 to +0.96875 of the unit symbol level.
Resolution : 0.03125 of the unit symbol level per LSB.

If the scaled sample level is greater than +3.96875, a +3 symbol level is decoded with the sample error capped at +0.96875. Likewise if the scaled sample level is less than –4.0, a -3 symbol level is decoded with the sample error capped at –1.0.

Voice Data

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	2's complement encoded voice data															

This word holds the next voice signal to the DAC path. This is sampled voice data to be output to the audio output during a voice based signal reception or to drive the modulator outputs during a voice based signal transmission.

This word holds the current sampled and filtered voice signal from the ADC path. This may be the voice input from the selected microphone input during transmission, or the extracted (by band pass filtering) voice signal from the FM discriminator input during receive.

FFSK Data

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFSK/MSK	MS Data Byte								LS Data Byte							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

This word holds the next 2 bytes of FFSK/MSK data or the next 8 C4FM/CQPSK symbols to be transmitted. Outgoing data is treated as continuous. If new data is not provided before the current data has been transmitted, the current data will be re-transmitted, until new data is provided. Transmission of the current word of data will be completed before transmission of the new data begins.

Data Padding

The most significant bit of FFSK/MSK data is transmitted first. The most significant symbol of C4FM/CQPSK data is transmitted first. Bits or symbols beyond the actual data message length should be padded with innocuous values (system dependent). In the C4FM case an innocuous symbol sequence may be "+3, +3, -3, -3, …" and in the FFSK case an innocuous bit sequence may be all '1's. The modulator outputs can be ramped down whilst transmitting this data padding.

1.6 Application Notes

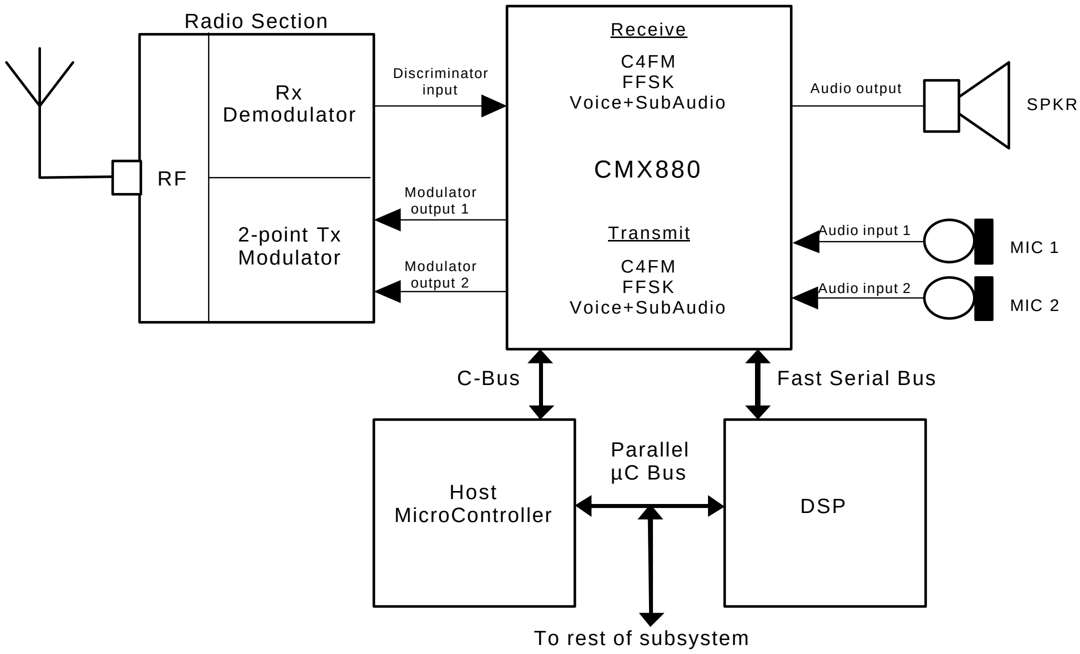


Figure 22 Possible APCO 25 Configuration

1.7 Performance Specification

1.7.1 Electrical Performance

The performance data are target figures, that may change subject to the outcome of device evaluation.

Absolute Maximum Ratings
Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply: V_{DD}(D)- V_{SS}(D)	–0.3	7.0	V
V_{DD}(A)- V_{SS}(A)	–0.3	7.0	V
Voltage on any pin to V_{SS}(D)	–0.3	V_{DD}(D) + 0.3	V
Voltage on any pin to V_{SS}(A)	–0.3	V_{DD}(A) + 0.3	V
Current into or out of V_{DD}(A), V_{SS}(A), V_{DD}(D) and V_{SS}(D)	–30	+30	mA
Current into or out of any other pin	–20	+20	mA
Voltage differential between power supplies:			
V_{DD}(D) and V_{DD}(A)	0	0.3	V
V_{SS}(D) and V_{SS}(A)	0	50	mV

D6 Package (SSOP)	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25°C		550	mW
... Derating		9	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

E1 Package (TSSOP)	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25°C		400	mW
... Derating		5.3	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Operating Limits
Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		2.7	5.5	V
Operating Temperature		–40	+85	°C
Clock/Xtal Frequency	11,12	15.3598464	15.3601536	MHz
	11,13	15.3584	15.3616	MHz

Notes:
11. Nominal clock frequency is 15.36MHz.
12. For APCO 25 digital channels, the clock frequency must be accurate to within 10ppm.
13. For analogue only channels, the accuracy can be relaxed to the accuracy required by the system.

Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 2;
Maximum load on digital outputs = 30pF;
Xtal Frequency = 15.36MHz ±0.01% (100ppm);
V_{DD} = 2.7V to 5.5V; Tamb = –40°C to +85°C;
Reference Signal Level = 308mV rms at 1kHz with V_{DD} = 5V;
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB;
Output stage attenuation = 0dB.

DC Parameters		Notes	Min.	Typ.	Max.	Units
Supply Current						
I_{DD}(D) (V_{DD} = 5.0V)		21		15.0	**TBD**	mA
I_{DD}(A) (V_{DD} = 5.0V)		21		3.0	**TBD**	mA
I_{DD}(D) (V_{DD} = 3.0V)		21		9.0	**TBD**	mA
I_{DD}(A) (V_{DD} = 3.0V)		21		2.0	**TBD**	mA
I_{DD}(D) (Power-saved)		21		**TBD**	**TBD**	µA
I_{DD}(A) (Power-saved)		21		**TBD**	**TBD**	µA
"C-BUS" and FSB Interfaces						
Input Logic "1"			70%			V_{DD}
Input Logic "0"					30%	V_{DD}
Input Leakage Current (Logic "1" or "0")			–1.0		1.0	µA
Input Capacitance			-		7.5	pF
Output Logic "1"	(I_{OH} = 120µA)		90%			V_{DD}
Output Logic "0"	(I_{OL} = 360µA)				10%	V_{DD}
"Off" State Leakage Current					10	µA
IRQN	(Vout = V_{DD}(D))		–1		1	µA
REPLY_DATA (output HiZ)			–1		1	µA
CLOCK_OUT						
Output Logic "1"	(I_{OH} = 120µA)		90%			V_{DD}
	(I_{OH} = 1mA)		80%			V_{DD}
Output Logic "0"	(I_{OL} = 360µA)				10%	V_{DD}
	(I_{OL} = -1.5mA)				15%	V_{DD}
CLOCK/XTAL		22				
Input Logic "1"			70%			V_{DD}
Input Logic "0"					30%	V_{DD}
Input current (Vin = V_{DD})					40	µA
Input current (Vin = V_{SS})			–40			µA
V_{BIAS}		23				
Output voltage offset wrt V_{DD}/2 (I_{OL} < 1µA)			-2%		+2%	V_{DD}
Output impedance				22		kΩ

Notes:

21. Not including any current drawn from the device pins by external circuitry. [max limit awaiting further device characterisation]
22. Characteristics when driving the CLOCK/XTAL pin with an external clock source.
23. Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2.

AC Parameters		Notes	Min.	Typ.	Max.	Units
CLOCK/XTAL Input						
'High' pulse width		31	25			ns
'Low' pulse width		31	25			ns
Input impedance (at 15.36MHz)						
Powered-up	Resistance			150		kΩ
	Capacitance			20		pF
Powered-down	Resistance			300		kΩ
	Capacitance			20		pF
Clock frequency				15.36		MHz
Clock stability/accuracy	(mixed or digital)	32			±10	ppm
	(analogue only)	33			±100	ppm
Clock start up (from power-save)				400		ms
V_{BIAS}						
Start up time (from power-save)				30		ms
Microphone Inputs 1 and 2 and FM Disc Input (MIC_1, MIC_2, FM_DISC)						
Input impedance		34		1		MΩ
Input signal range		35	10		90	$\%V_{DD}$
Feedback load resistance			80			kΩ
Amplifier open loop voltage gain (I/P = 1mV rms at 100Hz)				60		dB
Unity gain bandwidth				1.0		MHz

Notes:

31. Timing for an external input to the CLOCK/XTAL pin.
32. This is the clock accuracy required when using the CMX880 in C4FM digital or mixed digital/analogue modes in order to meet the APCO 25 TSB102.CAAB, Digital C4FM/CQPSK Transceiver Performance Recommendations.
33. This clock accuracy is required when using the CMX880 in analogue only modes.
34. With no external components connected
35. After multiplying by gain of input circuit, with external components connected.

AC Parameters	Notes	Min.	Typ.	Max.	Units
CLOCK_OUT Output					
CLOCK/XTAL input to CLOCK_OUT timing:					
(in high to out high)	36		15		ns
(in low to out low)	36		15		ns
'High' pulse width	37	26	32.5	39	ns
'Low' pulse width	37	26	32.5	39	ns
Modulator Outputs 1 and 2 and Audio Output (MOD_1, MOD_2, AUDIO)					
Power-up to output stable	38		50	100	µs
Modulator Attenuators					
Attenuation (at 0dB)		–0.5	0	0.5	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		–1.6		1.6	dB
Output Impedance Enabled	39		600		Ω
Output Impedance Disabled	39		500		kΩ
Audio Attenuator					
Attenuation (at 0dB)		–0.2	0	0.2	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		–0.6		0.6	dB
Output Impedance Enabled	39		600		Ω
Output Impedance Disabled	39		500		kΩ
Feedback load resistance		80			kΩ
Amplifier open loop voltage gain (I/P = 1mV rms at 100Hz)			60		dB
Unity gain bandwidth			1.0		MHz

Notes:

36. CLOCK/XTAL input driven by external source such as a temperature compensated crystal oscillator (TCXO).
37. 15.36MHz XTAL fitted.
38. Power-up refers to issuing a "C-BUS" command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and "C-BUS" interface, to be in placed in power-save mode.
39. Small signal impedance, at V_{DD} = 5.0V and Tamb = 25°C.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Units
Auxiliary RSSI Monitor					
8 Bit ADC Mode					
Resolution			8		Bits
Input Range	41	V_{SS}(A)		V_{DD}(A)	V
Conversion time	42		12.5		µs
Input impedance					
Resistance			10		MΩ
Capacitance			5		pF
Zero error (input offset to give ADC output = 0)		–20		+20	mV
Input rate of change	43			1.1	mV/µs
Integral Non-linearity				2.0	LSB
Differential Non-linearity	44			1.0	LSB
Source output impedance	45			24	kΩ
Level Threshold Detect Mode					
Threshold Resolution			8		Bits
Upper threshold range (VTH)	46	VTL		V_{DD}(A)	V
Lower threshold range (VTL)	46	V_{SS}(A)		VTH	V
RSSI change to IRQ	47			120	µs
RSSI change to Receiver-Turn-On	48			60	µs

Notes:

41. At V_{DD} = 5.0V only. Signal levels and currents are proportional to V_{DD}.
42. With clock frequency of 15.36MHz. Conversion time is dependent on A-to-D clock frequency.
43. Linear rate of change of input to ensure < 1 bit error.
44. Guaranteed monotonic with no missing codes.
45. Denotes output impedance of the driver of the RSSI input, to ensure < 1 bit additional error under nominal conditions.
46. Upper threshold > Lower threshold
47. Time from RSSI rising above Upper Threshold or falling below Lower Threshold, to IRQN being asserted.
48. Time from RSSI rising above Upper Threshold to receiver path powering up, settling and starting automatic signal type identification.

AC Parameters (cont.)		Notes	Min.	Typ.	Max.	Units
Receiver Signal Type Identification						
Probability of correctly identifying signal type	(SNR = 12dB)			>>99.9		%
CTCSS Detector						
Sensitivity	(Pure Tone)	51		-26		dB
Response Time	(Composite Signal)	52		140	250	ms
De-response Time	(Composite Signal)	52		145		ms
Frequency Range			60		260	Hz
SELCALL Detector						
Sensitivity	(Pure Tone)	53		-26		dB
Response Time	(Good Signal)			14		ms
De-response Time	(Good Signal)			22		ms
Frequency Range	(Selcall)		300		3000	Hz
DCS Decoder						
Sensitivity		51	58			mVp-p
Bit-Rate Sync Time				2		edges
FFSK/MSK Decoder						
Signal Input Dynamic Range	(SNR = 50dB)	54	100	230	1000	mVrms
Bit Error Rate		54				
	(SNR = 12dB at 1200 baud)			2.5		10^{-4}
	(SNR = 12dB at 2400 baud)			1.5		10^{-3}
	(SNR = 20dB at 1200/2400 baud)			<1		10^{-8}
Receiver Synchronisation	(SNR = 12dB)					
	Probability of bit 16 being correct			>99.9		%
C4FM Decoder						
Input Signal Level		55			1000	mVrms
DC Offset wrt V_{DD} /2		55	-50		+50	mV
Symbol Rate				4800		S/s
Maximum Symbol Rate Drift		56		40		ppm
Bit Error Rate	(SNR = 12dB)	57		4		10^{-4}
	(SNR = 16dB)	57		2		10^{-6}

Notes:

51. Sub-Audio Detection Level threshold set to 16mV.
52. Composite signal = 308mV rms at 1kHz + 75mV rms Noise + 31mV rms Sub-Audio signal. Noise bandwidth = 5kHz Band Limited Gaussian.
53. Selcall Tone Detection Level threshold set to 16mV.
54. For a “101010101 ... 01” pattern. See Figure 25 and Figure 26 for variation of BER with SNR and with input signal level.
55. For optimum performance, measured at FM_DISC input pin, for a “+3 +3 –3 –3 ...” symbol sequence, with V_{DD} = 5V and the Unit Level set to 2048. The optimum levels and DC offset values are proportional to V_{DD}.
56. The CMX880 will track and decode received symbol sequences with up to this symbol rate error wrt to the local clock. BER increases by ~10^{-4} per 10ppm drift, at SNR = 12dB.
57. See graph shown in Figure 27. Noise Bandwidth = bit rate bandwidth (bit rate bandwidth = 2 × C4FM symbol rate = 0 to 9600Hz).

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Units

CTCSS Encoder					
Frequency Range		60.0		260	Hz
Tone Frequency Resolution				0.2	%
Tone Amplitude Tolerance	61	-1.0		+1.0	dB
Total Harmonic Distortion	62		2.0	4.0	%
Selcall Encoder					
Frequency Range		300		3000	Hz
Tone Frequency Resolution				0.2	%
Tone Amplitude Tolerance	65	-1.0		+1.0	dB
Total Harmonic Distortion	62		2.0	4.0	%
DTMF Encoder					
Output signal level High tone			0		dB
Low tone (twist on)	66		-2		dB
(twist off)	66		0		dB
Output distortion			2	5	%
DCS Encoder					
Bit Rate			134.4		bits/s
Amplitude Tolerance	61	-1.0		+1.0	dB
FFSK/MSK Encoder					
Output signal level			775		mVrms
Output level variation		-1.0		+1.0	dB
Output distortion				5	%
3rd harmonic distortion				3	%
Logic 1 freq 1200baud and 2400baud		1198	1200	1202	Hz
Logic 0 freq 1200baud		1798	1800	1802	Hz
2400baud		2398	2400	2402	Hz
Isochronous distortion (0 to 1 and 1 to 0)				40	µs
C4FM Encoder					
Output signal level	63			1000	mVrms
Output DC offset wrt $V_{DD}/2$	63	-50		+50	mV
Symbol Rate			4800		S/s
Symbol Rate Drift	64			10	ppm
CQPSK Encoder					
Output signal level	63			1000	mVrms
Output DC offset wrt $V_{DD}/2$	63	-50		+50	mV
Symbol Rate			4800		S/s
Symbol Rate Drift	64			10	ppm

Notes:
61. $V_{DD}(A)$ = 5.0V and TX Sub-Audio Level set to 88mV p-p (31mV rms).
62. Measured at MOD_1 or MOD_2 output.
63. Measured after external RC filter (R10,C12/R11,C13) for a "+3 +3 –3 –3 ..." symbol sequence, with V_{DD} = 5V and the Unit Level set to 2048. The output levels are proportional to V_{DD}.
64. Dependant on crystal or clock accuracy.
65. $V_{DD}(A)$ = 5.0V and TX Selcall Level set to 881mV p-p (308mV rms).
66. With respect to High Tone

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Units
Analogue Channel Audio Filtering					
Pass-band (nominal bandwidth):					
Received voice	71	300		3000	Hz
12.5kHz channel transmitted voice	72	300		3000	Hz
25kHz channel transmitted voice	73	300		2550	Hz
Pass-band Gain (at 1.0kHz)			0		dB
Pass-band Ripple (wrt gain at 1.0kHz)		-2		+0.5	dB
Stop-band Attenuation		33.0			dB
Residual Hum and Noise	78		-50		dBp
Pre-emphasis	74		6		dB/oct
De-emphasis	75		–6		dB/oct
Digital (APCO 25) Channel Audio Filtering					
Band Pass filtering (TX)	76				
Voice from MIC input (nominal bw)		200		3300	Hz
Pass-band Gain (at 1.0kHz)			0		dB
Pass band ripple (wrt gain at 1kHz)		–2		1	dB
Low Pass filtering (RX)	77				
Voice to Audio output (nominal bw)		0		3300	Hz
Pass-band Gain (at 1.0kHz)			0		dB
Pass band ripple (wrt gain at 1.0kHz)		–1		2	dB

Notes:

71. The receiver voice filter complies with the characteristic shown in Figure 5. The high pass filtering removes sub-audio components from the audio signal.
72. The 12.5kHz channel filter complies with the characteristic shown in Figure 13
73. The 25kHz channel filter complies with the characteristic shown in Figure 12
74. The pre-emphasis filter complies with the characteristic shown in Figure 14.
75. The de-emphasis filter complies with the characteristic shown in Figure 6.
76. The high pass filtering part of the band pass is implemented by the microphone input filter components defined in section 1.4. The Tx voice filter complies with the characteristic shown in Figure 17.
77. The Rx voice filter complies with the characteristic shown in Figure 10.
78. dBp represents a psophometrically weighted measurement.

“C-BUS” Timing

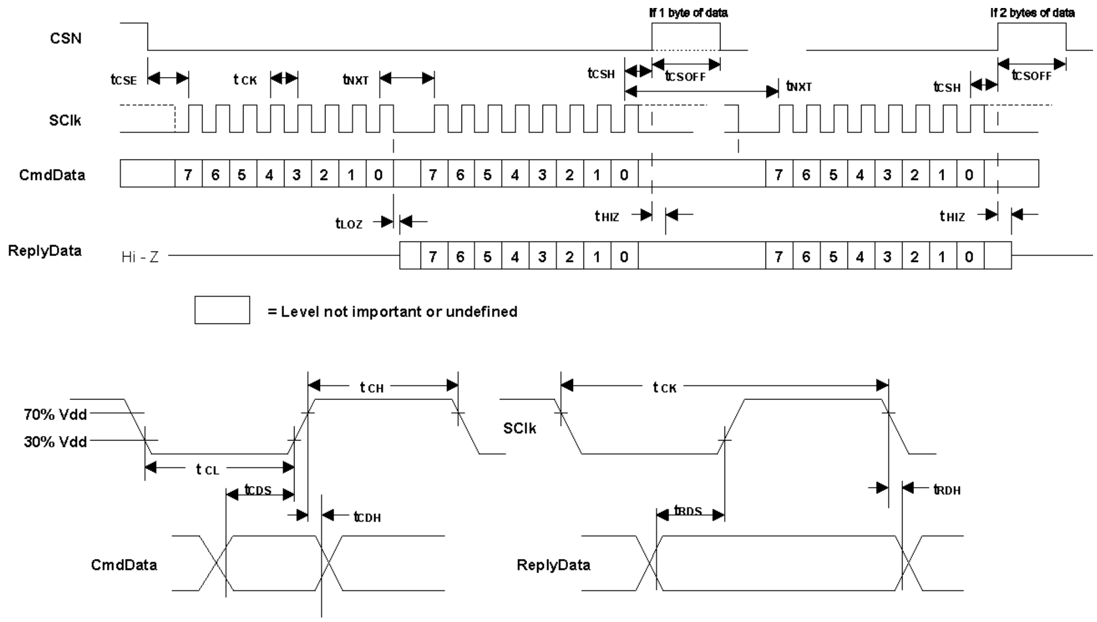


Figure 23 “C-BUS” Timing

“C-BUS” Timing		Notes	Min.	Typ.	Max.	Units
t_{CSE}	CSN Enable to SClk high time		100			ns
t_{CSH}	Last SClk high to CSN high time		100			ns
t_{LOZ}	SClk low to ReplyData Output Enable Time		0.0			ns
t_{HIZ}	CSN high to ReplyData high impedance				1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0			µs
t_{NXT}	Inter-byte time		200			ns
t_{CK}	SClk cycle time		200			ns
t_{CH}	SClk high time		100			ns
t_{CL}	SClk low time		100			ns
t_{CDS}	Command Data setup time		75			ns
t_{CDH}	Command Data hold time		25			ns
t_{RDS}	Reply Data setup time		50			ns
t_{RDH}	Reply Data hold time		0			ns

Maximum 30pF load on each C-BUS interface line.

Notes:
1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. REPLY DATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SERIAL_CLOCK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats “C-BUS” compatible ICs are able to work with SERIAL_CLOCK pulses starting and ending at either polarity.

These timings are for the latest version of “C-BUS”, and allow faster transfers than the original “C-BUS” timings given in CML Publication D/800/Sys/3 July 1994. The CMX880 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

Fast Serial Bus Timing

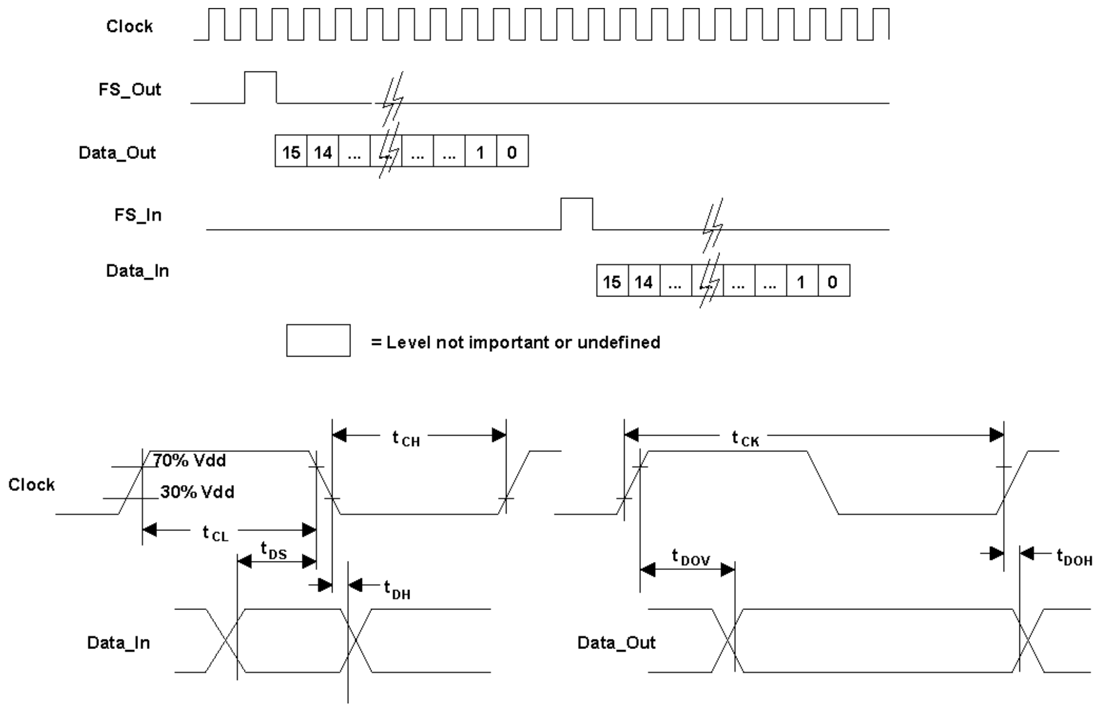


Figure 24 Fast Serial Bus Timings.

Fast Serial Bus Interface Timing		Notes	Min.	Typ.	Max.	Units
t_{CK}	Clock cycle time	1		260		ns
t_{CL}	Clock 'low' pulse width		100			ns
t_{CH}	Clock 'high' pulse width		100			ns
t_{DOV}	Out data valid time				50	ns
t_{DOH}	Out data hold time		0			ns
t_{DS}	In data set up time		50			ns
t_{DH}	In data hold time		0			ns

Maximum 30pF load on each FSB interface line.

Notes: 1. The FSB clock frequency is a quarter of the CLOCK/XTAL frequency.

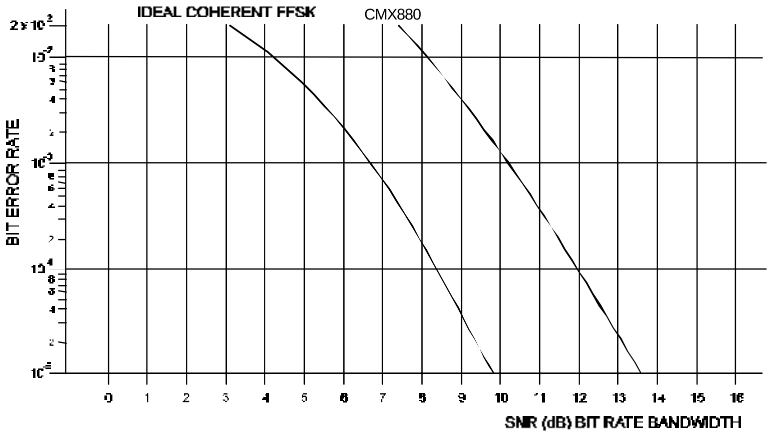


Figure 25 Typical FFSK/MSK Bit Error Rate Graph

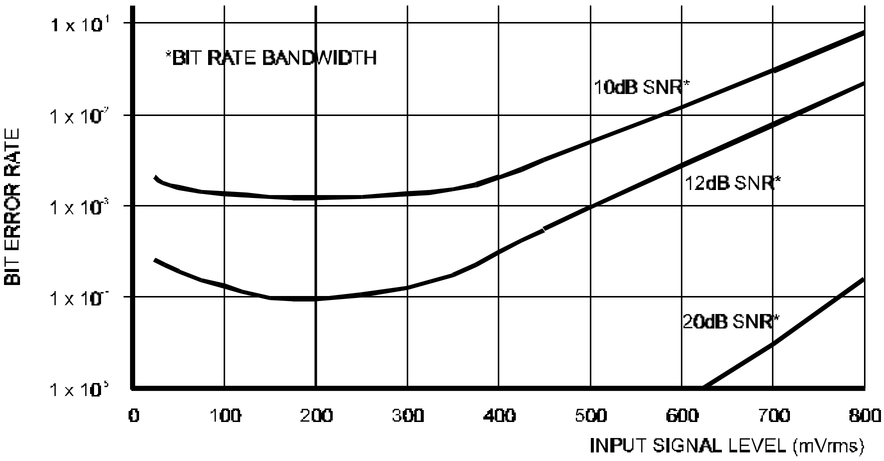


Figure 26 FFSK/MSK Typical Variation of Bit Error Rate with Input Signal Level

C4FM Receiver Bit Error Rates

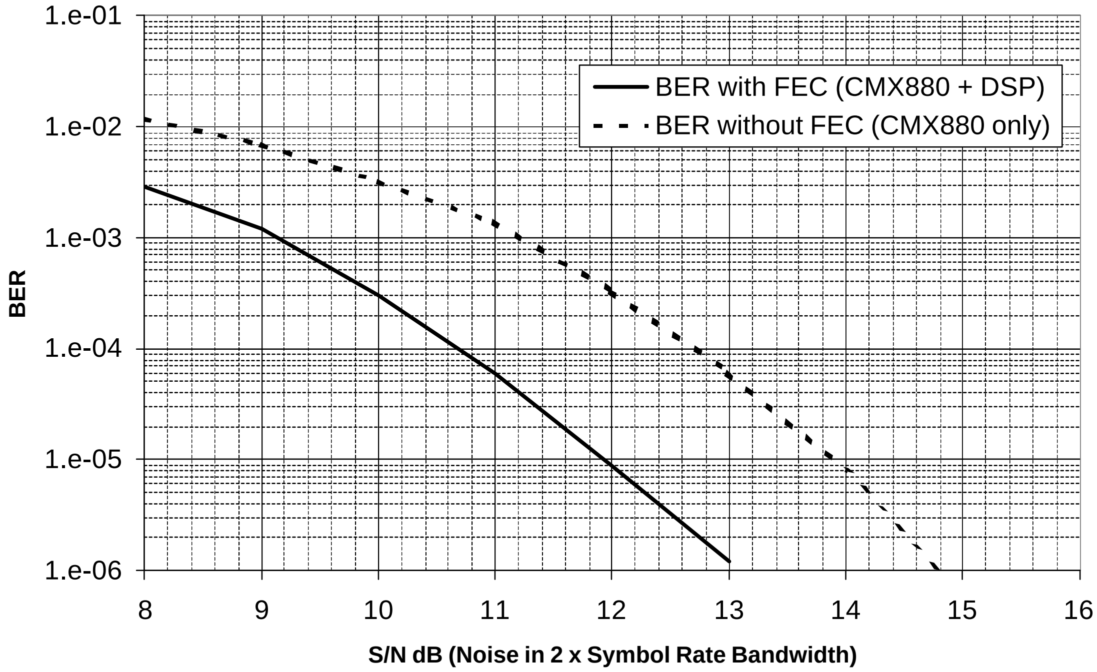


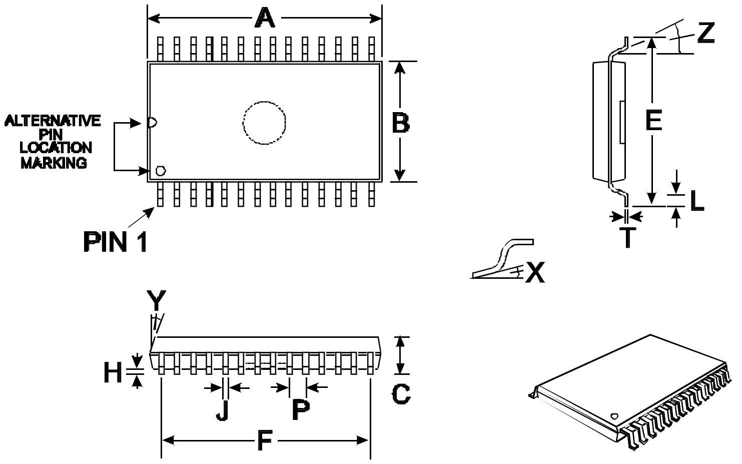
Figure 27 Typical Bit Error Rate with and without FEC

The Bit Error Rate (BER) performance shown in Figure 27 is measured under nominal working conditions, with pseudo-random data. The graph shows the BER of the CMX880 (which is without FEC), and also the BER that is expected to be attainable when the CMX880 is used in conjunction with a DSP performing error correction. This will depend on the DSP error correction algorithm performance.

Note: S/N calculated as $20 \times LOG_{10}$(Signal Voltage $\div$ Noise Voltage), where:

- Signal Voltage is the measured rms voltage of a random 4-level signal.
- Noise Voltage is the rms voltage of a flat Gaussian noise signal having a bandwidth from a few Hz to twice the symbol rate (9600Hz).
- Both signals are measured at the same point in the test circuit.

1.7.2 Packaging



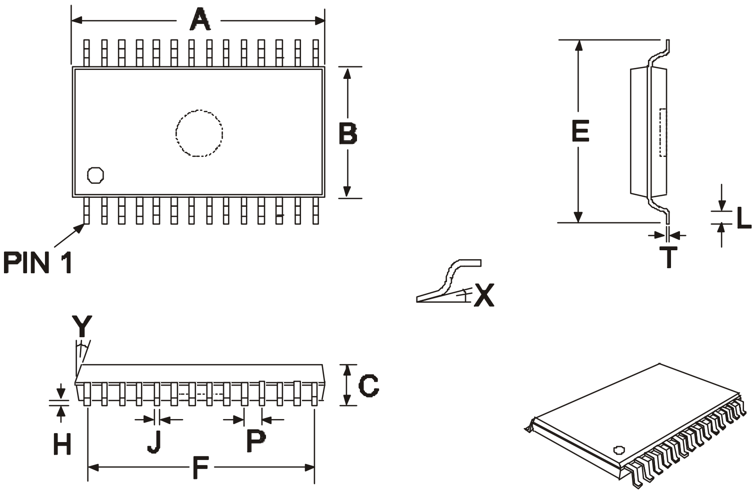
DIM.	MIN.	TYP.	MAX.
* A	0.396 (10.06)		0.407 (10.34)
* B	0.205 (5.21)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
F		0.333 (8.45)	
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.56)		0.037 (0.94)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.23)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 28 Mechanical Outline of 28-pin SSOP (D6): Order as part no. CMX880D6



DIM.	MIN.	TYP.	MAX.
* A	0.378 (9.60)		0.386 (9.80)
* B	0.169 (4.30)		0.177 (4.50)
C	--------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
F		0.333 (8.45)	
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.026 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
X	0°		7°
Y		12°	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 29 Mechanical Outline of 28-pin TSSOP (E1): Order as part no. CMX880E1

Consumer Microcircuits Limited
COMMUNICATION SEMICONDUCTORS

Oval Park - LANGFORD
MALDON - ESSEX
CM9 6WG - ENGLAND

Telephone: +44 (0)1621 875500
Telefax: +44 (0)1621 875600
e-mail: sales@cmlmicro.co.uk
http://www.cmlmicro.co.uk