BURR-BROWN®

MP32

FOR A COMPLETE DATA SHEET, SEE PDS-424B

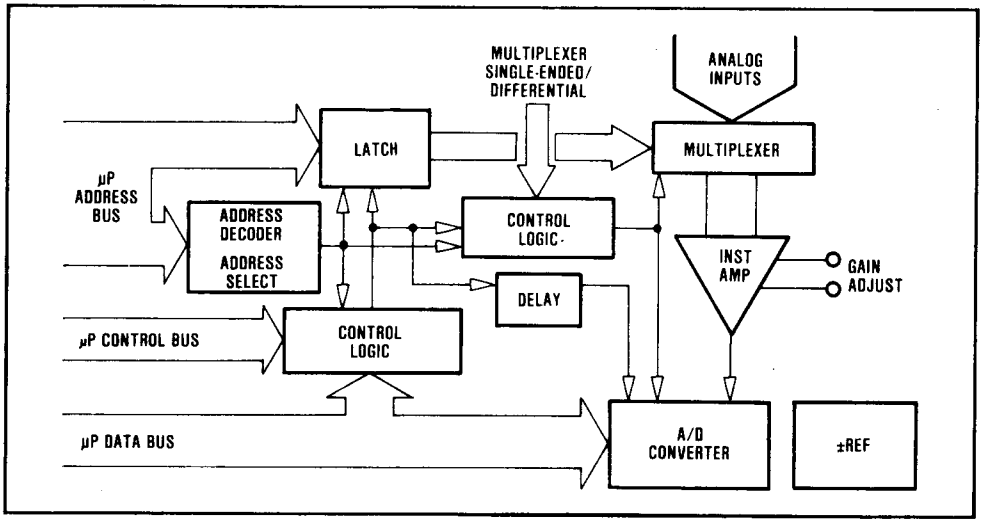
Microprocessor-Interfaced 12-BIT DATA ACQUISITION SYSTEM

FEATURES

- **INTERFACES WITH SEVERAL MICROPROCESSOR TYPES WITHOUT ADDITIONAL COMPONENTS**
- **COMPATIBLE WITH SEVERAL MINICOMPUTERS**
- **EASY TO PROGRAM**
  - **One instruction acquires data as a memory-mapped device**
  - **Two instructions acquire data as an accumulator I/O device**

DESCRIPTION

The MP32 is a complete analog input system and interfaces to many microprocessors without additional external components. Contained in an 80-pin quad-in-line package, it includes a 12-bit CMOS A/D converter, instrumentation amplifier, input multiplexer that accepts up to 16 single-ended signals or 8 differential signals, an addess decoder, and control logic. Logic to generate interrupt, halt, and direct memory access request signals is also included. The system can digitize low level or high level analog signals. Gain of the internal instrumentation amplifier can be programmed with a single external resistor allowing input ranges as low as ±10mV.



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DESCRIPTION (CONT)

ANALOG MULTIPLEXERS

Two 8-channel CMOS analog multiplexers are used on the input which permits selection of 16 single-ended or 8 differential inputs. A 16-channel pseudo-differential mode of operation can also be achieved by connecting the amplifier's inverting input to a common, remote signal ground. Channels are addressed by the address decoder which is connected directly to the microprocessor address bus. The number of input channels can be expanded without limit using external multiplexers.

INSTRUMENTATION AMPLIFIER

The instrumentation amplifier is a low drift, differential amplifier featuring high speed at gains above unity and gain programming with an external resistor. Gain may be selected from unity to 500.

ANALOG-TO-DIGITAL CONVERTER

The 12-bit A/D converter is a CMOS, successive approximation device with 40μsec conversion time and three-state outputs. Laser-trimmed, compatible thin-film networks are used to assure linearity and stability over wide temperature ranges.

ADDRESS DECODER

The 12-bit address decoder has been included in the MP32 so the device can be uniquely specified within 4k bands of the address field. If further decoding is required, the chip select (CS) pin can provide a 13th bit or the output of an external decoder can be connected to the internal address decoder output "wired-AND" node.

DELAY TIMER

A time delay between channel selection and start of conversion is built into the MP32 and is described in detail in the Analog Input Configuration section.

CONTROL LOGIC

The control logic generates signals to halt or interrupt the CPU while conversion takes place and to signal the CPU when conversion is complete and data can be read. Enable signals are also generated to gate the data onto the data bus.

REFERENCE

The internal voltage reference of the MP32 has been optimized for stable outputs with respect to temperature. Output current up to 2mA can be drawn externally from the reference outputs.

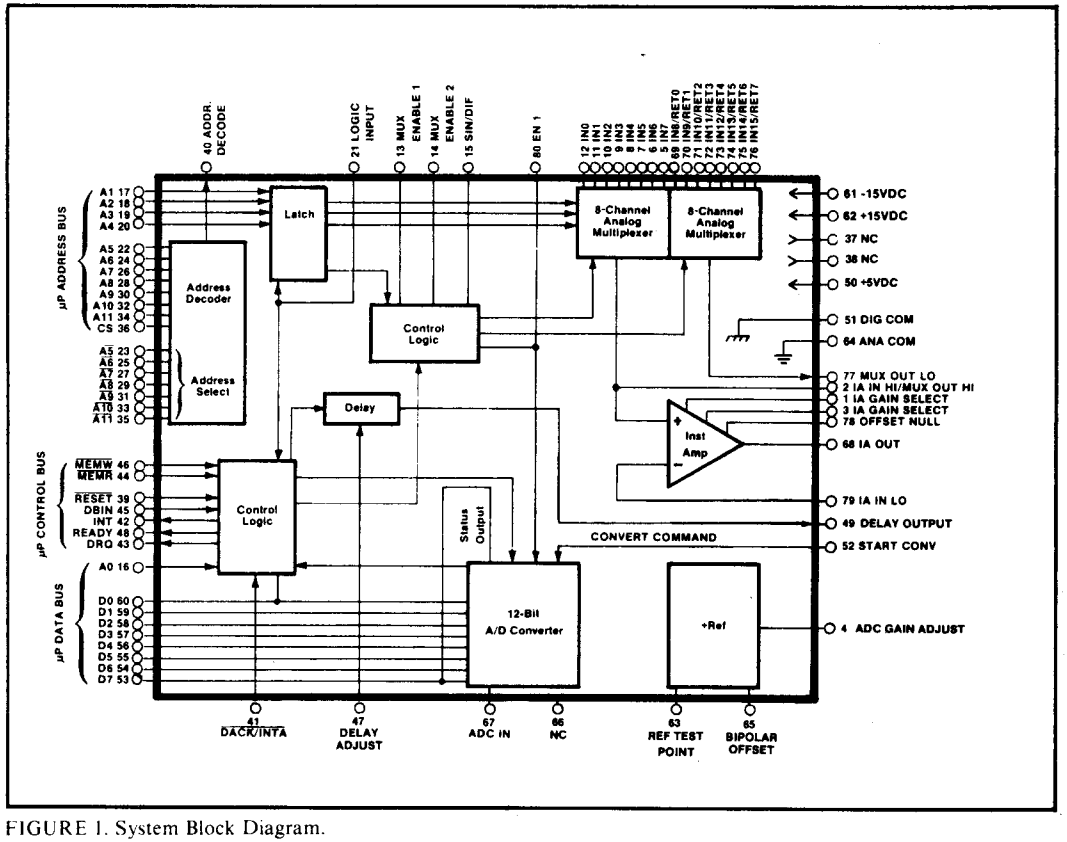


FIGURE 1. System Block Diagram.

SPECIFICATIONS

ELECTRICAL

Typical at +25°C and rated supplies unless otherwise noted.

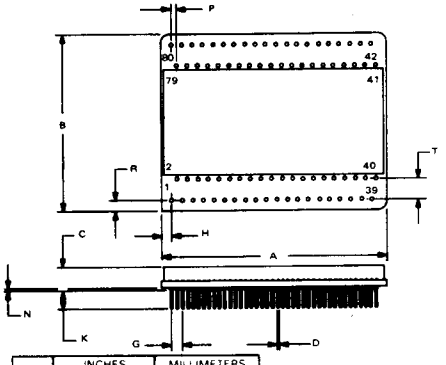
MODEL	MP32BG AND MP32CG MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS				
Resolution[1]	12	12	12	Bits
Number of Channels		16 Single-ended/8 Differential		
Throughput Rate[1] at G = 1	50	70	80	µsec/Channel
ANALOG INPUT/OUTPUT				
ADC Voltage Input Ranges[2]				
Bipolar[3]		±10		V
Unipolar[1]		0 to +10		V
Amplifier Gain Range		1 to 500		V/V
Gain Equation		1 + (25kΩ/R_{EXT})		
Input Voltage Without Damage			±35	V
Input Voltage for Multiplexer Operation			±10	V
Input Impedance				
Off Channel			10^{18}	Ω
On Channel		1.5	1.8	kΩ
Bias Current				
+25°C			300	nA
0°C to +70°C			400	nA
Amplifier Output Noise G = 100, R_S = 1500Ω		1.2		mV, rms
		7.0		mV, p-p
Amplifier Input Offset		±0.5	±7.0	mV
Amplifier Input Offset Drift (R_{source} = 1.5kΩ max)		±[7 + (90/G)]	±[26 + (190/G)]	µV/°C
Amplifier Gain Drift, (R_{EXT} ≤ 10ppm/°C)				
G = 1			±10	ppm/°C
G = 10			±110	ppm/°C
G = 100			±120	ppm/°C
G = 500			±120	ppm/°C
Amplifier Settling Time to ±0.01% of FSR				
G = 1[1]			15	µsec
G = 10		20		µsec
G = 100		25		µsec
G = 500		100		µsec
CMRR for Differential Inputs DC to 60Hz	80	84		dB
Instrumentation Amplifier				
Power Supply Sensitivity			[1 + (2/G)] 10^{-4}	% FSR/%ΔV
ACCURACY				
System RSS Accuracy[4] at 25kHz Throughput				
G = 1, BG			±0.05	
CG			±0.025	
Linearity, BG			±0.025	% FSR
CG			±0.0125	% FSR
Differential Linearity, BG		±0.025		% FSR
CG		±0.0125		% FSR
Gain Error		Adjustable to Zero		
Offset Error		Adjustable to Zero		
System RSS Accuracy at 1kHz Throughput				
G = 500			±0.39	%FSR
ADC Accuracy Drift				
Linearity			±3	ppm/°C
Gain			±10	ppm/°
Reference Drift				
Ref Out (Pin 63)			±15	ppm/°C
Bipolar Offset (Pin 65)			±25	ppm/°C
System Accuracy Drift (Excluding IA)				
Unipolar			±25	ppm/°C
Bipolar			±60	ppm/°C
No Missing Codes (-25°C to +85°C) (Bits 1 thru 12) CG		Guaranteed		
(Bits 1 thru 11) BG		Guaranteed		

ELECTRICAL (CONT)

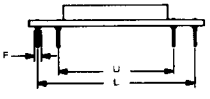
MODEL	MP32BG AND MP32CG			
	MIN	TYP	MAX	UNITS
Power Supply Sensitivity (Excluding IA)				
±15VDC			±0.008	% FSR/%ΔV
+5VDC			±0.0002	% FSR/%ΔV
DIGITAL INPUT/OUTPUT				
Biopolar Code		Bipolar Offset Binary		
Unipolar Code		Unipolar Straight Binary		
Logic Loading Pin (21)			3LSTTL	
Logic Loading Pin (60)			2LSTTL	
All Other Digital Inputs			1LSTTL	
Output Drive	1TTL Load			
Analog Input Channels Selected By:		A1-A4		
Output Data		D0-D7		
POWER REQUIREMENTS				
Rated Power Supply Voltages(1)		±15, +5		VDC
Power Supply Ranges for Rated Accuracy		+4.75 to +5.25 and ±11.4 to ±15.75		VDC
Power Supply Operating Range (±15VDC only)	±10		±18	VDC
Supply Drain				
+15VDC		10	20	mA
-15VDC		15	20	mA
+5VDC		80	160	mA
Power Dissipation (at rated supplies)		700	1300	mW
TEMPERATURE RANGE				
Specification	-25		+85	°C
Operating	-40		+100	°C
Storage	-55		+125	°C

NOTES:
1. These parameters are 100% tested. 2. Input voltage must be kept 2V below supply voltage. 3. External amplifier required. 4. Gain and offset adjust to zero.

MECHANICAL



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.120	2.180	53.85	55.37
B	1.670	1.720	42.42	43.69
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.100 BASIC		2.54 BASIC	
K	.150	.250	3.81	6.35
L	1.500 BASIC		38.1 BASIC	
N	.002	.010	0.05	0.25
P	.050 BASIC		1.27 BASIC	
R	.100 BASIC		2.54 BASIC	
T	.200 BASIC		5.08 BASIC	
U	1.100 BASIC		27.94 BASIC	



NOTE
LEADS IN TRUE POSITION WITHIN 0.015" (0.38mm) R (@ MMC AT SEATING PLANE

Pin numbers shown for reference only. Numbers may not be marked on package

MATERIAL: Ceramic
WEIGHT: 32 grams (1.2 oz.
MATING CONNECTOR: 2350MC (set of four 20 pin strips

PIN ASSIGNMENTS

	Pin No.		
IA GAIN SELECT	1	41	$\overline{\text{DACK/INTA}}$
IA IN HI/MUX OUT HI	2	42	INT
IA GAIN SELECT	3	43	$\overline{\text{DRQ}}$
ADC GAIN ADJUST	4	44	$\overline{\text{MEMR}}$
IN7	5	45	$\overline{\text{DBIN}}$
IN6	6	46	$\overline{\text{MEMW}}$
IN5	7	47	DELAY ADJUST
IN4	8	48	READY
IN3	9	49	DELAY OUTPUT
IN2	10	50	+5VDC
IN1	11	51	DIG COM
IN0	12	52	START CONV
MUX ENABLE 1	13	53	D7 MSB
MUX ENABLE 2	14	54	D6
SIN/DIF	15	55	D5
A0	16	56	D4
A1	17	57	D3
A2	18	58	D2
A3	19	59	D1
A4	20	60	D0 LSB
LOGIC INPUT	21	61	-15VDC
$\overline{\text{A5}}$	22	62	+15VDC
$\overline{\text{A5}}$	23	63	REF TEST POINT
$\overline{\text{A6}}$	24	64	ANA COM
$\overline{\text{A6}}$	25	65	BIPOLAR OFFSET
$\overline{\text{A7}}$	26	66	NC
$\overline{\text{A7}}$	27	67	ADC IN
$\overline{\text{A8}}$	28	68	IA OUT
$\overline{\text{A8}}$	29	69	IN8/RET0
$\overline{\text{A9}}$	30	70	IN9/RET1
$\overline{\text{A9}}$	31	71	IN10/RET2
$\overline{\text{A10}}$	32	72	IN11/RET3
$\overline{\text{A10}}$	33	73	IN12/RET4
$\overline{\text{A11}}$	34	74	IN13/RET5
$\overline{\text{A11}}$	35	75	IN14/RET6
CHIP SELECT CS	36	76	IN15/RET7
NC	37	77	MUX OUT LO
$\overline{\text{NC}}$	38	78	OFFSET NULL
$\overline{\text{RESET}}$	39	79	IA IN LO
ADDR DECODE	40	80	EN1