ABRIDGED VERSION

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A TDK Group Company

SSI 32P4744
Read Channel with 1,7 ENDEC, 4-burst Servo

January 1996

DESCRIPTION

The SSI 32P4744 device is a high performance BiCMOS single chip read channel ICs that contain all the functions needed to implement a complete zoned recording read channel for hard disk drive systems. Functional blocks include the pulse detector, programmable filter, 4-burst servo capture, time base generator, and data separator with 1,7 RLL ENDEC. Data rates can be programmed using an internal DAC whose reference current is set by a single external resistor.

Programmable functions of the SSI 32P4744 device are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 32P4744 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

FEATURES

GENERAL:

- **DAC controlled programmable data rates up to 40 Mbit/s**
- **Complete zoned recording application support**
- **Low power operation - 425 mW typical @ 5V and 40 Mbit/s**
- **Bi-directional serial port for register access**
- **Register programmable power management (Sleep mode < 0.5 mA)**
- **Power supply range (4.5 to 5.5 volts)**
- **Small footprint 64-lead TQFP package**

PULSE DETECTOR:

- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Low Drift AGC hold circuitry**
- **Temperature compensated, exponential control AGC**

(continued)

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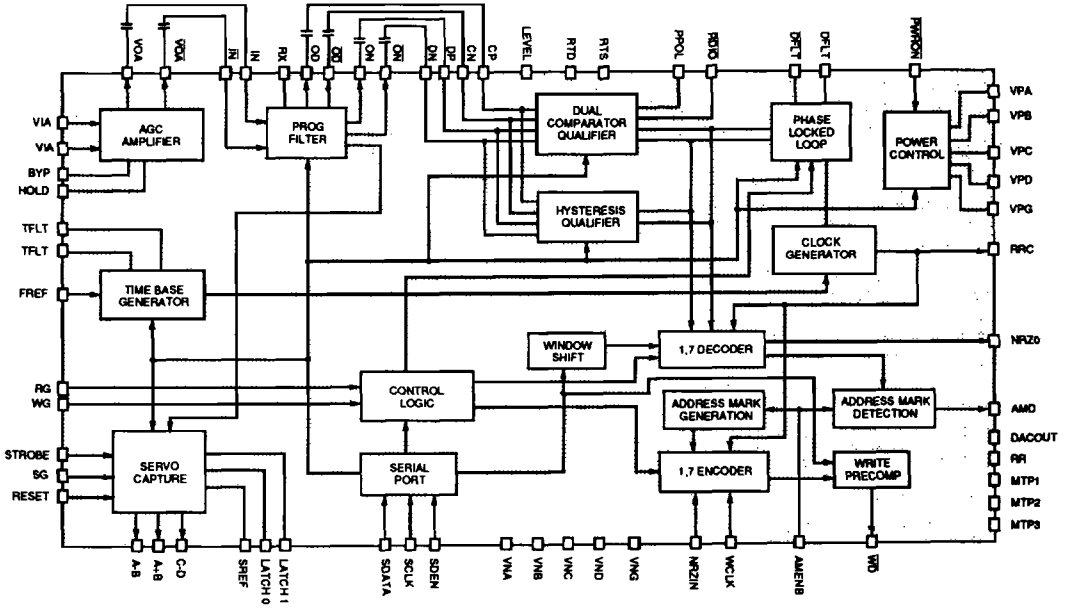
BLOCK DIAGRAM



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FEATURES (continued)

- Wide bandwidth, high precision full-wave rectifier
- Dual mode pulse qualification circuitry (user selectable)
- Programmable voltage qualification threshold level
- CMOS $\overline{\text{RDIO}}$ signal output for servo timing support
- Internal LOW-Z and fast decay timing
- 0.8 ns max. pulse pairing

SERVO CAPTURE:

- 4-burst servo capture with A-B, C-D, A+B outputs
- Internal hold capacitors
- Programmable charge current (4-bit DAC)
- Separate registers for fc and VTH during Servo mode
- 4-bit DAC for AGC level control (0.75 to 1 Vp-p)

PROGRAMMABLE FILTER:

- Programmable cutoff frequency from 6 to 18 MHz
- Programmable boost/equalization of 0 to 13 dB
- Matched normal and differentiated outputs
- ± 15% fc accuracy
- ± 2% maximum group delay variation
- Less than 1% total harmonic distortion
- Low-Z input switch
- No external filter components required

TIME BASE GENERATOR:

- Better than 1% frequency resolution
- Up to 75 MHz frequency output
- Independent M and N divide-by registers
- VCO center frequency matched to data synchronizer VCO

DATA SEPARATOR:

- Fast acquisition phase lock loop with zero phase restart technique
- Integrated 1,7 RLL Encoder/Decoder
- Fully integrated data separator
  - No external delay lines or active devices required
  - No external active PLL components required
- Programmable decode window symmetry control via serial port
  - Window shift control ± 34.5% (4-bit)
  - Includes delayed read data and VCO clock monitor points
- Programmable early/late write precomp (3-Bits each)
- Hard and soft sector operation
- VCO and Synchronized Read Data test points

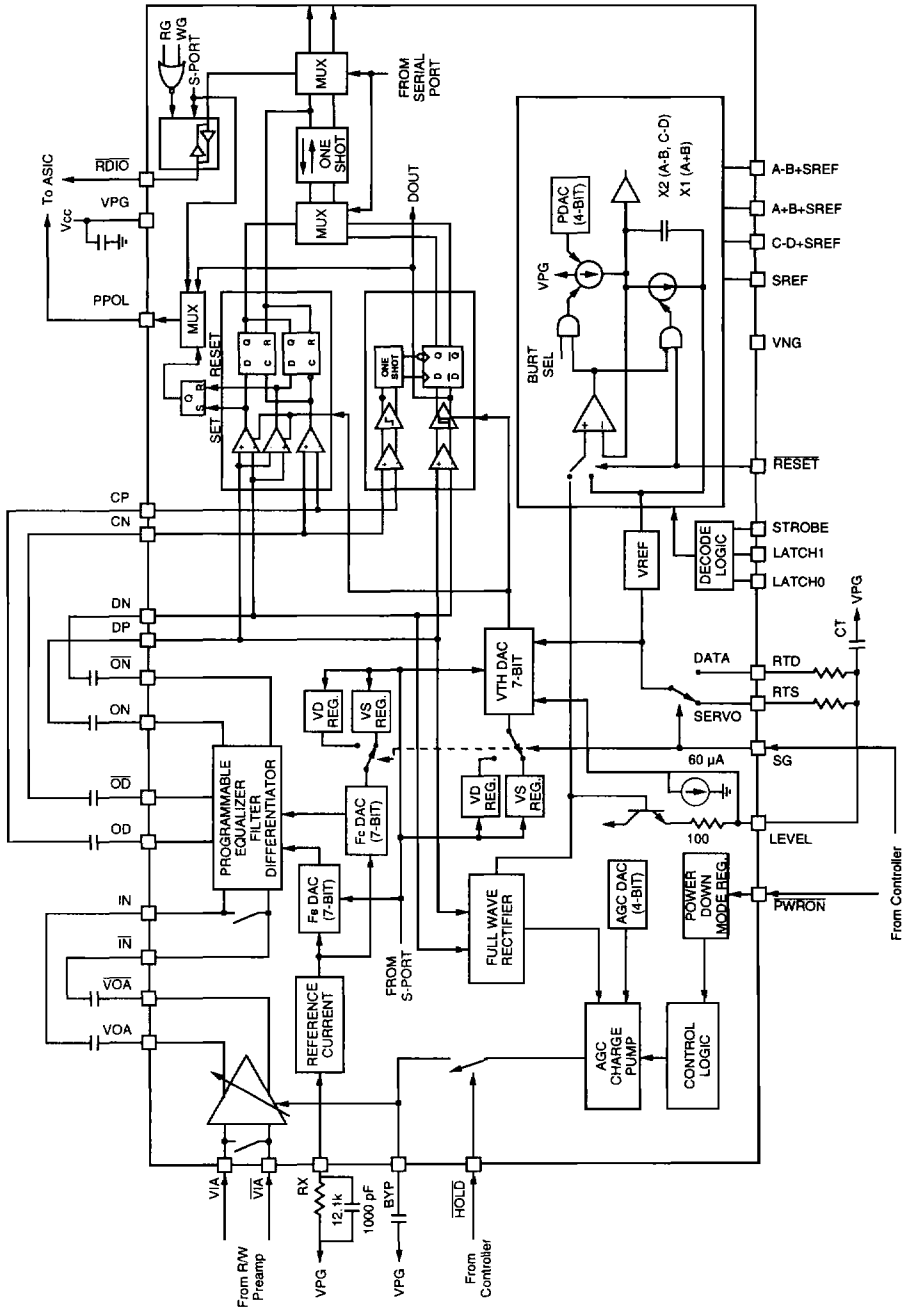


FIGURE 1A: 32P4744 Application Diagram Front End

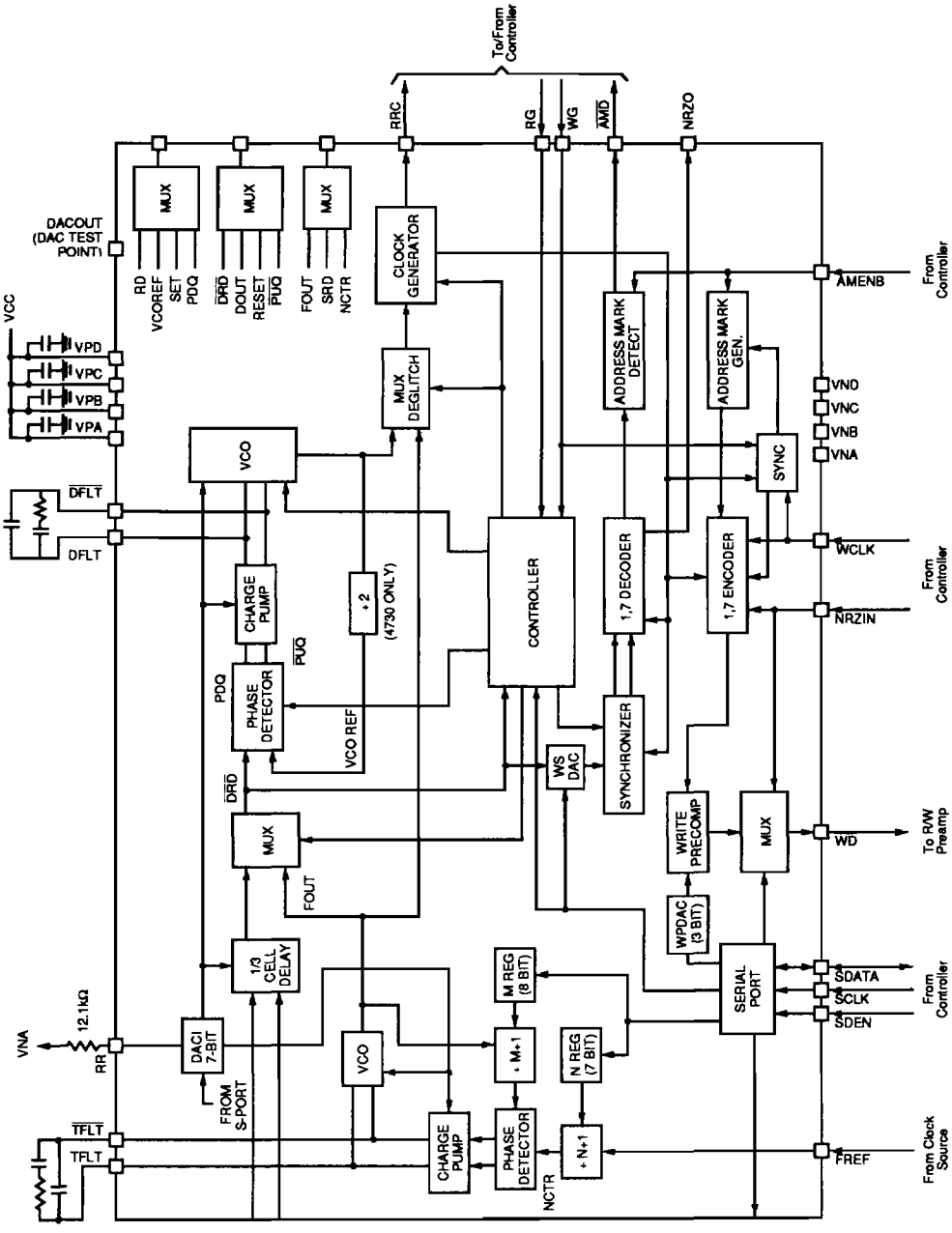
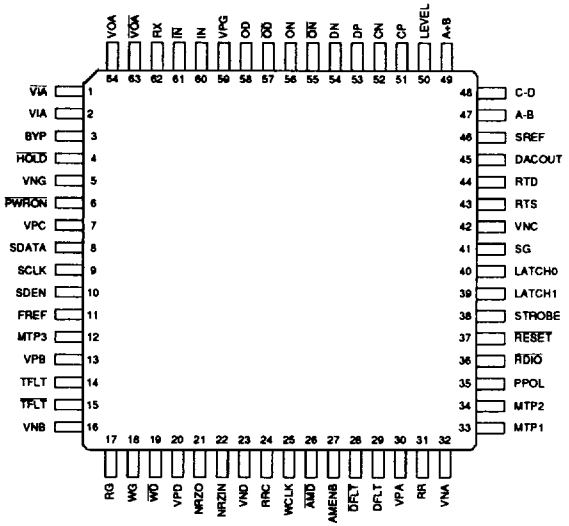


FIGURE 1B: 32P4744 Application Diagram Back End

PACKAGE PIN DESIGNATIONS

(Top View)



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

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ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32P4744	64-Lead TQFP	32P4744-CGT	32P4744-CGT
	68-Pin PLCC	32P4744-CH	32P4744-CH

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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