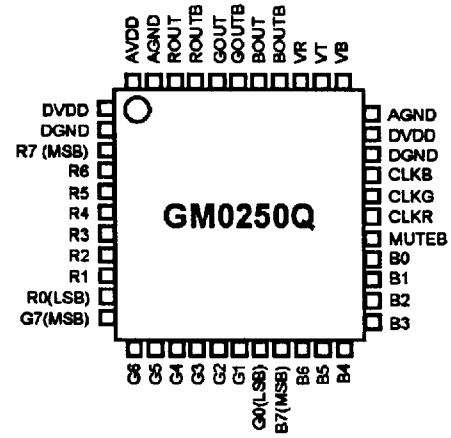
Description

The GM0250Q is a high speed low power 8bit 3 channel CMOS D/A converter combined with a high stability voltage reference fabricated on a single monolithic chip. Using high accuracy current cell, the nonlinearity and glitch energy are minimized. The analog output mismatching between each channels is within 2%. Advanced monolithic processing have made the GM0250Q the most accurate 8bit D/A converter available while keeping costs consistent with large volume integrated circuit production. The digital input level is applicable to both TTL and CMOS. This LSI is suitable for use of CD-I, HDTV, digital TV, Digital camcorder, and the other graphical display, etc.

Features

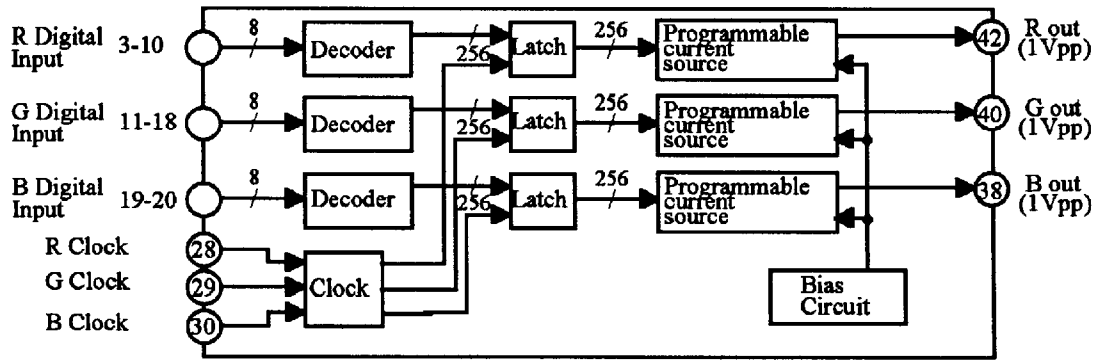
- Resolution : 8bit 3 channel
- Max. conversion speed : 50MHz(min.)
- Differential nonlinearity : ±0.5LSB
- Integral nonlinearity : ±0.5LSB
- Current output type : 13.2㎃ × 3 channel
- Analog output voltage : Vdd-1 to Vdd (75Ω load)
- Digital input voltage level : TTL, CMOS compatible
- Built in self bias circuit
- Power supply : +5V single
- Power consumption : 300mW(typ.)
- Package type : 44QFP

Pin Configuration



44QFP
(Top View)

Block Diagram



Absolute maximum ratings

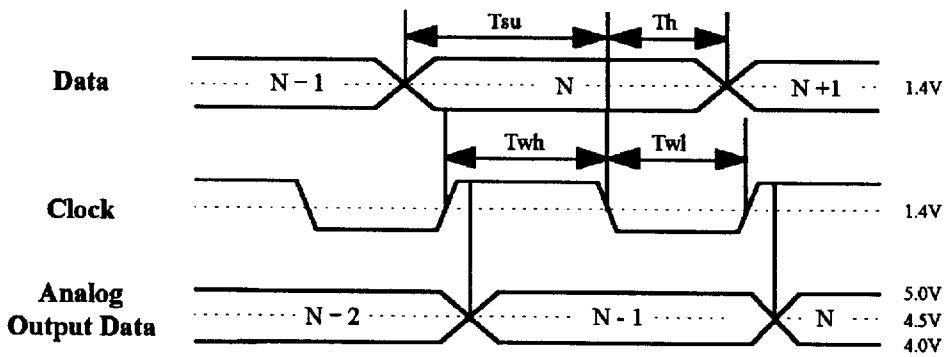
Characteristics	Symbol	Value		Unit
		Min	Max	
Supply voltage	AVDD, DVDD	-0.5	+7.0	V
Digital input voltage	R0 - R7 G0 - G7 B0 - B7 CLKR, G, B	DGND-0.5	DVDD+0.5	V
Operating temperature range	Topr	-20	+75	℃
Storage temperature range	Tstg	-55	125	℃
Power Dissipation	Pd		420	mW

Electrical Characteristics (V_{DD}=5V, Ta=25℃, R_O=75Ω, R_{ref}=3.3kΩ)

1. Analog Value

Item		Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage		V_{DD}	4.75	5.00	5.25	V
Current Dissipation		I_{DD}*		55	65	mA
Reference Current		I_{ref}	350	418	500	μA
Output Voltage Range	Ro = 75Ω	V_{out} 1				V
	Ro = 150Ω	V_{out} 2				V
Differential Non-Linearity		DNL			±0.5	LSB
Integral Non-Linearity		INL			±0.5	LSB
Conversion Speed		f_s	0.1		50	MSPS
Settling time		t_{set}		10		ns
Rising time		t_r			10	ns
Falling Time		t_f			10	ns
Channel Gain Error		A_{gain}		1.0	2.0	%
Crosstalk between channel		V_{crt}			- 40	dB

* f_{CLK} = 30MHz



2. Digital Value

Item		Symbol	Min.	Typ.	Max.	Unit
Data Inputs	Input Low Level	V_{IL}			0.8	V
	Input High Level	V_{IH}	2.0			V
Data Set up time		T_{su}			10	ns
Data Hold time		T_h			10	ns
Clock Inputs	Input Low Level	V_{IL}			1.0	V
	Input High Level	V_{IH}	2.0			V
Clock Low Duration		T_{wl}			10	ns
Clock High Duration		T_{wh}			10	ns

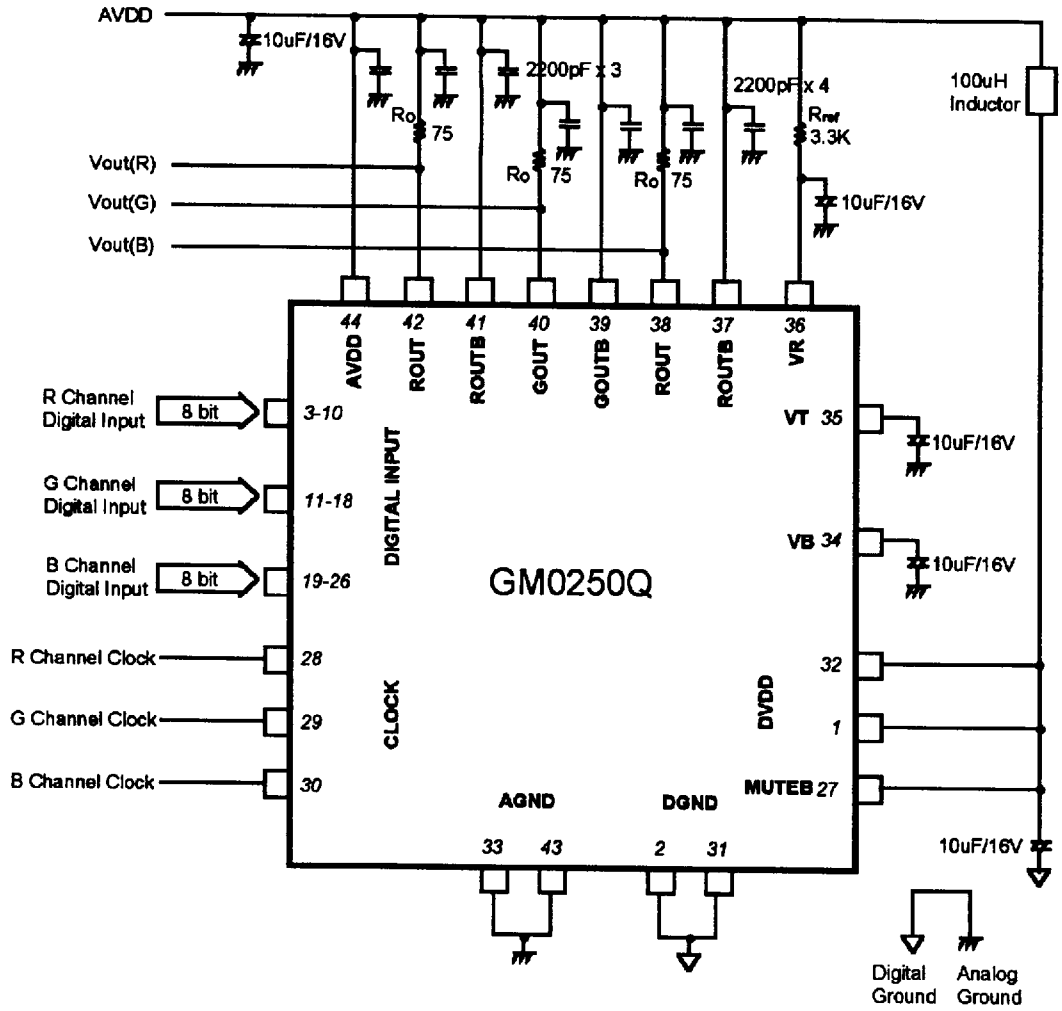
Pin description

Symbol	Pin	Function	Remark
R7 - R0	3 - 10	R Channel Digital input	LSB : R0
G7 - G0	11 - 18	G Channel Digital input	LSB : G0
B7 - B0	19 - 26	B Channel Digital input	LSB : B0
CLKR	28	R Channel Clock input	
CLKG	29	G Channel Clock input	
MUTEB	27	Picture Mute	Mute at Low
CLKB	30	B Channel Clock Input	
DVDD	1, 32	Digital power supply	
DGND	2, 31	Digital ground	
AVDD	44	Analog power supply	
AGND	43, 33	Analog ground	
VB	34	Bias voltage	
VT	35	Bias voltage	
VR	36	Bias voltage	
BoutB	37	Inverted output of B channel	
Bout	38	B channel analog output	
GoutB	39	Inverted output of G channel	
Gout	40	G channel analog output	
RoutB	41	Inverted output of R channel	
Rout	42	R channel analog output	

Analog Output Value Table (Vdd=5V, Ro=75Ω, Rref=3.3kΩ)

Code	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)	Vout(V)
0	0	0	0	0	0	0	0	0	4.000
1	0	0	0	0	0	0	0	1	4.004
. .	.	.	.	.	.	.	.	.	.
. .	.	.	.	.	.	.	.	.	.
. .	.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1	4.498
128	1	0	0	0	0	0	0	0	4.502
129	1	0	0	0	0	0	0	1	4.506
. .	.	.	.	.	.	.	.	.	.
. .	.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0	4.996
255	1	1	1	1	1	1	1	1	5.000

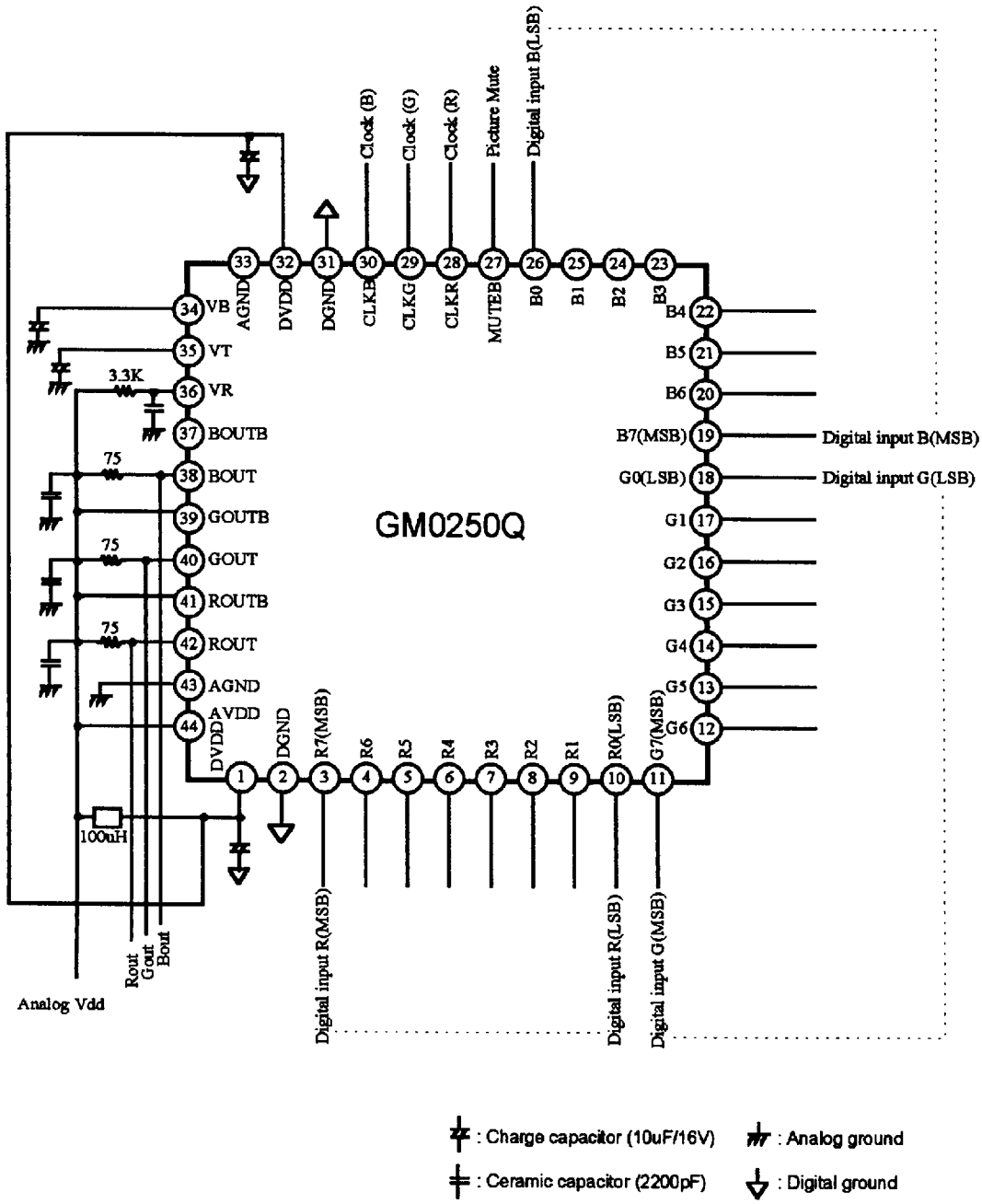
Application Circuit



NOTE)

1. AGND and DGND should be connected directly with the ground of Analog power source.
2. Protecting Latch-up, Analog power source and Digital power source should be used as one and 100uH inductor should be inserted between them like above circuit.
3. The resistor and capacitor which used in external circuit should be linked closely with IC pin as close as possible.
4. Power line and ground line should use wide pattern on the PCB.
5. Descriminating crosstalk, the shield line should be inserted among wires as possible.
6. To reduce error occured in high frequency operation, the ground line should be wired under GM0250Q on the PCB board and ground area should be wide.

Application circuit



: Charge capacitor (10uF/16V) : Analog ground

: Ceramic capacitor (2200pF) : Digital ground

Package Dimension

Unit : mm

M : MAX
m : MIN