Standard Products

UT8CR512K32 16 Megabit SRAM

Advanced Data Sheet
March 2005
www.aeroflex.com/4MSRAM

FEATURES

- ❑ 17ns maximum access time
- ❑ Asynchronous operation for compatibility with industry-standard 512K x 8 SRAMs
- ❑ CMOS compatible inputs and output levels, three-state bidirectional data bus
  - I/O Voltage 3.3 volts, 1.8 volt core
- ❑ Radiation performance
  - Intrinsic total-dose: 300 Krad(Si)
  - SEL Immune >100 MeV-cm^2/mg
  - LET_{th} (0.25): 53.0 MeV-cm^2/mg
  - Memory Cell Saturated Cross Section 1.67E-7cm^2/bit
  - Neutron Fluence: 3.0E14n/cm^2
  - Dose Rate
    - Upset 1.0E9 rad(Si)/sec
    - Latchup 1.0E11 rad(Si)/sec
- ❑ Packaging options:
  - 68-lead ceramic quad flatpack (20.238 grams with lead frame)
- ❑ Standard Microcircuit Drawing 5962-04227
  - QML compliant part

INTRODUCTION

The UT8CR512K32 is a high-performance CMOS static RAM multi-chip module (MCM), organized as four individual 524,288 words by 8 bit SRAMs with common output enable. Easy memory expansion is provided by active LOW chip enables ($\overline{E}$), an active LOW output enable ($\overline{G}$), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected**.**

Writing to each memory is accomplished by taking the corresponding chip enable ($\overline{E}$) input LOW and write enable ($\overline{W}$) input LOW. Data on the I/O pins is then written into the location specified on the address pins (A_0 through A_{18}). Reading from the device is accomplished by taking the chip enable ($\overline{E}$) and output enable ($\overline{G}$) LOW while forcing write enable ($\overline{W}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The input/output pins are placed in a high impedance state when the device is deselected ($\overline{E}$ HIGH), the outputs are disabled ($\overline{G}$ HIGH), or during a write operation ($\overline{E}$ LOW and $\overline{W}$ LOW). Perform 8, 16, 24 or 32 bit accesses by making $\overline{W}$ along with $\overline{E}$ a common input to any combination of the discrete memory die.

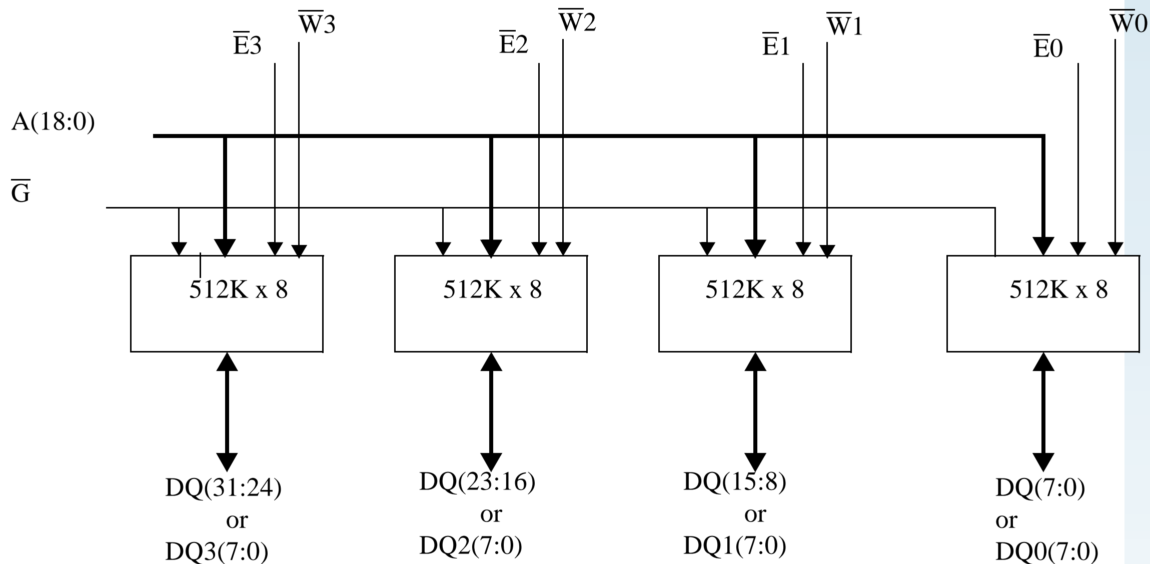


Figure 1. UT8CR512K32 SRAM Block Diagram

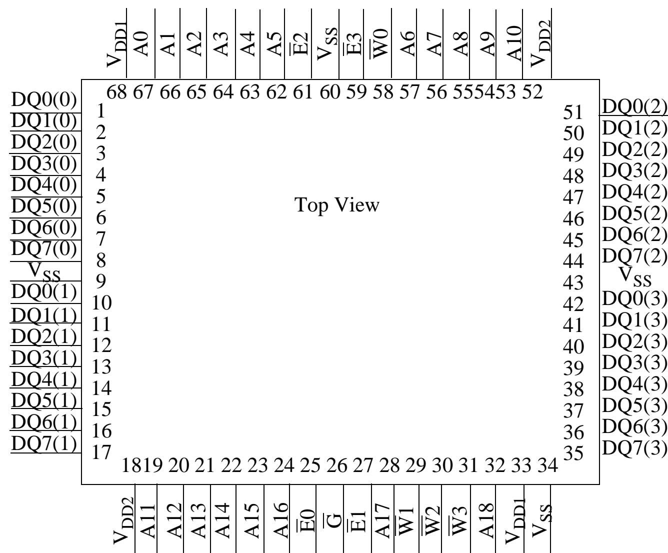


Figure 2. 17ns SRAM Pinout 68)

PIN NAMES

A(18:0)	Address
DQ(7:0)	Data Input/Output
$\overline{E}$	Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
V_{DD1}	Power (1.8V)
V_{DD2}	Power (3.3V)
V_{SS}	Ground

DEVICE OPERATION

Each die in the UT8CR512K32 has three control inputs called Enable ($\overline{E}$), Write Enable ($\overline{W}$), and Output Enable ($\overline{G}$); 19 address inputs, A(18:0); and eight bidirectional data lines, DQ(7:0). The device enable ($\overline{E}$) controls device selection, active, and standby modes. Asserting $\overline{E}$ enables the device, causes I_{DD} to rise to its active value, and decodes the 19 address inputs to each memory die by selecting the 2,048,000 byte of memory. $\overline{W}$ controls read and write operations. During a read cycle, $\overline{G}$ must be asserted to enable the outputs.

Table 1. Device Operation Truth Table

$\overline{G}$	$\overline{W}$	$\overline{E}$	I/O Mode	Mode
X	X	1	3-state	Standby
X	0	0	Data in	Write
1	1	0	3-state	Read[2]
0	1	0	Data out	Read

Notes:
1. “X” is defined as a “don’t care” condition.
2. Device active; outputs disabled.

READ CYCLE

A combination of $\overline{W}$ greater than V_{IH} (min) with $\overline{E}$ and $\overline{G}$ less than V_{IL} (max) defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output.

SRAM read Cycle 1, the Address Access is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}$ deasserted. Valid data appears on data outputs DQn(7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

SRAM read Cycle 2, the Chip Enable-controlled Access is initiated by $\overline{E}$ going active while $\overline{G}$ remains asserted, $\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the eight-bit word addressed by A(18:0) is accessed and appears at the data outputs DQn(7:0).

SRAM read Cycle 3, the Output Enable-controlled Access is initiated by $\overline{G}$ going active while $\overline{E}$ is asserted, $\overline{W}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

WRITE CYCLE

A combination of $\overline{W}$ less than V_{IL}(max) and $\overline{E}$ less than V_{IL}(max) defines a write cycle. The state of $\overline{G}$ is a “don’t care” for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH}(min), or when $\overline{W}$ is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access is defined by a write terminated by $\overline{W}$ going high, with $\overline{E}$ still active. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}$, and by t_{ETWH} when the write is initiated by $\overline{E}$. Unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQn(7:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access is defined by a write terminated by the former of $\overline{E}$ or $\overline{W}$ going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{W}$, and by t_{ETEF} when the write is initiated by the $\overline{E}$ going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQn (7:0) to avoid bus contention.

RADIATION HARDNESS

The UT8CR512K32 SRAM incorporates special design and layout features which allows operation in a limited radiation environment.

Table 2. Radiation Hardness Design Specifications[1]

Total Dose	300K	rad(Si)
Heavy Ion Error Rate[2]	$8.9x10^{-10}$	Errors/Bit-Day

Notes:
1. The SRAM is immune to latchup to particles >100MeV-cm^2/mg.
2. 10% worst case particle environment, Geosynchronous orbit, 100 mils of Aluminum.

Supply Sequencing

No supply voltage sequencing is required between V_{DD1} and V_{DD2}.

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD1}	DC supply voltage	-0.3 to 2.0V
V_{DD2}	DC supply voltage	-0.3 to 3.8V
$V_{I/O}$	Voltage on any pin	-0.3 to 3.8V
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	1.2W
T_J	Maximum junction temperature[2]	+150°C
Θ_{JC}	Thermal resistance, junction-to-case[3]	5°C/W
I_I	DC input current	±5 mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Maximum junction temperature may be increased to +175°C during burn-in and steady-static life.
3. Test per MIL-STD-883, Method 1012.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD1}	Positive supply voltage	1.7 to 1.9V
V_{DD2}	Positive supply voltage	3.0 to 3.6V
T_C	Case temperature range	(C) Screening: -55 to +125°C (W) Screening: -40 to +125°C
V_{IN}	DC input voltage	0V to V_{DD2}

DC ELECTRICAL CHARACTERISTICS (Pre and Post-Radiation)*
(-55°C to +125°C for (C) screening and -40°C to 125°C for (W) screening)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IH}	High-level input voltage		$.7*V_{DD2}$		V
V_{IL}	Low-level input voltage			$.3*V_{DD2}$	V
V_{OL1}	Low-level output voltage	I_{OL} = 8mA, $V_{DD2} = V_{DD2}$ (min)		$.2*V_{DD2}$	V
V_{OH1}	High-level output voltage	I_{OH} = -4mA, $V_{DD2} = V_{DD2}$ (min)	$.8*V_{DD2}$		V
C_{IN}[1]	Input capacitance	f = 1MHz @ 0V		44	pF
C_{IO}[1]	Bidirectional I/O capacitance	f = 1MHz @ 0V		21	pF
I_{IN}	Input leakage current	$V_{IN} = V_{DD2}$ and V_{SS}	-2	2	μA
I_{OZ}	Three-state output leakage current	$V_O = V_{DD2}$ and V_{SS}, $V_{DD2} = V_{DD2}$ (max) $\overline{G} = V_{DD2}$ (max)	-2	2	μA
I_{OS}[2, 3]	Short-circuit output current	$V_{DD2} = V_{DD2}$ (max), $V_O = V_{DD2}$ $V_{DD2} = V_{DD2}$ (max), $V_O = V_{SS}$	-100	+100	mA
$I_{DD1}(OP_1)$	Supply current operating @ 1MHz	Inputs : $V_{IL} = V_{SS}$ + 0.2V $V_{IH} = V_{DD2}$ - 0.2V, I_{OUT} = 0 $V_{DD1} = V_{DD1}$ (max), $V_{DD2} = V_{DD2}$ (max)		40	mA
$I_{DD1}(OP_2)$	Supply current operating @58.8MHz	Inputs : $V_{IL} = V_{SS}$ + 0.2V, $V_{IH} = V_{DD2}$ - 0.2V, I_{OUT} = 0 $V_{DD1} = V_{DD1}$ (max), $V_{DD2} = V_{DD2}$ (max)		100	mA
$I_{DD2}(OP_1)$	Supply current operating @ 1MHz	Inputs : $V_{IL} = V_{SS}$ + 0.2V $V_{IH} = V_{DD2}$ - 0.2V, I_{OUT} = 0 $V_{DD1} = V_{DD1}$ (max), $V_{DD2} = V_{DD2}$ (max)		.35	mA
$I_{DD2}(OP_2)$	Supply current operating @58.8MHz	Inputs : $V_{IL} = V_{SS}$ + 0.2V, $V_{IH} = V_{DD2}$ - 0.2V, I_{OUT} = 0 $V_{DD1} = V_{DD1}$ (max), $V_{DD2} = V_{DD2}$ (max)		11	mA
$I_{DD1}(SB)$[4]	Supply current standby @ 0Hz	CMOS inputs , I_{OUT} = 0 $\overline{E} = V_{DD2}$ -0.2 $V_{DD1} = V_{DD1}$ (max), $V_{DD2} = V_{DD2}$ (max)		35	mA
$I_{DD2}(SB)$[4]				5	μA
$I_{DD1}(SB)$[4]	Supply current standby A(18:0) @ 58.8MHz	CMOS inputs , I_{OUT} = 0 $\overline{E} = V_{DD2}$ - 0.2 $V_{DD1} = V_{DD1}$ (max), $V_{DD2} = V_{DD2}$ (max)		35	mA
$I_{DD2}(SB)$[4]				5	μA

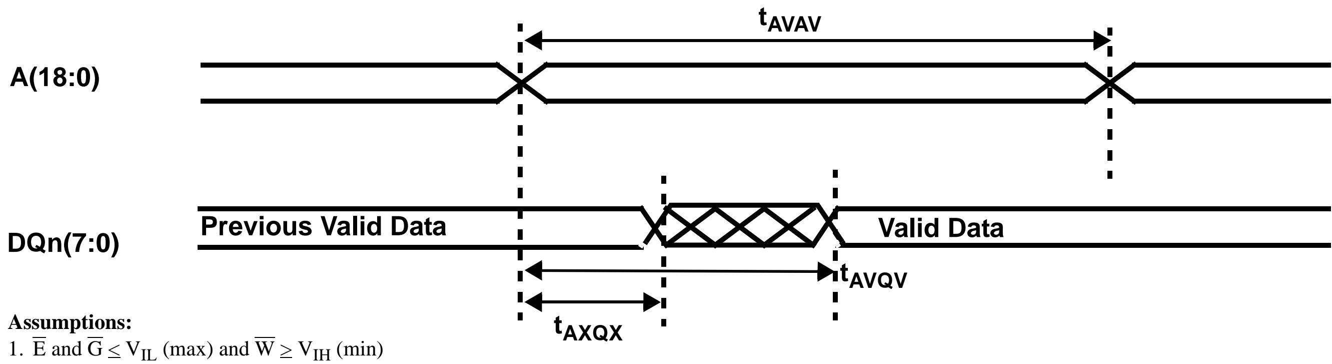
Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E5 rad(Si).
1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. $V_{IH} = V_{DD2}$ (max), V_{IL} = 0V.

AC CHARACTERISTICS READ CYCLE (Pre and Post-Radiation)*

(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening, $V_{DD1} = V_{DD1}$ (min), $V_{DD2} = V_{DD2}$ (min))

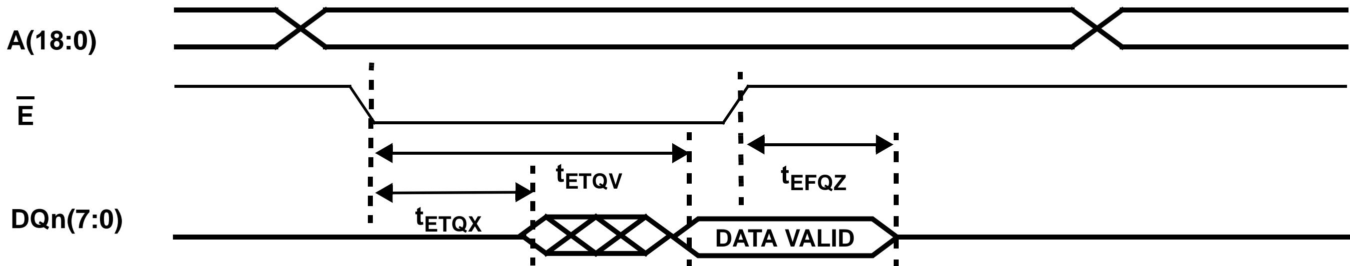
SYMBOL	PARAMETER	8CR512-155 MIN	MAX	UNIT
t_{AVAV}[1]	Read cycle time	17		ns
t_{AVQV}	Read access time		17	ns
t_{AXQX}[2]	Output hold time	3		ns
t_{GLQX}[1,2]	$\overline{G}$-controlled output enable time	0		ns
t_{GLQV}	$\overline{G}$-controlled read access time		7	ns
t_{GHQZ}[2]	$\overline{G}$-controlled output three-state time		7	ns
t_{ETQX}[2,3]	E-controlled output enable time	5		ns
t_{ETQV}[3]	E-controlled access time		17	ns
t_{EFQZ}[4]	E-controlled output three-state time[2]		10	ns

Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.
1. Guaranteed, but not tested.
2. Three-state is defined as a 200mV change from steady-state output voltage.
3. The ET (enable true) notation refers to the latter falling edge of $\overline{E}$. SEU immunity does not affect the read parameters.
4. The EF (enable false) notation refers to the latter rising edge of $\overline{E}$. SEU immunity does not affect the read parameters.



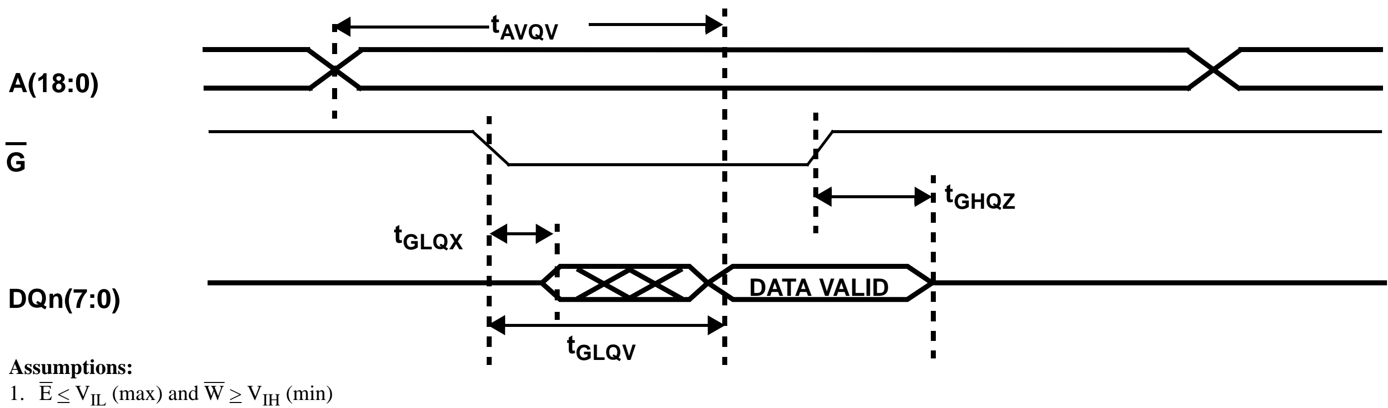
Assumptions:
1. $\overline{E}$ and $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

Figure 3a. SRAM Read Cycle 1: Address Access



Assumptions:
1. $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

Figure 3b. SRAM Read Cycle 2: Chip Enable-Controlled Access



Assumptions:
1. $\overline{E} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

Figure 3c. SRAM Read Cycle 3: Output Enable-Controlled Access

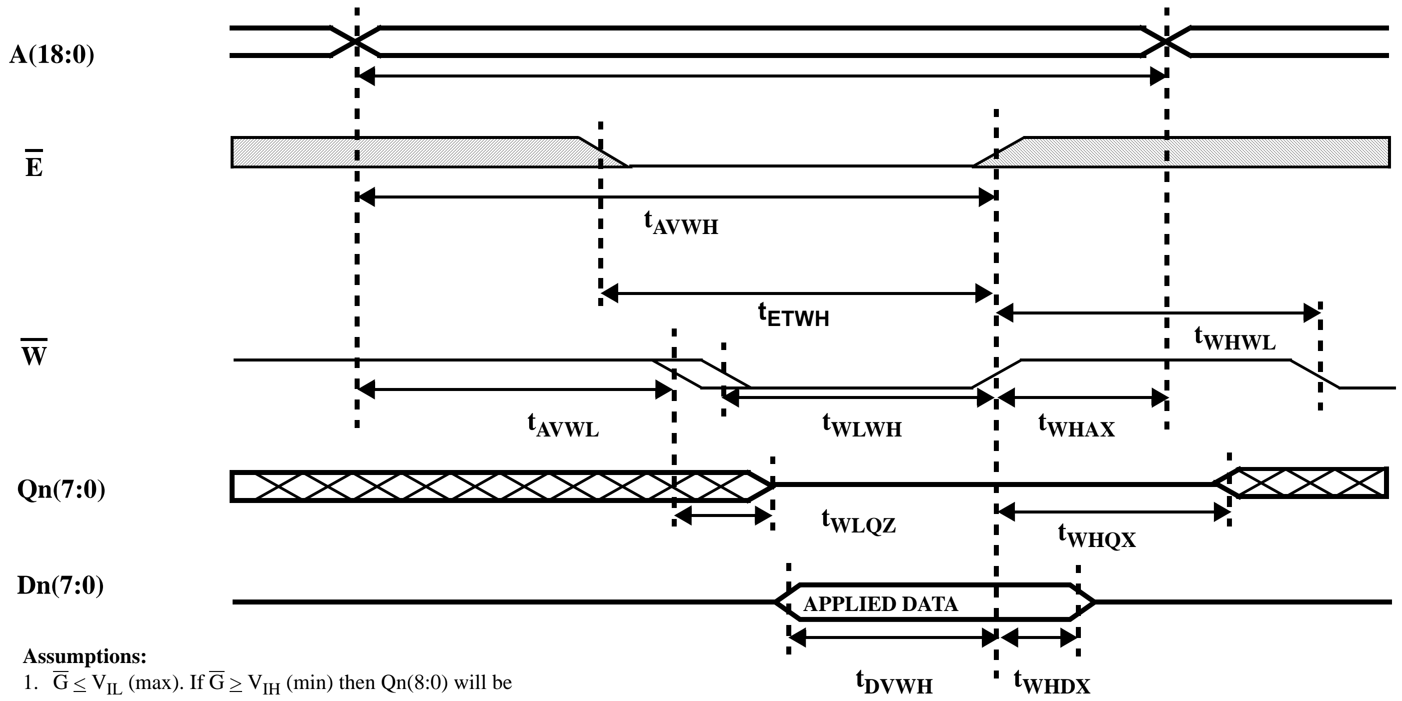
AC CHARACTERISTICS WRITE CYCLE (Pre and Post-Radiation)*

(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening, $V_{DD1} = V_{DD1}$ (min), $V_{DD2} = V_{DD2}$ (min))

SYMBOL	PARAMETER	8CR512-15 MIN	8CR512-15 MAX	UNIT
t_{AVAV}[1]	Write cycle time	17		ns
t_{ETWH}	Device enable to end of write	12		ns
t_{AVET}	Address setup time for write ($\overline{E}$- controlled)	0		ns
t_{AVWL}	Address setup time for write ($\overline{W}$ - controlled)	0		ns
t_{WLWH}	Write pulse width	12		ns
t_{WHAX}	Address hold time for write ($\overline{W}$ - controlled)	2		ns
t_{EFAX}	Address hold time for device enable ($\overline{E}$- controlled)	0		ns
t_{WLQZ}[2]	$\overline{W}$ - controlled three-state time		5	ns
t_{WHQX}[2]	$\overline{W}$ - controlled output enable time	4		ns
t_{ETEF}	Device enable pulse width ($\overline{E}$ - controlled)	12		ns
t_{DVWH}	Data setup time	7		ns
t_{WHDX}	Data hold time	2		ns
t_{WLEF}	Device enable controlled write pulse width	12		ns
t_{DVEF}	Data setup time	12		ns
t_{EFDX}	Data hold time	0		ns
t_{AVWH}	Address valid to end of write	12		ns
t_{WHWL}[1]	Write disable time	3		ns

Notes:

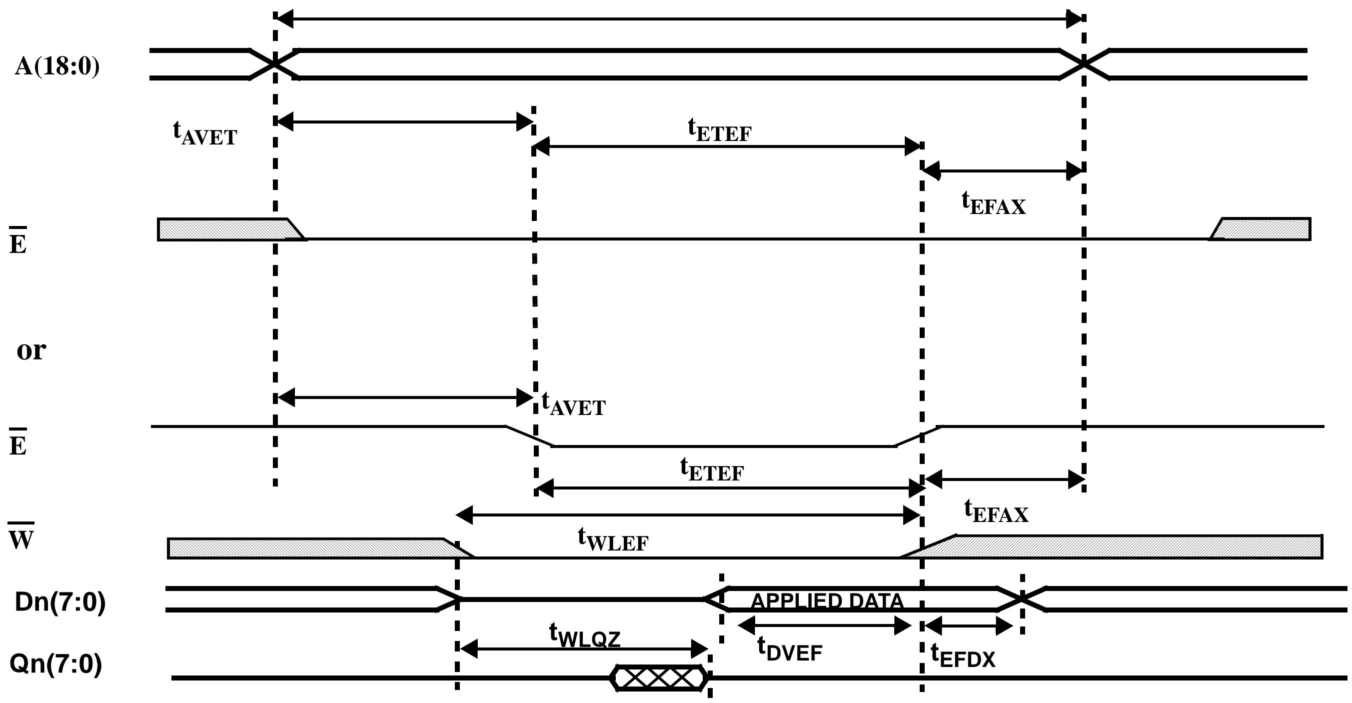
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.
1. Test with $\overline{G}$ high.
2. Three-state is defined as 200mV change from steady-state output voltage.



Assumptions:

1. $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq V_{IH}$ (min) then Qn(8:0) will be in three-state for the entire cycle.

Figure 4a. SRAM Write Cycle 1: Write Enable - Controlled Access



Assumptions & Notes:

1. $\overline{G} \le V_{IL}$ (max). If $\overline{G} \ge V_{IH}$ (min) then Qn(7:0) will be in three-state for the entire cycle.
2. Either $\overline{E}$ scenario above can occur.

Figure 4b. SRAM Write Cycle 2: Chip Enable - Controlled Access

DATA RETENTION CHARACTERISTICS (Pre-Radiation)* (V_{DD2} = V_{DD2} (min), 1 Sec DR Pulse)

SYMBOL	PARAMETER		MINIMUM	MAXIMUM	UNIT
V_{DR}	V_{DD1} for data retention	1.0	1.0	--	V
I_{DDR} [1] Device Type 1	Data retention current	-55°C	--	500	µA
		25°C		500	µA
		125°C		30	mA
I_{DDR} [1] Device Type 2	Data retention current	-40°C	--	500	µA
		25°		500	µA
		125°C		30	mA
t_{EFR} [1,2]	Chip deselect to data retention time	0	0		ns
t_R [1,2]	Operation recovery time	t_{AVAV}	t_{AVAV}		ns

Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.
1. $\overline{E}$ = V_{DD2} all other inputs = V_{DD2} or V_{SS}
2. V_{DD2} = 0 volts to V_{DD2} (max)

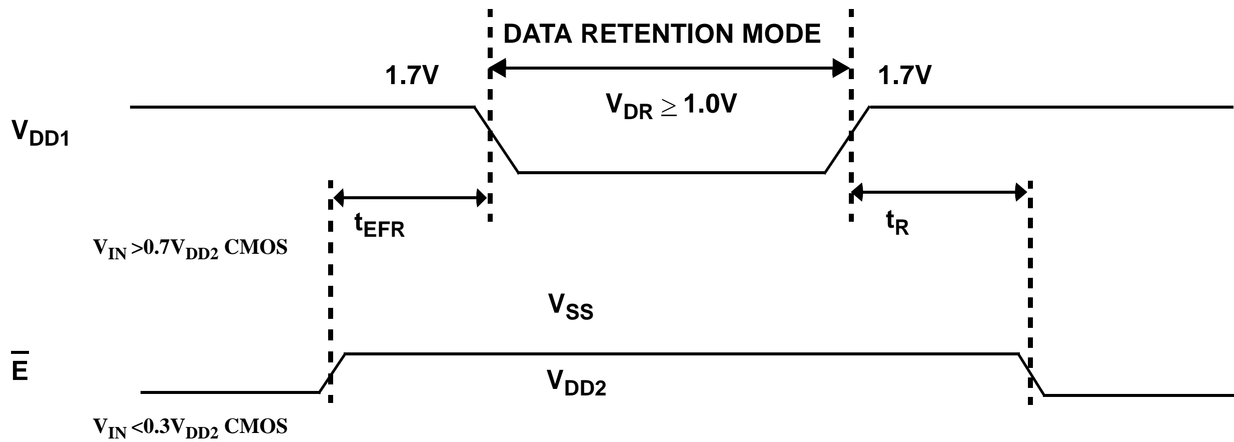
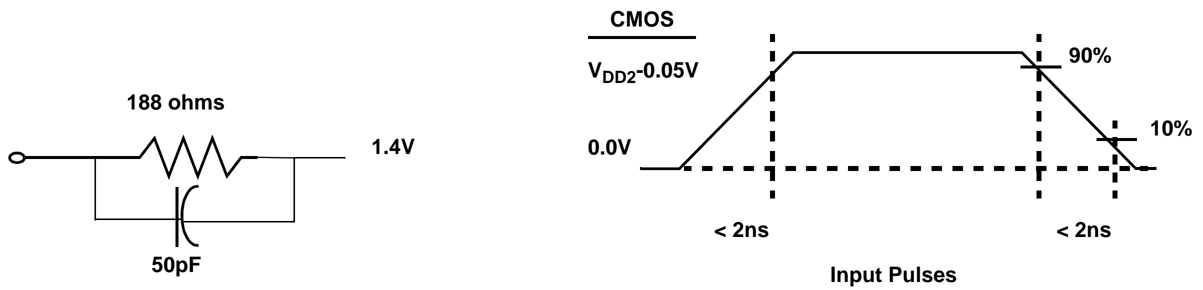


Figure 5. Low V_{DD} Data Retention Waveform



Notes:
1. 50pF including scope probe and test socket.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = $V_{DD2}/2$).

Figure 6. AC Test Loads and Input Waveforms

PACKAGING

DETAIL A
SCALE 3:1

REWORK DETAIL
NO SCALE

POWER AND GROUND EXTERNAL PIN TABLE

VSS	9, 34, 43, 60
VDD1	33, 68
VDD2	18, 52

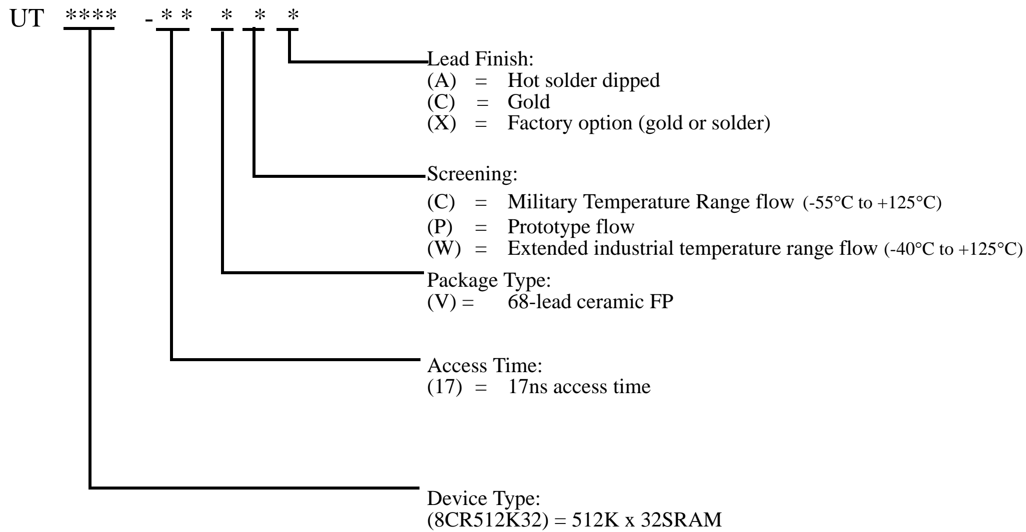
Notes:

1. All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance to MIL-PRF-38535.
4. Ceramic shall be dark alumina.
5. Letter designations are to cross reference to MIL-STD-1835.
6. Dogleg geometries are optional within dimensions shown.
7. These areas may have notches and tabs different than shown.
8. Lead true position tolerances and coplanarity are not measured.
9. Packages may be shipped with repaired leads as shown. Coplanarity requirements do not apply in the repaired area.
10. Numbering and lettering on the ceramic are not subject to visual or marking criteria.

Figure 7. 68-pin Ceramic FLATPACK

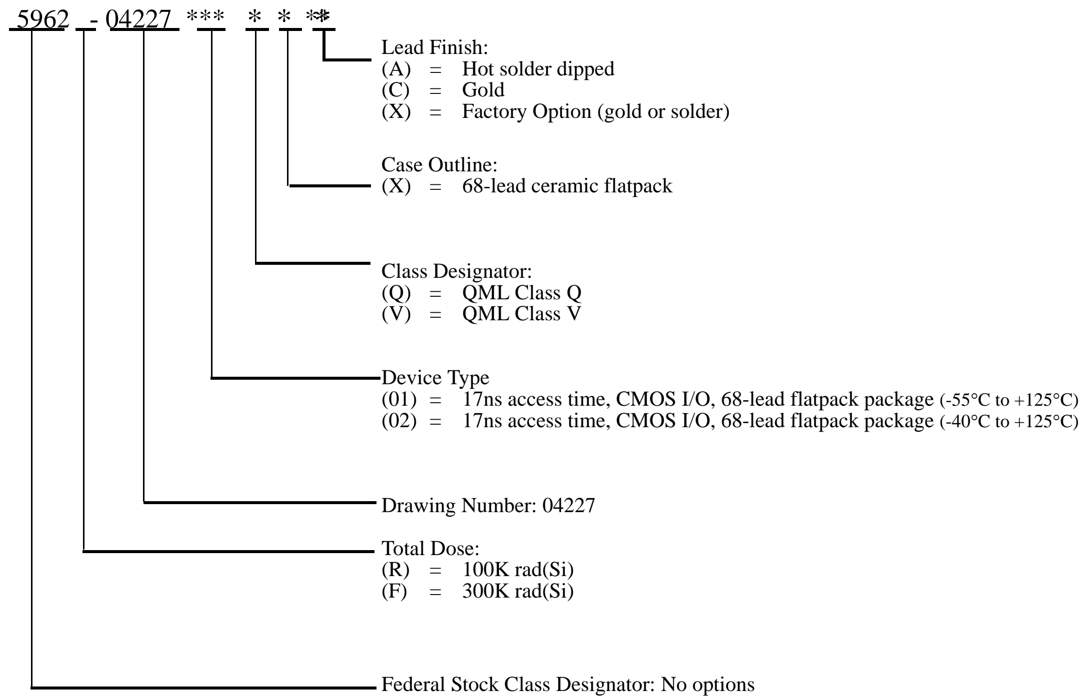
ORDERING INFORMATION

512K32 SRAM:



Notes:
1. Lead finish (A,C, or X) must be specified.
2. If an “X” is specified when ordering, then the part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
3. Prototype flow per UTMC Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per UTMC Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

512K x 32 SRAM: SMD



Notes:

1.Lead finish (A,C, or X) must be specified.

2.If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).

3.Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

NOTES

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