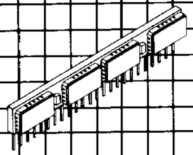
MB85204-10, MB85204-12, MB85204-15

262,144 x 4-Bit Dynamic Random Access Memory SIP Module

Description

The Fujitsu MB85204 is a fully decoded, 262,144 word x 4-bit NMOS dynamic random access memory module consisting of four MB81256 DRAMs in 18-pad LCC packages mounted on a 24-pin multilayer ceramic substrate.

The MB85204 is intended for use in memory applications where large memory capacity is required within limited physical volume. Significant size reduction can be realized in applications such as mainframe memory, buffer memory, desk top computers and peripheral storage.



MSP-24S-CC04

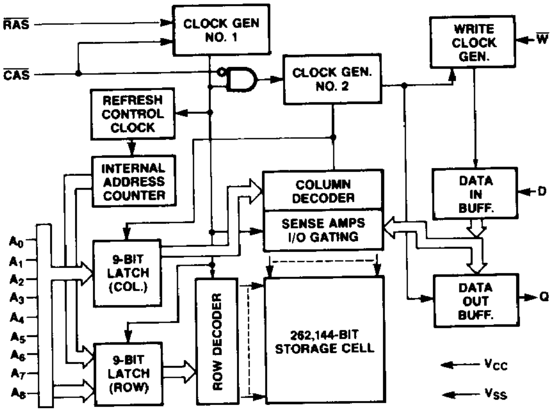
Features

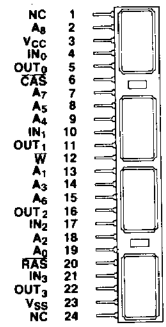
- **262,144 x 4 DRAM**
  24-pin SIP (MB81256x4)
- **Row access time**
  100 ns max. (MB85204-10)
  120 ns max. (MB85204-12)
  150 ns max. (MB85204-15)
- **Cycle time**
  210 ns min. (MB85204-10)
  230 ns min. (MB85204-12)
  260 ns min. (MB85204-15)
- **Page cycle time**
  100 ns min. (MB85204-10)
  120 ns min. (MB85204-12)
  150 ns min. (MB85204-15)
- **Single + 5V supply, ±10% tolerance**
- **Low power (active)**
  1540 mW max. (MB85204-10)
  1430 mW max. (MB85204-12)
  1254 mW max. (MB85204-15)
  100 mW max. (standby)
- **4 ms/256 refresh cycles capability**
- **$\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden refresh capability**
- **Read-Modify-Write and Page Mode Capability**
- **Common I/O capability using Early Write operation**
- **On-chip latches for Addresses and Data-in**
- **All inputs and outputs are TTL compatible.**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

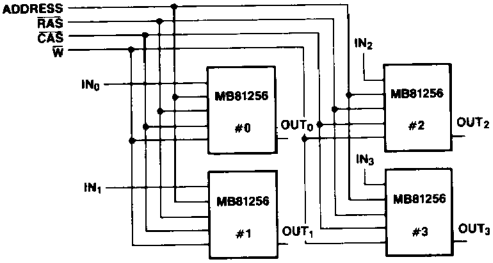
MB85204 Block Diagrams and Pin Assignment

Block Diagram for Each Chip





Functional Block Diagram



Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative toV_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	2.4	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Description

Simple Timing Requirements

The MB85204 has improved circuitry that eases timing requirements for high speed access operations. The MB85204 can operate under the condition of t_{RCD}(max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB85204 has minimal hold times of address (t_{CAH}), $\overline{W}$ (t_{WCH}) and IN (t_{DH}). Fujitsu has made timing requirements that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the column address, IN and $\overline{W}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{W}$ Delay) are not restricted by t_{RCD}.

Address Inputs

A total of eighteen binary input address bits are required to decode any 4 bits of data in 1,048,576 storage cells within the MB85204. Nine row address bits are established on the input pins (A_0 through A_8) and latched with $\overline{RAS}$. Nine column address bits are established on the input pins and latched with $\overline{CAS}$. All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable

The read mode or write mode is selected with the $\overline{W}$ input. A logic high on the $\overline{W}$ dictates read mode, logic low dictates write mode. Data inputs are disabled when read mode is selected.

Data Inputs

The 4-bit data is written into the MB85204 during a write or read-write cycle. The latter falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the IN register. In a write cycle, if $\overline{W}$ is brought low before the negative transition of $\overline{CAS}$, the set-up and hold times are referenced to $\overline{CAS}$. In a delayed write or read-write cycle, $\overline{W}$ will be low after $\overline{CAS}$ has already been low. Thus IN_0 to IN_3 are strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Outputs

The output buffers of each chip are three-state TTL compatible with a fan-out of two standard TTL loads. OUT is the same polarity as IN. The output is in high impedance state until $\overline{CAS}$ is brought low. In a read or read-write cycle, the output is valid after t_{RAC} from negative transition of the $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from negative transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle, the identical sequence occurs but data is not valid.

Fast Read-While-Write Cycle

The MB85204 has a fast read-while-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{W}$ when $\overline{CAS}$ goes low. When $\overline{W}$ is low during $\overline{CAS}$ transition to low, the MB85204 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when $\overline{W}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MB85204 goes into the delayed write mode. The output then contains the data from the cell selected and the data from IN are written into the cell selected. Therefore, a very fast read-write cycle ($t_{RC} = t_{RWC}$) is possible with the MB85204.

Page-Mode

Page-mode operation permits strobing the row-address into the MB85204 while maintaining $\overline{RAS}$ at low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row addresses (A_0 through A_7) at least every 4 ms. During refresh, either V_{IL} or V_{IH} is permitted for A_8. Then MB85204 offers the following three types of refresh.

1) $\overline{RAS}$-Only Refresh;
   $\overline{RAS}$ Only refresh avoids any output during refresh because the output buffer is in high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed.
2) $\overline{CAS}$-before-$\overline{RAS}$ Refresh;
   $\overline{CAS}$-before-$\overline{RAS}$ refresh available on the MB85204 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter for each chip are enabled, and an internal refresh operation takes place. After the refresh operation has been executed the refresh address counter is automatically incremented for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.
3) Hidden Refresh;
   Hidden refresh may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. In the MB85204, hidden refresh means $\overline{CAS}$-before-$\overline{RAS}$ refresh and the internal refresh address is used; that is, no external refresh address is needed.

Description
(Continued)

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Counter Test Cycle

A special timing sequence using $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh activated circuitry. After the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh operation, if $\overline{\text{CAS}}$ goes into high and goes into low again while $\overline{\text{RAS}}$ is held low, the read and write operations are enabled. This is shown in the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ counter test cycle timing diagram. A memory cell address (consisting of a row address (9 bits) and a column address (9 bits)) to be accessed, can be defined as follows:

1) A ROW ADDRESS—Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set high internally.
2) A COLUMN ADDRESS—All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{\text{CAS}}$.

Suggested $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Counter Test Procedure

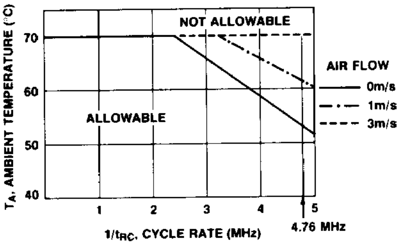
1) Initialize the internal refresh address counter by using eight $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles.
2) Throughout the test, use the same column address, and keep RA8 high.
3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
4) Read "low" written in step (3) and check, and simultaneously write "high" to the same address by using internal refresh counter test read-write cycles. This spec is repeated 256 times, with the addresses being generated by internal refresh address counter.
5) Read "high" written in step (4) and check by using normal read cycle for all 256 locations.
6) Complement the test pattern and repeat step (3), (4) and (5).

Decoupling and Noise Reduction Recommendations for MB85204

To minimize noise induction between signal lines as well as between signal and power supply lines, good board design practice requires consideration of the following:

1) Provide a capacitor of approx. a few μF for each module—even though the MB85204 has two or four decoupling capacitors of 0.1 μF on each module.
2) Remove noise, overshoot and undershoot from the address, control and data-input lines, so that the MB85204 won't latch wrong signals due to the noise induction between signal lines, and between signal and power supply lines.
3) Keep enough timing margin and remove critical timing in the board design to avoid the problem mentioned in Item 2 above.
4) In order to avoid noise induction on the IN line at the falling edge of $\overline{\text{W}}$ when the delayed write or read-modify-write cycle is used, the falling edge of $\overline{\text{W}}$ signal should not coincide with the transition point of address and OUT signals. (Since decoupling capacitors on the module board can't smooth the output current at the OUT pin, noise is inducted on the power supply line (V_{CC} or V_{SS}) and also on the IN line at t_{RAC} or t_{CAC} in the read cycle.)
5) Provide an appropriate damping if necessary, to avoid excessive overshoot or undershoot on the TTL input waveform.

MB85204 Derating Curve



Recommended Operating Conditions

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V	0°C to +70°C[*1]
Input high voltage	V_{IH}	2.4		6.5	V	
Input low voltage	V_{IL}	−2.0		0.8	V	

Note: 1* Maximum ambient temperature is permissible under certain conditions. See derating curve.

Capacitance

(T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input capcitance A_0 to A_8	C_{IN1}		40	pF
Input capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$	C_{IN2}		50	pF
Input capacitance IN	C_{IN3}		15	pF
Output capacitance OUT	C_{OUT}		15	pF

DC Characteristics

(Recommended operating conditions unless otherwise noted.)

		MB85204-10		MB85204-12		MB85204-15		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Operating current Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	I_{CC1}	280		260		228		mA
Standby current Standby power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		18		18		18	mA
Refresh current 1[*1] Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min.)	I_{CC3}		240		220		200	mA
Page mode current Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = Min.)	I_{CC4}		140		120		100	mA
Refresh current 2[*1] Average power supply current ($\overline{CAS}$-before-RAS; t_{RC} = Min.)	I_{CC5}		260		240		220	mA
Input leakage current, any input ($0 \leq V_{IN} \leq 5.5V$, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	$I_{I(L)}$	−40	40	−40	40	−40	40	µA
Output leakage current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	$I_{O(L)}$	−10	10	−10	10	−10	10	µA
Output levels Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)	 V_{OH} V_{OL}	 2.4 	 0.4	 2.4 	 0.4	 2.4 	 0.4	V

Notes: *1 I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC Characteristics[*1,2,3]

(Recommended operating conditions unless otherwise noted.)

Parameter	**Symbol**	**MB85204-10**		**MB85204-12**		**MB85204-15**		**Unit**
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	
Time between refresh	t_{REF}		4		4		4	ms
Random read/write cycle time[*12]	t_{RC}	210		230		260		ns
Read-write-cycle time[*12]	t_{RWC}	210		230		260		ns
Access time from $\overline{\text{RAS}}$[*4,5]	t_{RAC}		100		120		150	ns
Access time from $\overline{\text{CAS}}$[*5,6]	t_{CAC}		50		60		75	ns
Output buffer turn off delay	t_{OFF}	0	25	0	25	0	30	ns
Transition time	t_T	3	50	3	50	3	50	ns
$\overline{\text{RAS}}$ precharge time	t_{RP}	90		100		100		ns
$\overline{\text{RAS}}$ pulse width	t_{RAS}	110	100000	120	100000	150	100000	ns
$\overline{\text{RAS}}$ hold time	t_{RSH}	60		60		75		ns
$\overline{\text{CAS}}$ pulse width	t_{CAS}	60	100000	60	100000	75	100000	ns
$\overline{\text{CAS}}$ hold time	t_{CSH}	110		120		150		ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time[*7,8]	t_{RCD}	20	50	22	60	25	75	ns
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ set up time	t_{CRS}	15		20		20		ns
Row address set up time	t_{ASR}	0		0		0		ns
Row address hold time	t_{RAH}	10		12		15		ns
Column address set up time	t_{ASC}	0		0		0		ns
Column address hold time	t_{CAH}	15		20		25		ns
Read command set up time	t_{RCS}	0		0		0		ns
Read command hold time referenced to $\overline{\text{CAS}}$[*11]	t_{RCH}	0		0		0		ns
Read command hold time referenced to $\overline{\text{RAS}}$[*11]	t_{RRH}	20		20		20		ns
Write command set up time[*9]	t_{WCS}	0		0		0		ns
Write command pulse width	t_{WP}	15		20		25		ns
Write command hold time	t_{WCH}	15		20		25		ns
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	40		50		60		ns

Notes:

*1 An initial pause of 200 μs is required after power-up. And then several cycle (to which any 8 cycle to perform refresh are adequate) are required before proper device operation is achieved.
If internal refresh counter is to be effective, a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles are required.

*2 AC characteristics assume $t_T = 5$ ns.

*3 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).

*4 Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

*5 Assumes that $t_{RCD} \geqslant t_{RCD}$ (max).

*6 Measured with a load equivalent to 2 TTL loads and 100 pF.

*7 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

*8 t_{RCD} (min) = t_{RAH} (min) + $2t_T$ ($t_T = 5$ ns) + t_{ASC} (min).

*9 t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqslant t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} \geqslant t_{CWD}$ (min) the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

*11 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

*12 The minimum cycle time is dependent on the ambient temperature and cooling conditions.
See derating curve.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

		MB85204-10		MB85204-12		MB85204-15		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	40		50		60		ns
Data in set up time	t_{DS}	0		0		0		ns
Data in hold time	t_{DH}	15		20		25		ns
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay[9]	t_{CWD}	15		20		25		ns
Refresh set up time for $\overline{\text{CAS}}$ referenced to $\overline{\text{RAS}}$	t_{FCS}	20		25		30		ns
Refresh hold time for $\overline{\text{CAS}}$ Referenced to $\overline{\text{RAS}}$	t_{FCH}	20		25		30		ns
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ active time	t_{RPC}	20		20		20		ns
Page mode read/write cycle time	t_{PC}	100		120		150		ns
Page mode read/write cycle time	t_{PRWC}	100		120		150		ns
Page mode $\overline{\text{CAS}}$ precharge time	t_{CP}	40		50		65		ns
Refresh counter test cycle time[10]	t_{RTC}	330		375		430		ns
Refresh counter test $\overline{\text{RAS}}$ pulse width[10]	t_{TRAS}	230	10000	265	10000	320	10000	ns
Refresh counter test $\overline{\text{CAS}}$ precharge time[10]	t_{CPT}	50		60		70		ns
$\overline{\text{CAS}}$ precharge time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycle)	t_{CPR}	20		25		30		ns

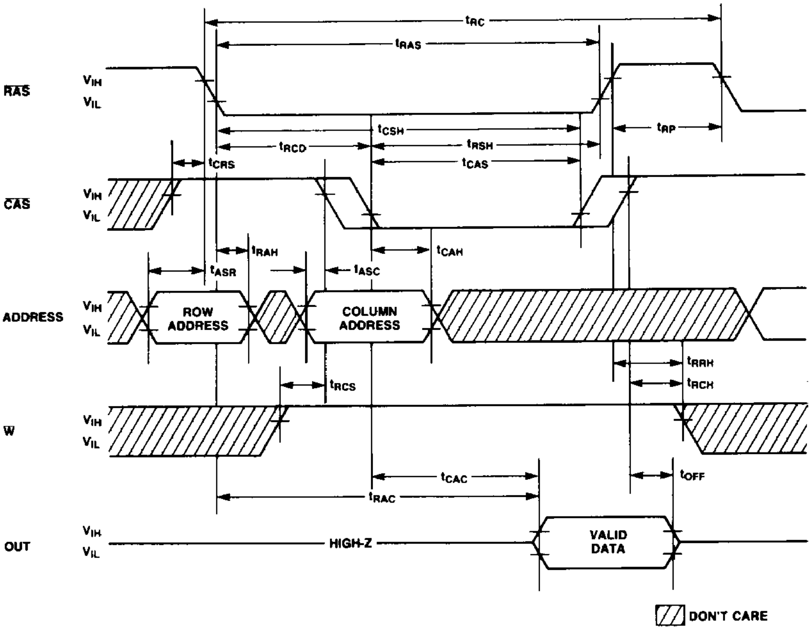
Notes:

[9] t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

[10] Test mode write cycle only.

Timing Diagrams

Read Cycle



Timing Diagrams
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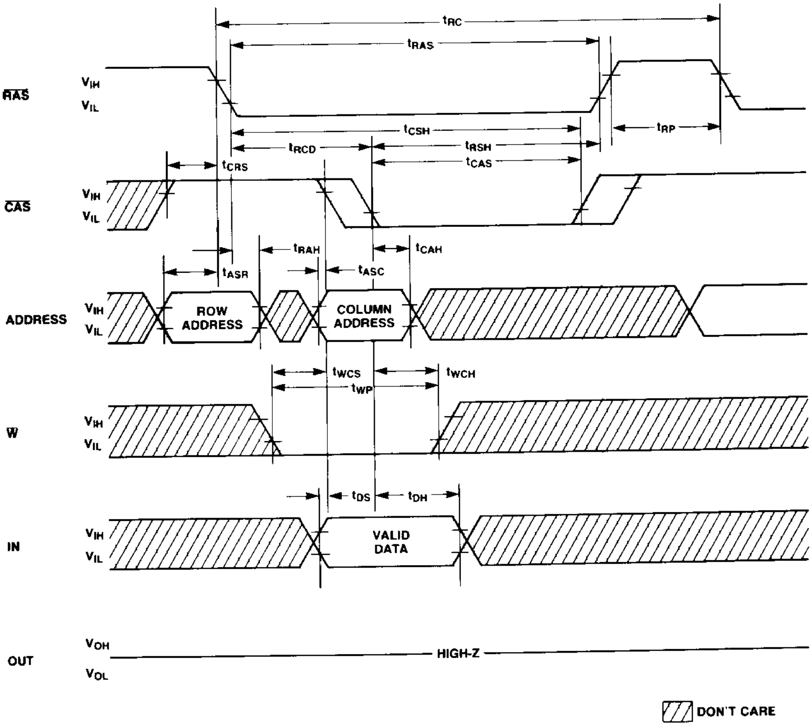
Write Cycle (Early Write)



Timing Diagrams
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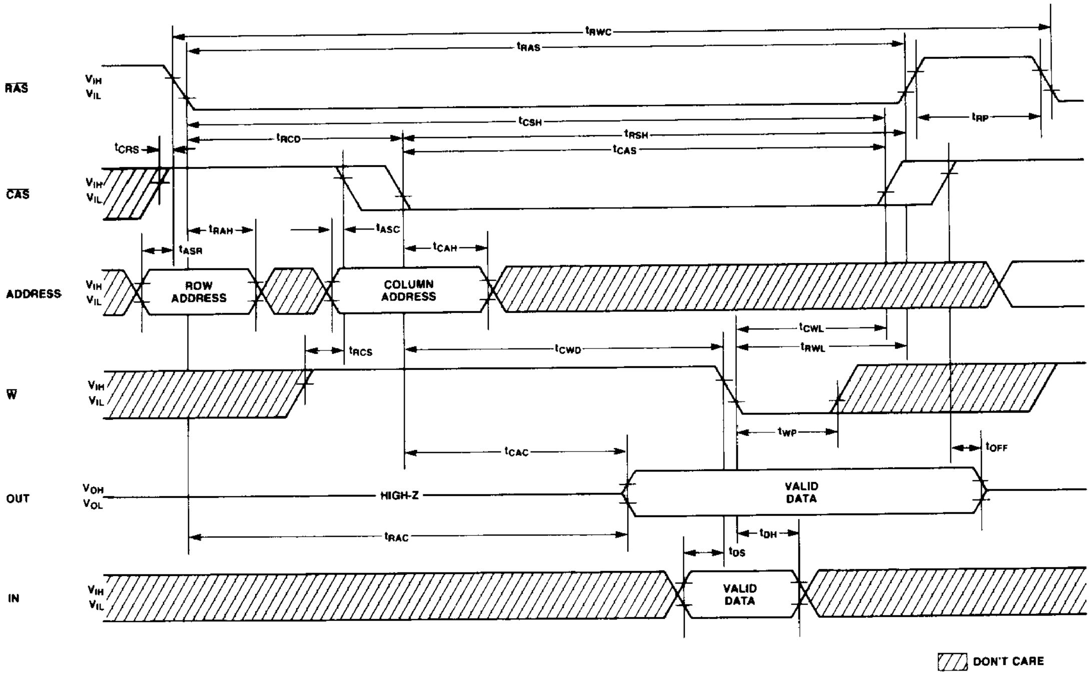
Read-Write/Read-Modify-Write Cycle



Timing Diagrams
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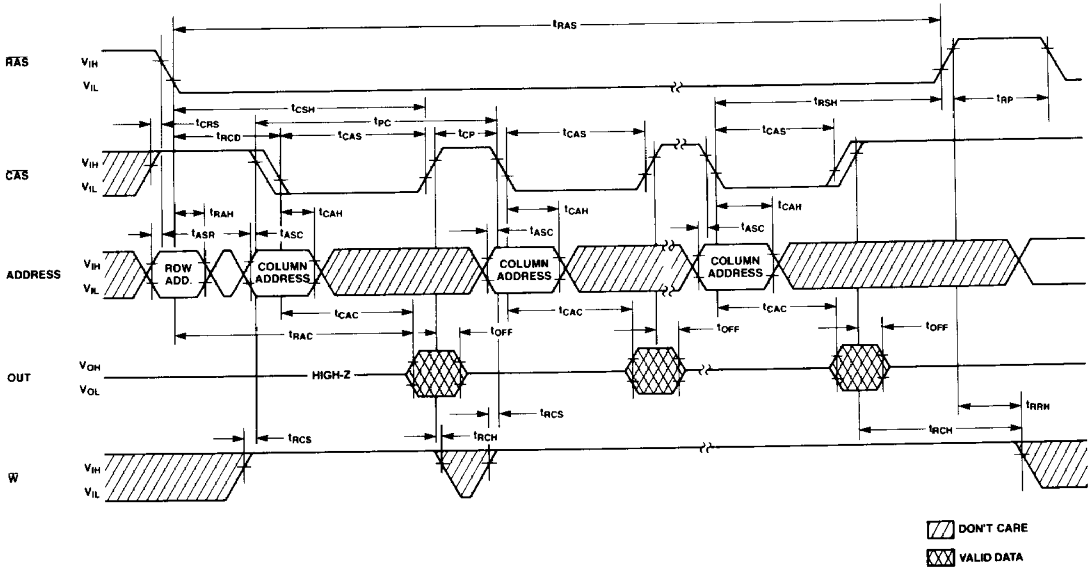
Page Mode Read Cycle



Timing Diagrams
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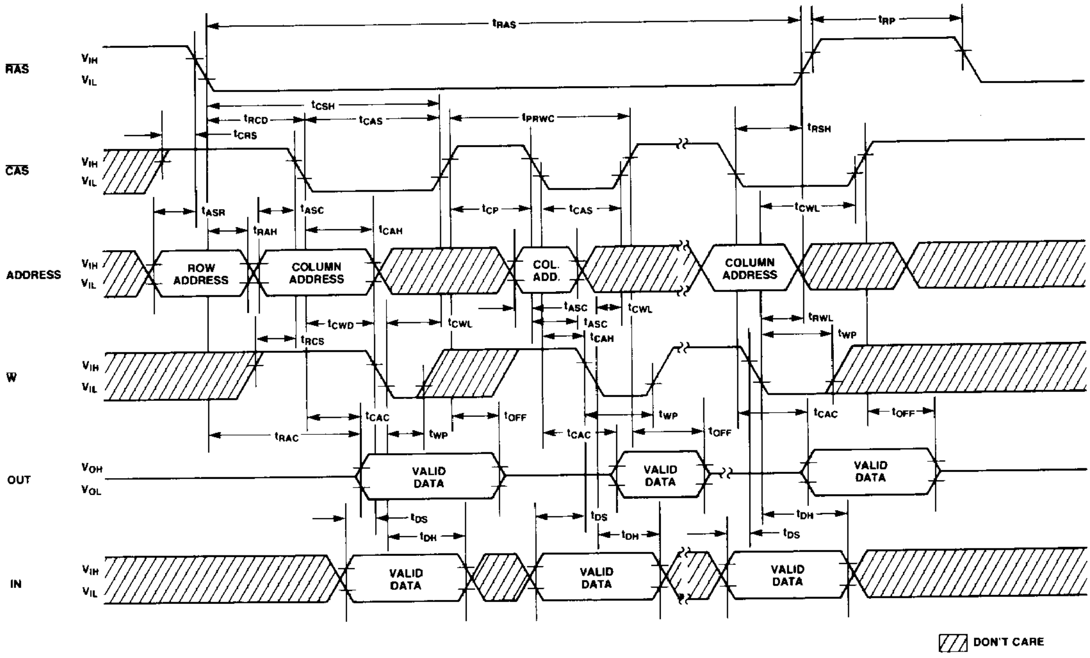
Page Mode Read-Write Cycle



Timing Diagrams
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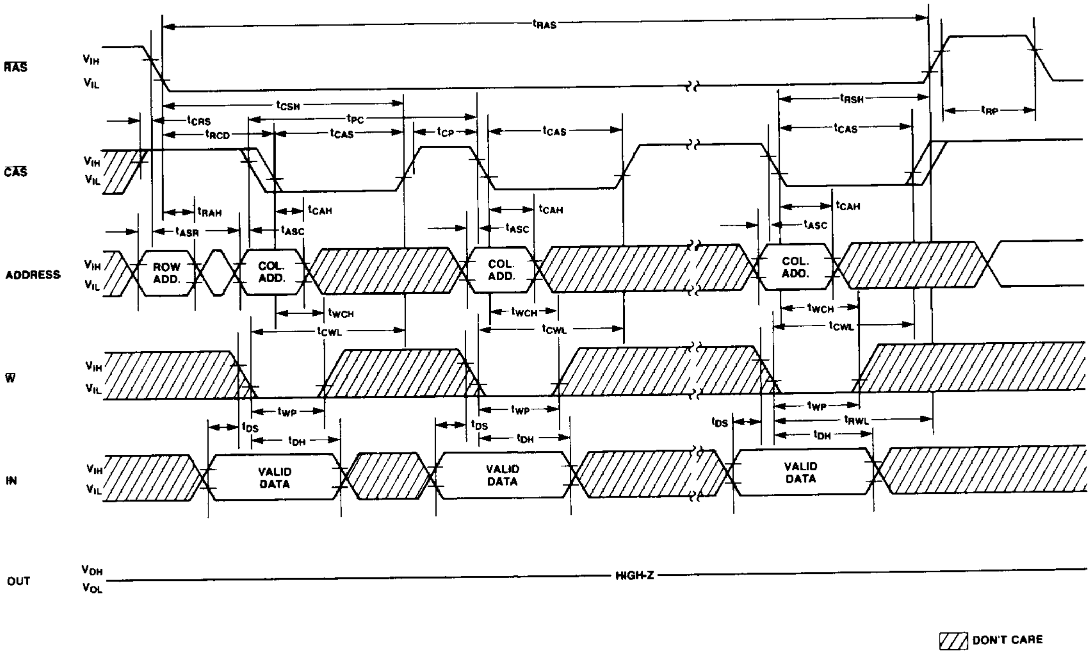
Page Mode Write Cycle



Timing Diagrams
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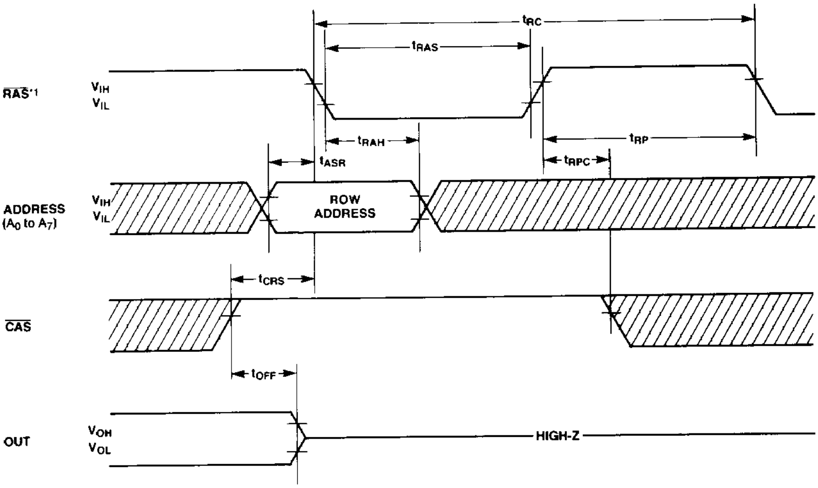
$\overline{\text{RAS}}$-only Refresh Cycle

Note: $\overline{\text{CAS}}$ = V_{IH}, W, IN = Don't Care, A_8 = V_{IH} or V_{IL}

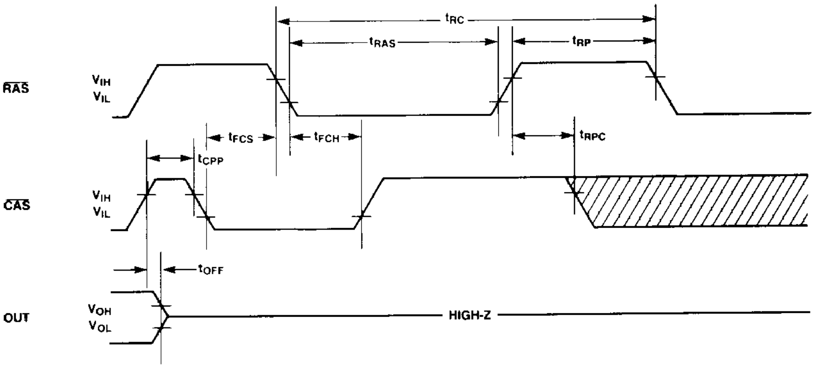


NOTE: *1 ANY COMBINATIONS OF $\overline{\text{RAS}}$0 TO $\overline{\text{RAS}}$3 ARE ALLOWED AND $\overline{\text{RAS}}$'s TO BE NOT REFRESHED ARE IN V_{IH}.

▨ DON'T CARE

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Cycle

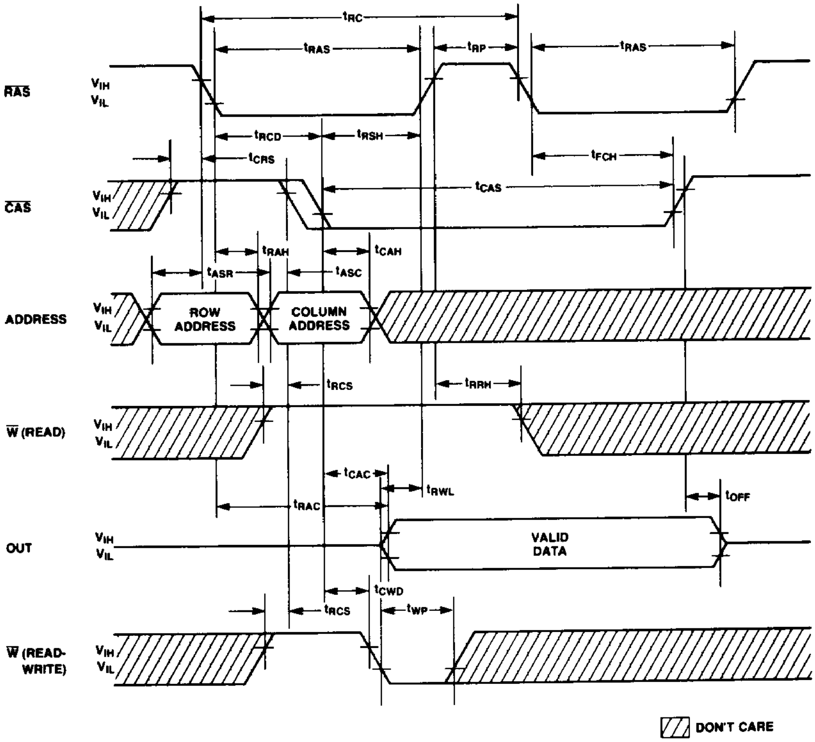
Note: Address, W, IN = Don't care



▨ DON'T CARE

Timing Diagrams
(Continued)

Hidden Refresh Cycle



Timing Diagrams
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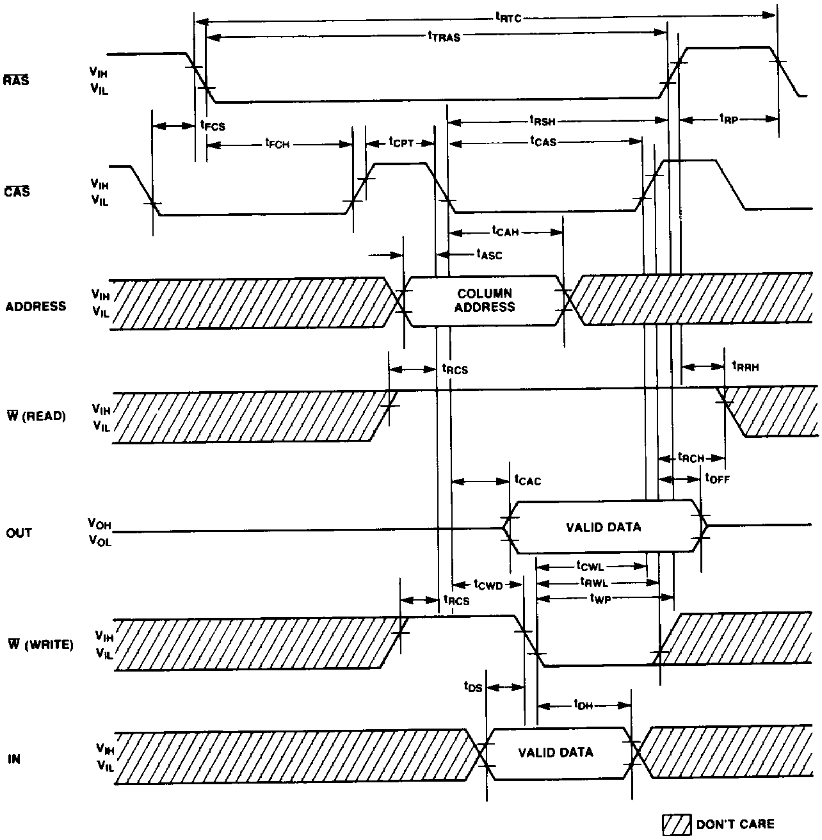
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



Package Dimensions

Dimensions in inches
(millimeters)

24-Lead Single In-Line Package Module
(Module No.: MSP-24S-CC04)