FAIRCHILD
SEMICONDUCTOR™

NM95MS15
Plug and Play Front-End Device for ISA-Bus Systems

General Description

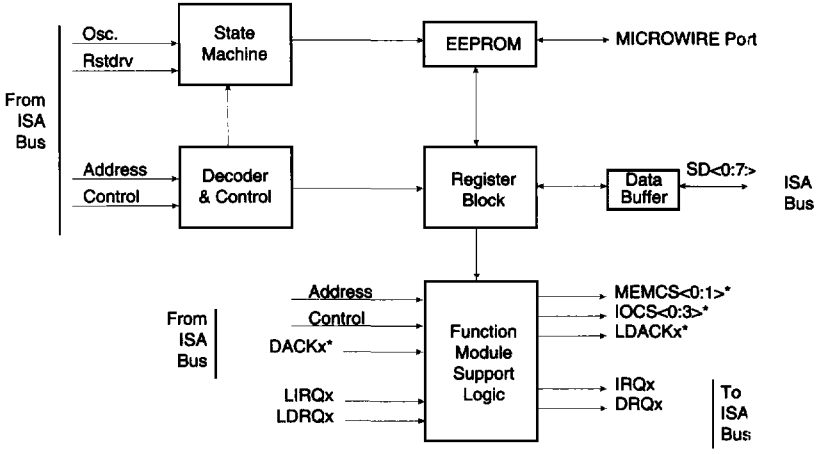
The NM95MS15 is one of the family of single chip solutions designed to provide complete Plug and Play capability for ISA bus systems. The NM95MS15 includes the necessary state machine logic to manage the Plug and Play protocol in addition to switches for steering Interrupt and DMA requests. It also features a built-in 4k bits of serial EEPROM for storing the resource data specified in the Plug and Play Standard. In addition, 4k bits of the EEPROM is available for use by other on-board logic. This device provides a truly complete single-chip solution for implementing Plug and Play on ISA-Bus adapter cards. The NM95MS15 supports two logical devices with a flexible choice of DMA/IRQ selection, I/O, and MEMORY Chip Select generation.

NM95MS15 is implemented using Fairchild's advanced CMOS process and operates from a single power supply. The NM95MS15 is available in a 64-pin TQFP package.

Features

- Single chip implementation of complete Plug and Play Standard
  - —Direct interface to ISA-bus
- Three modes of operation
  - —Normal DMA mode
  - —Extended Interrupt mode
  - —Extended DMA mode
- 6, 8, or 11 ISA-bus interrupt lines and 3 DRQ/DACK lines supported (IRQ's and DRQ's are mode dependent)
- On-chip EEPROM for resource request table
- Additional 4k bits of on-chip EEPROM available for external access
- 24 mA drivers for data outputs
- 64-pin TQFP package

Functional Diagram



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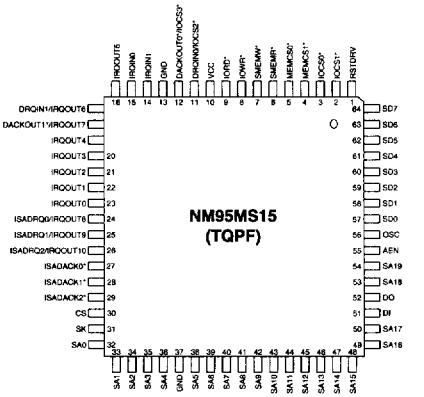
Connection Diagram



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Commercial Temperature Range (0°C to +70°C)

Order Number NM95MS15VEH

Signals	Type	Description
SA<19:0>	I	Address inputs from the ISA bus.
IORD* (Note 1) , SMEMR* (Note 1)	I	I/O and memory read strobes from the ISA bus.
IOWR* (Note 1) , SMEMW* (Note 1)	I	I/O write and memory write strobes from the ISA bus.
AEN	I	Address Enable from ISA bus—used in conjunction with DMA.
SD<7:0>	I/O	Data bus—lower byte—from/to the ISA bus.
OSC (Note 2)	I	"OSC" Clock from ISA bus—used for internal state machine.
RSTDRV	I	Reset input from the ISA bus.
SK,DI	I	Clock and Data input lines for microwire bus connection to access a portion (4k) on chip EEPROM.
CS	I	Chip select for microwire bus connection to access 4k on chip EEPROM. This pin should be pulled down to GND, if the 4k user portion is not used.
DO	O	Data output line for the Microwire interface detailed above.
IRQOUT<5:0>	O	Connection to ISA bus interrupt request pins. On-chip interrupt requests may be connected to any of the 6 lines.
IRQOUT6/DRQIN1	I/O	Interrupt request line to the ISA bus or DMA request line from on-board logic.
IRQOUT7/DACKOUT1* (Note 1)	O	Interrupt request line to the ISA bus or DMA ackowledge for on-board logic.
IRQIN<1:0>	I	Interrupt request from on-board logic.
DRQIN0/IOCS2* (Note 1)	I/O	DMA request from on-board logic or IOCS2 depending on mode selected.
DACKOUT0*/IOCS3*	O	DMA Acknowledge for on-board logic or IOCS3 depending on mode selected.
ISADRQ<2:0>/IRQOUT<10:8>	O	Connection for three ISA bus DMA Request lines, or additional interrupt request lines depending on the mode selected.
ISADACK<2:0>* (Note 1)	I	DMA acknowledge from the ISA bus.
IOCS<1:0>* (Note 1)	O	Programmable chip selects to address on-board peripherals
MEMCS<1:0>* (Note 1)	O	Programmable chip selects to address on-board ROM/Memory.

Note 1: * Means active low signal

Connection Diagram (Continued)

Note 2: "OSC" clock from ISA Bus is fixed at a standard frequency of 14.318 MHz. NM95MS15 is designed and tested for this frequency. However NM95MS15 can handle frequencies up to 24 MHz though it is not 100% tested.

Pinout Details for the NM95MS15

Mode 00 = DMA Mode; Mode 01 = Extended Interrupt Mode; Mode 10 = Extended DMA Mode

Pin #		Pin Name	
TQFP	Mode "00"	Mode "01"	Mode "10"
1	RSTDRV	RSTDRV	RSTDRV
2	IOCS1*	IOCS1*	IOCS1*
3	IOCS0*	IOCS0*	IOCS0*
4	MEMCS1*	MEMCS1*	MEMCS1*
5	MEMCS0*	MEMCS0*	MEMCS0*
6	SMEMR*	SMEMR*	SMEMR*
7	SMEMW*	SMEMW*	SMEMW*
8	IOWR*	IOWR*	IOWR*
9	IORD*	IORD*	IORD*
10	V_{CC}	V_{CC}	V_{CC}
11	DRQIN0	IOCS2*	DRQIN0
12	DACKOUT0*	IOCS3*	DACKOUT0*
13	GND	GND	GND
14	IRQIN1	IRQIN1	IRQIN1
15	IRQIN0	IRQIN0	IRQIN0
16	IRQOUT5	IRQOUT5	IRQOUT5
17	IRQOUT6	IRQOUT6	DRQIN1
18	IRQOUT7	IRQOUT7	DACKOUT1*
19	IRQOUT4	IRQOUT4	IRQOUT4
20	IRQOUT3	IRQOUT3	IRQOUT3
21	IRQOUT2	IRQOUT2	IRQOUT2
22	IRQOUT1	IRQOUT1	IRQOUT1
23	IRQOUT0	IRQOUT0	IRQOUT0
24	ISADRQ0	IRQOUT8 (Note 4)	ISADRQ0
25	ISADRQ1	IRQOUT9 (Note 4)	ISADRQ1
26	ISADRQ2	IRQOUT10 (Note 4)	ISADRQ2
27	ISADACK0*	NC	ISADACK0*
28	ISADACK1*	NC	ISADACK1*
29	ISADACK2*	NC	ISADACK2*
30	CS	CS	CS
31	SK	SK	SK
32	SA0	SA0	SA0

Pin #		Pin Name	
TQFP	Mode "00"	Mode "01"	Mode "10"
33	SA1	SA1	SA1
34	SA2	SA2	SA2
35	SA3	SA3	SA3
36	SA4	SA4	SA4
37	GND	GND	GND
38	SA5	SA5	SA5
39	SA6	SA6	SA6
40	SA7	SA7	SA7
41	SA8	SA8	SA8
42	SA9	SA9	SA9
43	SA10	SA10	SA10
44	SA11	SA11	SA11
45	SA12	SA12	SA12
46	SA13	SA13	SA13
47	SA14	SA14	SA14
48	SA15	SA15	SA15
49	SA16	SA16	SA16
50	SA17	SA17	SA17
51	DI	DI	DI
52	DO	DO	DO
53	SA18	SA18	SA18
54	SA19	SA19	SA19
55	AEN	AEN	AEN
56	OSC	OSC	OSC
57	SD0	SD0	SD0
58	SD1	SD1	SD1
59	SD2	SD2	SD2
60	SD3	SD3	SD3
61	SD4	SD4	SD4
62	SD5	SD5	SD5
63	SD6	SD6	SD6
64	SD7	SD7	SD7

Note 3: Mode selection (00, 01 or 10) is done by setting MS bits in the EEPROM configuration register. Detailed information about this is described in User's Guide.

Note 4: In Mode "01", IRQOUT8, 9, 10 are hardwired to ISA Bus interrupts IRQ10, IRQ11, IRQ12 respectively. This information supercedes the description in the "NM95MS15 User's Guide".

Absolute Maximum Ratings (Note 5)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	V_{CC} + 1V to -0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V Min

Operating Conditions

Ambient Operating Temperature NM95MS15	0°C to +70°C
Positive Power Supply (V_{CC})	4.5V to 5.5V

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min (Note 6)	Typ	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		6	20	mA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.2	15	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			15	µA
V_{IL}	Input Low Voltage			-0.1	0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 24 mA (Note 8) I_{OL} = 2.1 mA (Note 9)		0.4	V	
V_{OH}	Output High Voltage	I_{OH} = -3 mA (Note 8) I_{OH} = -400 µA (Note 9)	2.4 2.4		V V	

Capacitance T_A = +25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 7)	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 7)	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT} (Note 7)	Output Capacitance	V_{OUT} = 0V	6	pF

Note 5: Stresses above those listed under ≤Absolute Maximum Ratings≤ may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 6: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 7: This parameter is periodically sampled and not 100% tested.

Note 8: These values are for ISA signals SD[0:7], IRQx, DRQx.

Note 9: These values are for card signal IOCS[0:3]*, MEMCS[0:1]*, DO(EEPROM).

AC Electrical Characteristics

Symbol	Parameter	Min	Max	Unit
t_{AEN}	AEN Valid to Command Active	100		ns
t_{AC}	Address Valid to Command Active	88		ns
t_{RVD}	Active Read to Valid Data		200	ns
t_{AH}	Address, AEN Hold from Inactive Command	30		ns
t_{RDH}	Read Data Hold from Inactive Read		5	ns
t_{WD}	Write Data Valid before Write Active	22		ns
t_{WDH}	Write Data Hold after Write Inactive	25		ns
t_{CSA}	Chip Selects Valid from Address Valid	5	25	ns
t_{CSC}	Chip Selects Valid from Command Active	5	25	ns
t_{IDD}	Propagation Delay for IRQ/DRQ/DACK	5	25	ns

Resource Allocation Amongst the Two Logical Devices

NM95MS15 supports two Plug n Play logical devices: Logical Device #0, and Logical Device #1. The total resource structure supported by the NM95MS15 is allocated to each of these logical devices as follows:

Mode "00"

	Logical Device #0	*Logical Device #1*
1) I/O chipselects	IOCS0*	IOCS1*
2) Memory chipselects	MEMCS0*	MEMCS1*
3) Local IRQ input	IRQIN0	IRQIN1
4) Local DQR input	DRQIN0	—

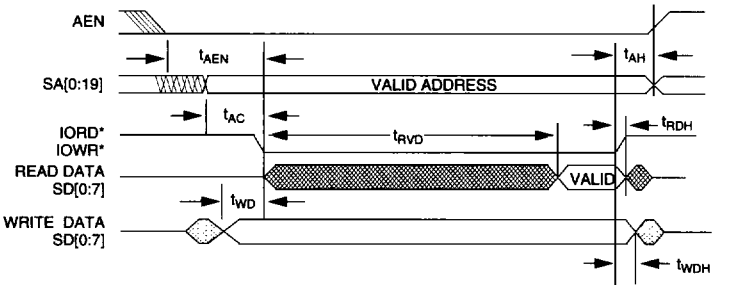
Mode "01"

	Logical Device #0	*Logical Device #1*
1) I/O chipselects	IOCS0* and IOCS2*	IOCS1* and IOCS3*
2) Memory chipselects	MEMCS0*	MEMCS1*
3) Local IRQ input	IRQIN0	IRQIN1

Mode "10"

	Logical Device #0	*Logical Device #1*
1) I/O chipselects	IOCS0*	IOCS1*
2) Memory chipselects	MEMCS0*	MEMCS1*
3) Local IRQ input	IRQIN0	IRQIN1
4) Local DQR input	DRQIN0	DRQIN1

(1) Timings for ISA Read/Write Cycle



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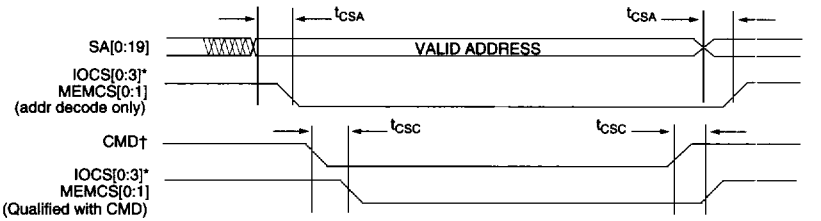
(2) Decode Delay for Chip select Generation



Note: CMD† means IORD*, IOWR*, SMEMR* and SMEMW*

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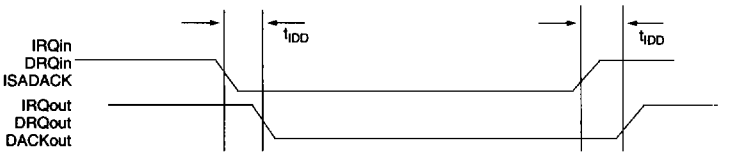
(3) Propagation Delay for IRQ/DRQ/DACK



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INTRODUCTION

The NM95MS15 is a single-chip solution for the ISA Plug and Play (PnP) specification. It implements the complete state machine and the necessary logic for supporting configurable interrupts and DMA channels on the ISA bus for one logical device. Apart from providing "PnP" capability, it has built-in EEPROM that eliminates external EEPROM. This device is available in a space saving 64-pin Thin Quad Flat Pack (TQFP) package.

Functional Description

NM95MS15 has three modes of operation, viz, "Normal DMA mode", "Extended Interrupt Mode" and "Extended DMA mode". These modes are programmed using the mode select (MS) bits in one of the configuration registers (Refer to the User's guide for detailed information). Each of these modes are discussed below.

Normal DMA Mode

In the Normal DMA mode, support is provided for

1. One on-board DMA request that is switchable to any three DMA channels on the ISA bus.
2. Two on-board interrupt request lines switchable to any eight IRQ lines on the ISA bus.
3. Two programmable I/O chip selects for on-board logic.
4. Two programmable Memory chip selects for on-board logic.

Figure 1 shows a Block Diagram of NM95MS15 configured for Normal DMA Mode.

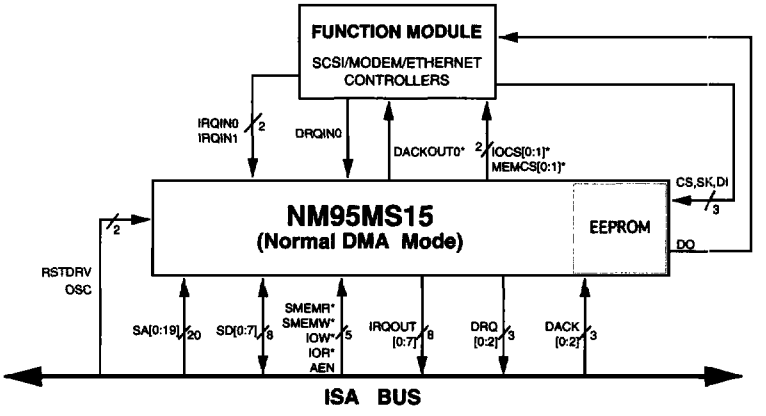

FIGURE 1.

Extended Interrupt Mode

In the Ext. Int mode, support is provided for:

1. Two on-board interrupt request lines switchable to any eleven IRQ lines on the ISA bus.
2. Four programmable I/O chip selects for on-board logic.
3. Two programmable Memory chip selects for on-board logic.

Figure 2 shows a Block Diagram of NM95MS15 configured for Extended Interrupt Mode.

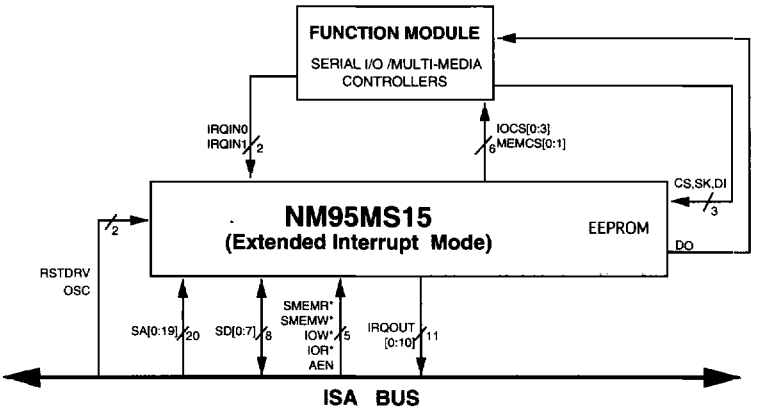

FIGURE 2.

Extended DMA Mode

In the Extended DMA mode, support is provided for:

1. Two on-board DMA request that is switchable to any three DMA channels on the ISA bus.
2. Two on-board interrupt request lines switchable to any six IRQ lines on the ISA bus.
3. Two programmable I/O chip selects for on-board logic.
4. Two programmable Memory chip selects for on-board logic.

Figure 3 shows a Block Diagram of NM95MS15 configured for Extended DMA Mode.

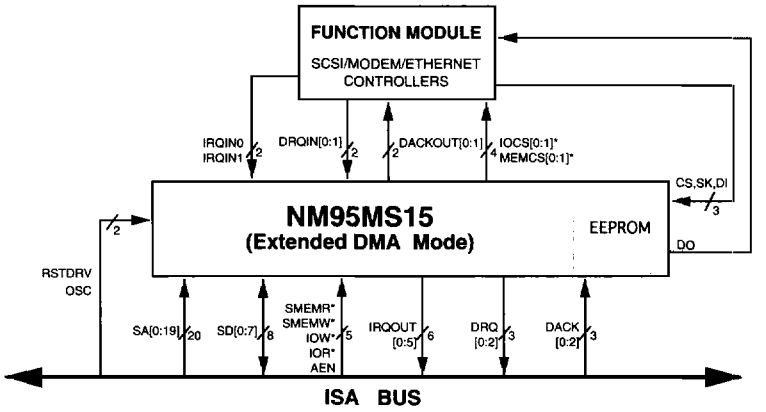

FIGURE 3.

Chip Select Generation

Individual I/O or Memory chip select can be generated in the following two ways:

A) Address Decode only

B) Address Decode qualified by Command (IORD*, IOWR* or SMEMR*, SMEMW*).

On-Chip EEPROM

NM95MS15 has 8k bits of EEPROM on chip. All the PnP resource data structure for the logical device is stored in this EEPROM. Of the 8k bits, 4k bits are available for the logical device's external usage. The logical device can access the EEPROM through a microwire port, which is essentially a 4-wire serial bus. The pins CS, SK, DI & DO follow the exact timing as the standard microwire bus and are compatible to the NM93Cxx family of EEPROMs.

EEPROM Programming

The entire 8k bits of EEPROM can be programmed throughthe ISA bus. The EEPROM can be programmed by puttingthe device (NM95MS15) in the Configuration state (as definedin the PnP standard). Under this state 4 registers at address 0xF0–0xF3 are accessible to program the EEPROM. The data to be programmed is loaded in register at address 0xF3 and 0xF2 (LSB and MSB

Ninth bit of address for 8k bits of memory is provided through the register at address 0xF0. Both read write are possible. The actual operation does not begin until Go Ahead (GA) bit is set. Programming a word takes approximately 10 ms. The status of the operation can be polled by the Status bit. This bit is set when the operation is in progress and will be reset when complete. The register at address 0xF0 is the COMMAND register. This is the handshake register in programming the EEPROM and is explained below in a tabular format.

COMMAND register	0xF0	Bit[1:0]	- OP Code bits 10 - Read operation 01 - Write operation
		Bit[2]	GA(Go ahead bits) If set to 1 the programming will continue.
		Bit[6:3]	- Reserved, should be 0.
		Bit[7]	- It provides A8 of the address. A[0:7] is provided by 0xF1 reg. (Note 10)
STATUS register	0x05	Bit[0]	- Status/Busy bit during programming "0" is busy, "1" is done.
Address Register	0xF1	Address Register [A0–A7]	
Data Register	0xF2	Data Byte [MSB]	
Data Register	0xF3	Data Byte [LSB]	

Note 10: The PNP resource data portion of the internal memory is at high address. Hence to program that portion, bit [7] of register 0xF0 (A8) should be set to 1.