

32-bit Microcontroller

CMOS

FR60Lite MB91230 Series

MB91233L/MB91F233A/MB91F233L/MB91V230

■ DESCRIPTION

The MB91230 series is a line of standard microcontrollers, based on a 32-bit high-performance RISC CPU and containing variety of I/O resources, for embedded control applications which require high CPU performance at high speed processing.

Audio motor control storage : Designed to specifications for embedded control applications which high CPU performance power processing.

The MB91230 series belongs to the FR60Lite.

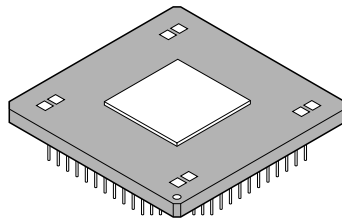
■ FEATURES

- 32-bit RISC, load/store architecture with a 5 stage pipeline
- Maximum operating frequency: 33.6 MHz (oscillation frequency = 4.2 MHz, oscillation frequency 8-multiplier (PLL clock multiplication method))
- 16-bit fixed length instructions (basic instructions)
- Execution speed of instructions : 1 instruction per cycle

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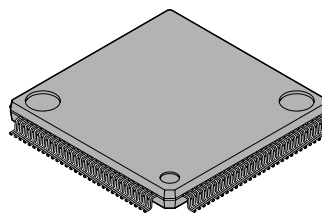
■ PACKAGES

401-pin Ceramic PGA



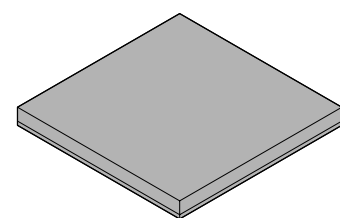
(PGA-401C-A02)

120-pin Plastic LQFP



(FPT-120P-M05)

128-pin plastic FLGA



(LGA-128P-M01)

MB91230 Series

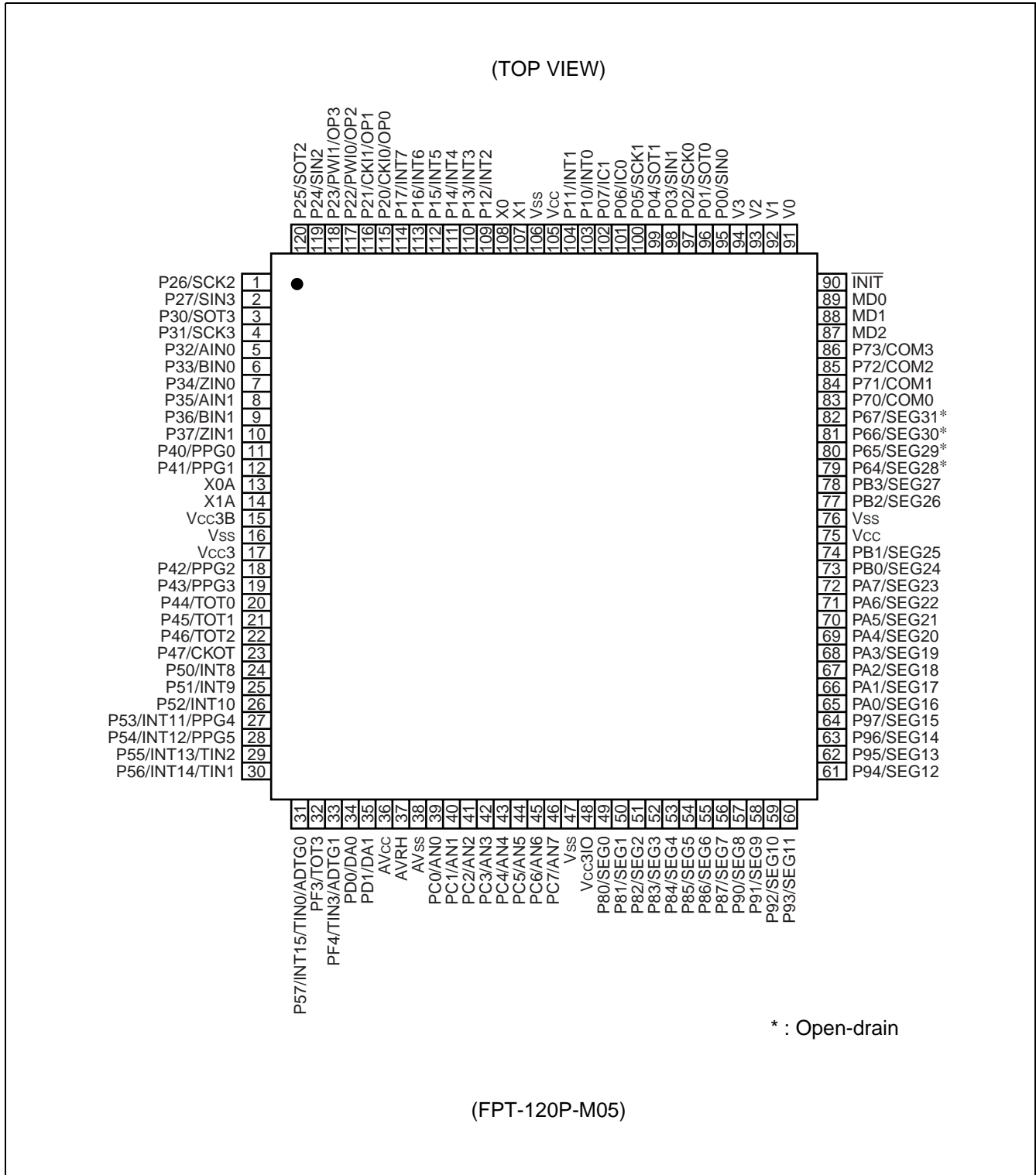
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- Memory-to-memory transfer, bit handling, and barrel shift instructions, etc. : Instructions suitable for embedded applications
- Function entry/exit instructions, multiple-register load/store instructions : Instructions adapted for C-language
- Register interlock function : Facilitates coding in assembler
- Built-in multiplier with instruction-level support
 - 32-bit multiplication with sign : 5 cycles
 - 16-bit multiplication with sign : 3 cycles
- Interrupt (PC and PS save) : 6 cycles (16 priority levels)
- Harvard architecture allowing program access and data access to be executed simultaneously
- Instruction compatible with FR family
- Capacity of built-in ROM and ROM type
 - MASK ROM : 256 Kbytes
 - FLASH ROM : 256 Kbytes
- Capacity of built-in RAM : 16 Kbytes
- General-purpose ports : Maximum 98 ports (including N-ch open-drain port : 4 ports)
- A/D converter (series-parallel type)
 - Resolution : 10-bit : 8 channels (4 channels × 2 unit)
 - Conversion time : 1.69 μs (Minimum conversion time)
- D/A converter (R-2R type)
 - Resolution : 8-bit : 2 channels (independence)
 - Conversion speed : 0.6 μs (when load capacitance 20 pF)
- External interrupt input : 16 channels
- Bit search module (for REALOS)
 - Function for searching the MSB (Upper bit) in each word for the first “0” or “1” inverted point
- UART (full-duplex double buffer) : 4 channels
 - Selectable parity On/Off
 - Asynchronous (start-stop synchronized) or clock-synchronous communications selectable
 - Internal timer for dedicated baud rate (U-timer) on each channel
 - External clock can be used as transfer clock
 - Error detection function for parity, frame and overrun
- PPG : 16-bit × 6 channels
- Up/down counter : 2 channels (8-bit × 2 channels or 16-bit × 1 channel)
- Reload timer : 16-bit × 4 channels
- Free-run timer : 16-bit × 2 channels
- Watch timer : 15-bit × 1 channel
- PWC : 8-bit × 2 channels
- Input capture : 2 channels (interface with free-run timer 0)
- Output compare : 4 channels (free-run timer 0 and output compare unit 0/1 cooperate, free-run timer 1 and output compare units 2/3)
- LCD controller : SEG0 to SEG31/COM0 to COM3 (also serving as a port)
- Clock monitor (peripheral clock output function) : 1 channel
- Timebase/watchdog timer (26-bit)
- Real-time clock (counting even with the real-time clock stopped)
- Low Power Consumption Mode
- Sleep/stop function
- Package : LQFP-120, FLGA-128
- Technology : CMOS 0.35 μm
- Power supply
- Dual power supply configuration [internal logic 3.3 V, I/O 5.5 V(3.3 V for A/D converter and D/A converter input/output)]

Note : Do not set the external bus mode in which the MB91230 series cannot operate.

PIN ASSIGNMENT

- MB91233L, MB91F233A, MB91F233L

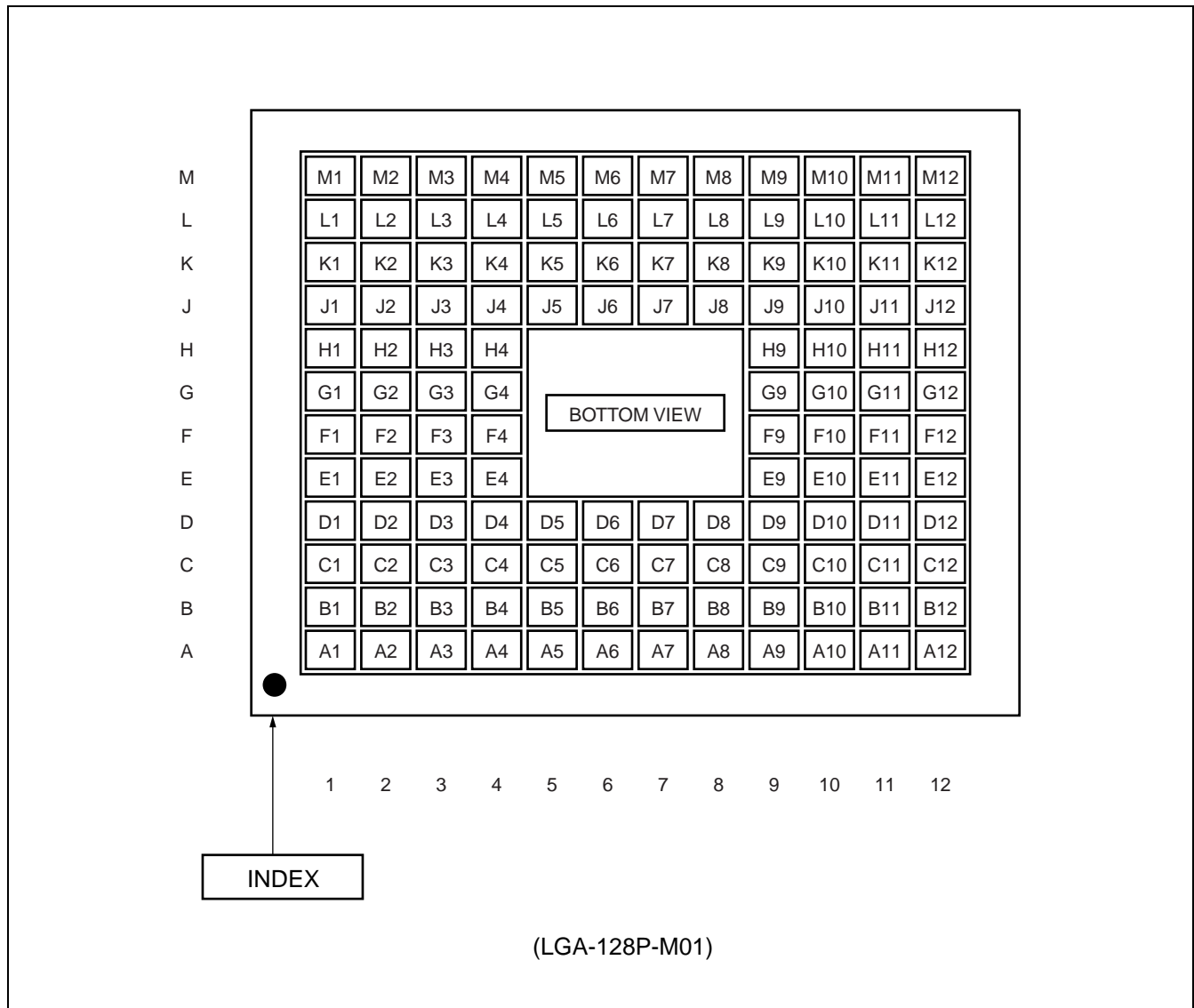


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MB91230 Series

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• MB91F233L



MB91230 Series

Pin correspondence table of LQFP-120 and FLGA-128 in MB91230 series (LGA-128P-M01)

| LQFP-120 No. | FLGA-128 No. (JEDEC No.) | Signal name | LQFP-120 No. | FLGA-128 No. (JEDEC No.) | Signal name | LQFP-120 No. | FLGA-128 No. (JEDEC No.) | Signal name |
|--------------|--------------------------|--------------------------|--------------|--------------------------|-----------------|--------------|--------------------------|---------------------|
| 1 | A1 | P26/SCK2 | 98 | C9 | P03/SIN1 | 18 | G1 | P42/PPG2 |
| 120 | A2 | P25/SOT2 | 93 | C10 | V2 | 15 | G2 | V _{cc} 3B |
| 117 | A3 | P22/PWI0/ OP2 | 85 | C11 | P72/COM2 | *2 | G3*4 | V _{cc} 3*4 |
| 114 | A4 | P17/INT7 | 87 | C12 | MD2 | 17 | G4 | V _{cc} 3 |
| — | A5 | *5 | 10 | D1 | P37/ZIN1 | 71 | G9 | PA6/ SEG22 |
| 109 | A6 | P12/INT2 | 6 | D2 | P33/BIN0 | 75 | G10 | V _{cc} |
| 107 | A7 | X1 | 8 | D3 | P35/AIN1 | 74 | G11 | PB1/ SEG25 |
| 103 | A8 | P10/INT0 | 119 | D4 | P24/SIN2 | 77 | G12 | PB2/ SEG26 |
| 100 | A9 | P05/SCK1 | 111 | D5 | P14/INT4 | 21 | H1 | P45/TOT1 |
| 97 | A10 | P02/SCK0 | — | D6 | *5 | 19 | H2 | P43/PPG3 |
| 94 | A11 | V3 | 101 | D7 | P06/IC0 | 23 | H3 | P47/CKOT |
| 91 | A12 | V0 | 95 | D8 | P00/SIN0 | 20 | H4 | P44/TOT0 |
| 4 | B1 | P31/SCK3 | 89 | D9 | MD0 | 65 | H9 | PA0/ SEG16 |
| 118 | B2 | P23/PWI1/ OP3 | 86 | D10 | P73/COM3 | 72 | H10 | PA7/ SEG23 |
| 115 | B3 | P20/CKI0/ OP0 | 82 | D11 | P67/ SEG31*1 | 69 | H11 | PA4/ SEG20 |
| 112 | B4 | P15/INT5 | 84 | D12 | P71/COM1 | 73 | H12 | PB0/ SEG24 |
| 110 | B5 | P13/INT3 | 13 | E1 | X0A | 24 | J1 | P50/INT8 |
| 106 | B6 | V _{ss} | 9 | E2 | P36/BIN1 | 22 | J2 | P46/TOT2 |
| 104 | B7 | P11/INT1 | 12 | E3 | P41/PPG1 | 26 | J3 | P52/INT10 |
| 99 | B8 | P04/SOT1 | 5 | E4 | P32/AIN0 | 29 | J4 | P55/INT13/ TIN2 |
| 96 | B9 | P01/SOT0 | 81 | E9 | P66/ SEG30*1 | 35 | J5 | PD1/DA1 |
| 92 | B10 | V1 | 83 | E10 | P70/COM0 | 40 | J6 | PC1/AN1 |
| 88 | B11 | MD1 | 80 | E11 | P65/ SEG29*1 | 47 | J7 | V _{ss} |
| 90 | B12 | $\overline{\text{INIT}}$ | — | E12 | *5 | 50 | J8 | P81/SEG1 |

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MB91230 Series

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| LQFP-120 No. | FLGA-128 No. (JEDEC No.) | Signal name | LQFP-120 No. | FLGA-128 No. (JEDEC No.) | Signal name | LQFP-120 No. | FLGA-128 No. (JEDEC No.) | Signal name |
|--------------|--------------------------|---------------------|--------------|--------------------------|----------------------|--------------|--------------------------|------------------|
| 7 | C1 | P34/ZIN0 | 16 | F1 | V _{SS} | 59 | J9 | P92/SEG10 |
| 2 | C2 | P27/SIN3 | — | F2 | *5 | 68 | J10 | PA3/SEG19 |
| 3 | C3 | P30/SOT3 | 14 | F3 | X1A | 66 | J11 | PA1/SEG17 |
| 116 | C4 | P21/CK11/OP1 | 11 | F4 | P40/PPG0 | 70 | J12 | PA5/SEG21 |
| 113 | C5 | P16/INT6 | 78 | F9 | PB3/SEG27 | 27 | K1 | P53/INT11/PPG4 |
| 108 | C6 | X0 | 79 | F10 | P64/SEG28*1 | 25 | K2 | P51/INT9 |
| 105 | C7 | V _{CC} | 76 | F11 | V _{SS} | 33 | K3 | PF4/TIN3/ADTG1 |
| 102 | C8 | P07/IC1 | — | F12 | *5 | 38 | K4 | AV _{SS} |
| 41 | K5 | PC2/AN2 | 36 | L4 | AV _{CC} | 37 | M3 | AVRH |
| 44 | K6 | PC5/AN5 | *3 | L5*4 | AVRL*4 | 39 | M4 | PC0/AN0 |
| 48 | K7 | V _{CC} 3IO | 43 | L6 | PC4/AN4 | 42 | M5 | PC3/AN3 |
| 53 | K8 | P84/SEG4 | 45 | L7 | PC6/AN6 | 46 | M6 | PC7/AN7 |
| 56 | K9 | P87/SEG7 | 49 | L8 | P80/SEG0 | — | M7 | *5 |
| 63 | K10 | P96/SEG14 | 52 | L9 | P83/SEG3 | 51 | M8 | P82/SEG2 |
| 62 | K11 | P95/SEG13 | 55 | L10 | P86/SEG6 | 54 | M9 | P85/SEG5 |
| 67 | K12 | PA2/SEG18 | 58 | L11 | P91/SEG9 | 57 | M10 | P90/SEG8 |
| 30 | L1 | P56/INT14/TIN1 | 64 | L12 | P97/SEG15 | 60 | M11 | P93/SEG11 |
| 28 | L2 | P54/INT12/PPG5 | 31 | M1 | P57/INT15/TIN0/ADTG0 | 61 | M12 | P94/SEG12 |
| 32 | L3 | PF3/TOT3 | 34 | M2 | PD0/DA0 | | | |

*1 : Open-drain

*2 : Connected to pin 17(V_{CC}3) on the LQFP product

*3 : Connected to pin 38(AV_{SS}) on the LQFP product

*4 : Signals added to the FLGA product

*5 : NC pin on the FLGA product

■ PIN DESCRIPTION

| Pin no. | | Pin name | Circuit type | Description |
|---------|------|----------|--------------|---|
| LQFP | FLGA | | | |
| 1 | A1 | SCK2 | D | UART2 clock input/output. This function is valid when corresponding bit of PFR2 register is set to peripheral function. |
| | | P26 | | General purpose input/output port. This function is valid when corresponding bit of PFR2 register is set to port function. |
| 2 | C2 | SIN3 | D | UART3 data input. When using this function, corresponding bit of DDR2 register is set to input. |
| | | P27 | | General purpose input/output port. This function is always valid. |
| 3 | C3 | SOT3 | B | UART3 data output. This function is valid when corresponding bit of PFR3 register is set to peripheral function. |
| | | P30 | | General purpose input/output port. This function is valid when corresponding bit of PFR3 register is set to port function. |
| 4 | B1 | SCK3 | B | UART3 clock input/output. This function is valid when corresponding bit of PFR3 register is set to peripheral function. |
| | | P31 | | General purpose input/output port. This function is valid when corresponding bit of PFR3 register is set to port function. |
| 5 | E4 | AIN0 | B | Up/down counter 0 AIN input. When using this function, corresponding bit of DDR3 register is set to input. |
| | | P32 | | General purpose input/output port. This function is always valid. |
| 6 | D2 | BIN0 | B | Up/down counter 0 BIN input. When using this function, corresponding bit of DDR3 register is set to input. |
| | | P33 | | General purpose input/output port. This function is always valid. |
| 7 | C1 | ZIN0 | B | Up/down counter 0 ZIN input. When using this function, corresponding bit of DDR3 register is set to input. |
| | | P34 | | General purpose input/output port. This function is always valid. |
| 8 | D3 | AIN1 | B | Up/down counter 1 AIN input. When using this function, corresponding bit of DDR3 register is set to input. |
| | | P35 | | General purpose input/output port. This function is always valid. |

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MB91230 Series

| Pin no. | | Pin name | Circuit type | Description |
|---------|------|--------------------|--------------|---|
| LQFP | FLGA | | | |
| 9 | E2 | BIN1 | B | Up/down counter 1 BIN input. When using this function, corresponding bit of DDR3 register is set to input. |
| | | P36 | | General purpose input/output port. This function is always valid. |
| 10 | D1 | ZIN1 | B | Up/down counter 1 ZIN input. When using this function, corresponding bit of DDR3 register is set to input. |
| | | P37 | | General purpose input/output port. This function is always valid. |
| 11 | F4 | PPG0 | D | PPG0 output. This function is valid when corresponding bit of PFR4 register is set to peripheral function. |
| | | P40 | | General purpose input/output port. This function is valid when corresponding bit of PFR4 register is set to port function. |
| 12 | E3 | PPG1 | D | PPG1 output. This function is valid when corresponding bit of PFR4 register is set to peripheral function. |
| | | P41 | | General purpose input/output port. This function is valid when corresponding bit of PFR4 register is set to port function. |
| 13 | E1 | X0A | K | Sub-clock oscillation pin (32 kHz) |
| 14 | F3 | X1A | | |
| 15 | G2 | V _{cc} 3B | — | Power supply pin for backup (RTC) |
| 16 | F1 | V _{ss} | — | Power supply pin (GND) |
| 17 | G4 | V _{cc} 3 | — | Power supply pin (3.3 V internal logic) |
| 18 | G1 | PPG2 | D | PPG2 output. This function is valid when corresponding bit of PFR4 register is set to peripheral function. |
| | | P42 | | General purpose input/output port. This function is valid when corresponding bit of PFR4 register is set to port function. |
| 19 | H2 | PPG3 | D | PPG3 output. This function is valid when corresponding bit of PFR4 register is set to peripheral function. |
| | | P43 | | General purpose input/output port. This function is valid when corresponding bit of PFR4 register is set to port function. |

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MB91230 Series

| Pin no. | | Pin name | Circuit type | Description |
|---------|------|----------|--------------|---|
| LQFP | FLGA | | | |
| 20 | H4 | TOT0 | D | Reload timer 0 output port. This function is valid when corresponding bit of PFR4 register is set to peripheral function. |
| | | P44 | | General purpose input/output port. This function is valid when corresponding bit of PFR4 register is set to port function. |
| 21 | H1 | TOT1 | D | Reload timer 1 output port. This function is valid when corresponding bit of PFR4 register is set to peripheral function. |
| | | P45 | | General purpose input/output port. This function is valid when corresponding bit of PFR4 register is set to port function. |
| 22 | J2 | TOT2 | D | Reload timer 2 output port. This function is valid when corresponding bit of PFR4 register is set to peripheral function. |
| | | P46 | | General purpose input/output port. This function is valid when corresponding bit of PFR4 register is set to port function. |
| 23 | H3 | CKOT | D | Clock monitor function output pin. This function is valid when corresponding bit of PFR4 register is set to peripheral function. |
| | | P47 | | General purpose input/output port. This function is valid when corresponding bit of PFR4 register is set to port function. |
| 24 | J1 | INT8 | C | External interrupt input. When using this function, corresponding bit of DDR5 register is set to input. |
| | | P50 | | General purpose input/output port. This function is always valid. |
| 25 | K2 | INT9 | C | External interrupt input. When using this function, corresponding bit of DDR5 register is set to input. |
| | | P51 | | General purpose input/output port. This function is always valid. |
| 26 | J3 | INT10 | C | External interrupt input. When using this function, corresponding bit of DDR5 register is set to input. |
| | | P52 | | General purpose input/output port. This function is always valid. |

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MB91230 Series

| Pin no. | | Pin name | Circuit type | Description |
|---------|------|----------|--------------|---|
| LQFP | FLGA | | | |
| 27 | K1 | PPG4 | C | PPG4 output. This function is valid when corresponding bit of PFR5 register is set to peripheral function. |
| | | INT11 | | External interrupt input. This function is enabled when corresponding bit of PFR5 register is set to port function and corresponding bit of DDR5 register is set to input. |
| | | P53 | | General purpose input/output port. This function is valid when corresponding bit of PFR5 register is set to port function. |
| 28 | L2 | PPG5 | C | PPG5 output. This function is valid when corresponding bit of PFR5 register is set to peripheral function. |
| | | INT12 | | External interrupt input. This function is enabled when corresponding bit of PFR5 register is set to port function and corresponding bit of DDR5 register is set to input. |
| | | P54 | | General purpose input/output port. This function is valid when corresponding bit of PFR5 register is set to port function. |
| 29 | J4 | TIN2 | C | Reload timer 2 event input pin. This function is valid when corresponding bit of DDR5 register is set to input. |
| | | INT13 | | External interrupt input. This function is valid when corresponding bit of DDR5 register is set to input. |
| | | P55 | | General purpose input/output port. This function is always valid. |
| 30 | L1 | TIN1 | C | Reload timer 1 event input pin. This function is valid when corresponding bit of DDR5 register is set to input. |
| | | INT14 | | External interrupt input. This function is valid when corresponding bit of DDR5 register is set to input. |
| | | P56 | | General purpose input/output port. This function is always valid. |

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MB91230 Series

| Pin no. | | Pin name | Circuit type | Description |
|---------|------|------------------|--------------|---|
| LQFP | FLGA | | | |
| 31 | M1 | ADTG0 | C | External trigger input pin of A/D converter 0. This function is valid when corresponding bit of DDR5 register is set to input. |
| | | TIN0 | | Reload timer 0 event input pin. This function is valid when corresponding bit of DDR5 register is set to input. |
| | | INT15 | | External interrupt input. This function is valid when corresponding bit of DDR5 register is set to input. |
| | | P57 | | General purpose input/output port. This function is always valid. |
| 32 | L3 | TOT3 | D | Reload timer 3 output port. This function is valid when corresponding bit of PFRF register is set to peripheral function. |
| | | PF3 | | General purpose input/output port. This function is valid when corresponding bit of PFRF register is set to port function. |
| 33 | K3 | ADTG1 | D | External trigger input pin of A/D converter 1. This function is valid when corresponding bit of DDRF register is set to input. |
| | | TIN3 | | Reload timer 3 event input pin. This function is valid when corresponding bit of DDRF register is set to input. |
| | | PF4 | | General purpose input/output port. This function is always valid. |
| 34 | M2 | DA0 | F | D/A converter 0 output pin. This function is valid when corresponding bit of PFRD register is set to peripheral function. |
| | | PD0 | | General purpose input/output port. This function is valid when corresponding bit of PFRD register is set to port function. |
| 35 | J5 | DA1 | F | D/A converter 1 output pin. This function is valid when corresponding bit of PFRD register is set to peripheral function. |
| | | PD1 | | General purpose input/output port. This function is valid when corresponding bit of PFRD register is set to port function. |
| 36 | L4 | AV _{cc} | — | Analog power supply (for A/D, D/A converter) . |
| 37 | M3 | AVRH | — | Analog reference power supply (for A/D, D/A converter) . |
| 38 | K4 | AV _{ss} | — | GND level input for analog circuit (for A/D, D/A converter) . |

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MB91230 Series

| Pin no. | | Pin name | Circuit type | Description |
|----------|---|--------------------|--------------|--|
| LQFP | FLGA | | | |
| 39 to 46 | M4, J6, K5, M5, L6, K6, L7, M6 | AN0 to AN7 | E | Analog input pin for A/D converter. This function is valid when corresponding bit of PFRC register is set to peripheral function. |
| | | PC0 to PC7 | | General purpose input/output port. This function is valid when corresponding bit of PFRC register is set to port function. |
| 47 | J7 | V _{SS} | — | Power supply pin (GND) |
| 48 | K7 | V _{CC3IO} | — | Power supply pin (analog-shared pin I/O) |
| 49 to 56 | L8, J8, M8, L9, K8, M9, L10, K9 | SEG0 to SEG7 | I | LCD controller/driver LCD segment output pin. This function is valid when corresponding bit of PFR8 register is set to peripheral function. |
| | | P80 to P87 | | General purpose input/output port. This function is valid when corresponding bit of PFR8 register is set to port function. |
| 57 to 64 | M10, L11, J9, M11, M12, K11, K10, L12 | SEG8 to SEG15 | I | LCD controller/driver LCD segment output pin. This function is valid when corresponding bit of PFR9 register is set to peripheral function. |
| | | P90 to P97 | | General purpose input/output port. This function is valid when corresponding bit of PFR9 register is set to port function. |
| 65 to 72 | H9, J11, K12, J10, H11, J12, G9, H10 | SEG16 to SEG23 | I | LCD controller/driver LCD segment output pin. This function is valid when corresponding bit of PFRA register is set to peripheral function. |
| | | PA0 to PA7 | | General purpose input/output port. This function is valid when corresponding bit of PFRA register is set to port function. |
| 73, 74 | H12, G11 | SEG24, SEG25 | I | LCD controller/driver LCD segment output pin. This function is valid when corresponding bit of PFRB register is set to peripheral function. |
| | | PB0, PB1 | | General purpose input/output port. This function is valid when corresponding bit of PFRB register is set to port function. |
| 75 | G10 | V _{CC} | — | Power supply pin (5 V I/O MB91V230/F233A) |
| | | | | Power supply pin (3.3 V internal logic, I/O MB91F233L/MB91233L) |
| 76 | F11 | V _{SS} | — | Power supply pin (GND) |
| 77, 78 | G12, F9 | SEG26, SEG27 | I | LCD controller/driver LCD segment output pin. This function is valid when corresponding bit of PFRB register is set to peripheral function. |
| | | PB2, PB3 | | General purpose input/output port. This function is valid when corresponding bit of PFRB register is set to port function. |

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MB91230 Series

| Pin no. | | Pin name | Circuit type | Description |
|----------|--------------------|--------------------------|--------------|---|
| LQFP | FLGA | | | |
| 79 to 82 | F10, E11, E9, D11 | SEG28 to SEG31 | J | LCD controller/driver LCD segment output pin. This function is valid when corresponding bit of PFR6 register is set to peripheral function. |
| | | P64 to P67 | | General purpose input/output port. (open-drain) This function is valid when corresponding bit of PFR6 register is set to port function. |
| 83 to 86 | E10, D12, C11, D10 | COM0 to COM3 | I | LCD controller/driver common pins. This function is valid when corresponding bit of PFR7 register is set to peripheral function. |
| | | P70 to P73 | | General purpose input/output port. This function is valid when corresponding bit of PFR7 register is set to port function. |
| 87 to 89 | C12, B11, D9 | MD2, MD1, MD0 | H | Mode input pin. |
| 90 | B12 | $\overline{\text{INIT}}$ | G | External reset input. |
| 91 to 94 | A12, B10, C10, A11 | V0 to V3 | — | LCD controller/driver reference power supply input pins. |
| 95 | D8 | SIN0 | D | UART0 data input. When using this function, corresponding bit of DDR0 register is set to input. |
| | | P00 | | General purpose input/output port. This function is always valid. |
| 96 | B9 | SOT0 | D | UART0 data output. This function is valid when corresponding bit of PFR0 register is set to peripheral function. |
| | | P01 | | General purpose input/output port. This function is valid when corresponding bit of PFR0 register is set to port function. |
| 97 | A10 | SCK0 | D | UART0 clock input/output. This function is valid when corresponding bit of PFR0 register is set to peripheral function. |
| | | P02 | | General purpose input/output port. This function is valid when corresponding bit of PFR0 register is set to port function. |
| 98 | C9 | SIN1 | D | UART1 data input. This function is valid when corresponding bit of DDR0 register is set to input. |
| | | P03 | | General purpose input/output port. This function is always valid. |

(Continued)

MB91230 Series

| Pin no. | | Pin name | Circuit type | Description |
|---------|------|-----------------|--------------|---|
| LQFP | FLGA | | | |
| 99 | B8 | SOT1 | D | UART1 data output. This function is valid when corresponding bit of PFR0 register is set to peripheral function. |
| | | P04 | | General purpose input/output port. This function is valid when corresponding bit of PFR0 register is set to port function. |
| 100 | A9 | SCK1 | D | UART1 clock input/output. This function is valid when corresponding bit of PFR0 register is set to peripheral function. |
| | | P05 | | General purpose input/output port. This function is valid when corresponding bit of PFR0 register is set to port function. |
| 101 | D7 | IC0 | D | Input capture input 0. This function is valid when corresponding bit of DDR0 register is set to input. |
| | | P06 | | General purpose input/output port. This function is always valid. |
| 102 | C8 | IC1 | D | Input capture input 1. This function is valid when corresponding bit of DDR0 register is set to input. |
| | | P07 | | General purpose input/output port. This function is always valid. |
| 103 | A8 | INT0 | A | External interrupt input. This function is valid when corresponding bit of DDR1 register is set to input. |
| | | P10 | | General purpose input/output port. This function is always valid. |
| 104 | B7 | INT1 | A | External interrupt input. This function is valid when corresponding bit of DDR1 register is set to input. |
| | | P11 | | General purpose input/output port. This function is always valid. |
| 105 | C7 | V _{cc} | — | Power supply pin (5 V I/O MB91V230/F233A) |
| | | | | Power supply pin (3.3 V internal logic, I/O MB91F233L/MB91233L) |
| 106 | B6 | V _{ss} | — | Power supply pin (GND) |
| 107 | A7 | X1 | K | Main-clock oscillation pin |
| 108 | C6 | X0 | | |

(Continued)

MB91230 Series

| Pin no. | | Pin name | Circuit type | Description |
|---------|------|----------|--------------|--|
| LQFP | FLGA | | | |
| 109 | A6 | INT2 | A | External interrupt input. This function is valid when corresponding bit of DDR1 register is set to input. |
| | | P12 | | General purpose input/output port. This function is always valid. |
| 110 | B5 | INT3 | A | External interrupt input. This function is valid when corresponding bit of DDR1 register is set to input. |
| | | P13 | | General purpose input/output port. This function is always valid. |
| 111 | D5 | INT4 | A | External interrupt input. This function is valid when corresponding bit of DDR1 register is set to input. |
| | | P14 | | General purpose input/output port. This function is always valid. |
| 112 | B4 | INT5 | A | External interrupt input. This function is valid when corresponding bit of DDR1 register is set to input. |
| | | P15 | | General purpose input/output port. This function is always valid. |
| 113 | C5 | INT6 | A | External interrupt input. This function is valid when corresponding bit of DDR1 register is set to input. |
| | | P16 | | General purpose input/output port. This function is always valid. |
| 114 | A4 | INT7 | A | External interrupt input. This function is valid when corresponding bit of DDR1 register is set to input. |
| | | P17 | | General purpose input/output port. This function is always valid. |
| 115 | B3 | CKI0 | D | External clock input pin for free-run timer 0. This function is enabled when corresponding bit of PFR2 register is set to port function and corresponding bit of DDR2 register is set to input. |
| | | OP0 | | Output compare 0 output pin. This function is valid when corresponding bit of PFR2 register is set to peripheral function. |
| | | P20 | | General purpose input/output port. This function is valid when corresponding bit of PFR2 register is set to port function. |

(Continued)

MB91230 Series

(Continued)

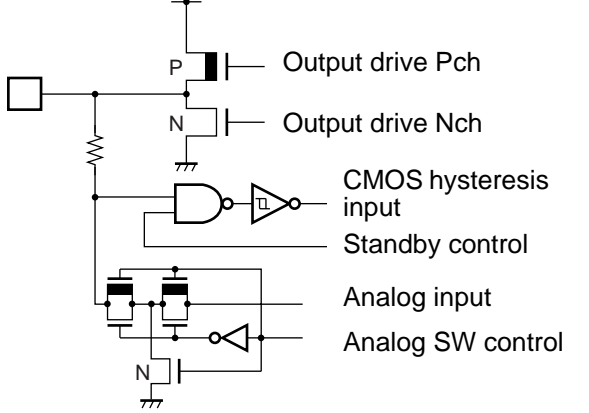
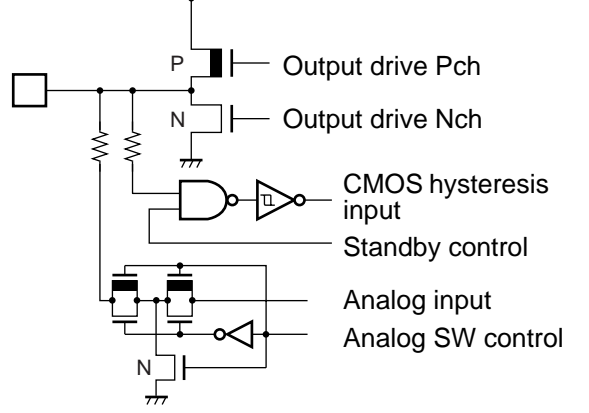
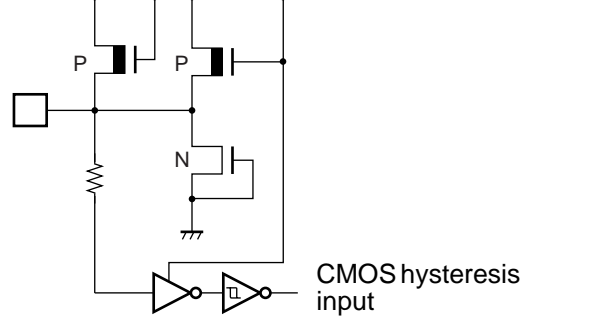
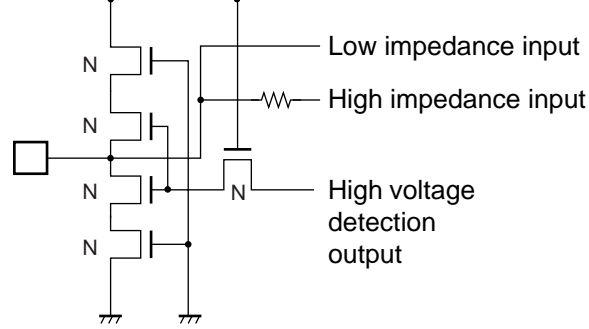
| Pin no. | | Pin name | Circuit type | Description |
|---------|--------------------------|----------|--------------|--|
| LQFP | FLGA | | | |
| 116 | C4 | CKI1 | D | External clock input pin for free-run timer 1. This function is enabled when corresponding bit of PFR2 register is set to port function and corresponding bit of DDR2 register is set to input. |
| | | OP1 | | Output compare1 output pin. This function is valid when corresponding bit of PFR2 register is set to peripheral function. |
| | | P21 | | General purpose input/output port. This function is valid when corresponding bit of PFR2 register is set to port function. |
| 117 | A3 | PWI0 | D | Pulse width counter 0 input. This function is enabled when corresponding bit of PFR2 register is set to port function and corresponding bit of DDR2 register is set to input. |
| | | OP2 | | Output compare2 output pin. This function is valid when corresponding bit of PFR2 register is set to peripheral function. |
| | | P22 | | General purpose input/output port. This function is valid when corresponding bit of PFR2 register is set to port function. |
| 118 | B2 | PWI1 | D | Pulse width counter 1 input. This function is enabled when corresponding bit of PFR2 register is set to port function and corresponding bit of DDR2 register is set to input. |
| | | OP3 | | Output compare3 output pin. This function is valid when corresponding bit of PFR2 register is set to peripheral function. |
| | | P23 | | General purpose input/output port. This function is valid when corresponding bit of PFR2 register is set to port function. |
| 119 | D4 | SIN2 | D | UART2 data input. This function is valid when corresponding bit of DDR2 register is set to input. |
| | | P24 | | General purpose input/output port. This function is always valid. |
| 120 | A2 | SOT2 | D | UART2 data output. This function is valid when corresponding bit of PFR2 register is set to peripheral function. |
| | | P25 | | General purpose input/output port. This function is valid when corresponding bit of PFR2 register is set to port function. |
| (38) | L5 | AVRL | — | Analog reference power supply (for A/D converter) AVRL pin is connected to AV _{ss} inside the IC on LQFP package product. |
| — | A5, D6, E12, F2, F12, M7 | NC | — | Unconnected pin. |

I/O CIRCUIT TYPE

| Type | Circuit type | Remarks |
|------|---|--|
| A | <p> Pull-up control Output drive Pch Output drive Nch CMOS hysteresis input Standby control </p> | With Pull-up control (50 kΩ) CMOS level output $I_{OH} = 4 \text{ mA}/I_{OL} = 4 \text{ mA}$ CMOS hysteresis input (with standby control) |
| B | <p> Pull-up control Output drive Pch Output drive Nch CMOS hysteresis input Standby control Test pin for FLASH Analog SW control </p> | With Pull-up control (50 kΩ) CMOS level output $I_{OH} = 4 \text{ mA}/I_{OL} = 4 \text{ mA}$ CMOS hysteresis input (with standby control) Test pin for FLASH |
| C | <p> Output drive Pch Output drive Nch CMOS hysteresis input Standby control </p> | CMOS level output CMOS hysteresis input (with standby control) |
| D | <p> Output drive Pch Output drive Nch CMOS hysteresis input Standby control Test pin for FLASH Analog SW control </p> | CMOS level output $I_{OH} = 4 \text{ mA}/I_{OL} = 4 \text{ mA}$ CMOS hysteresis input (with standby control) Test pin for FLASH |

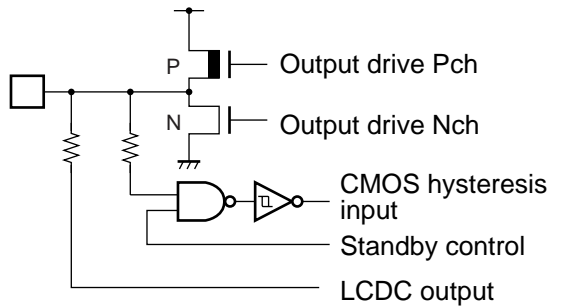
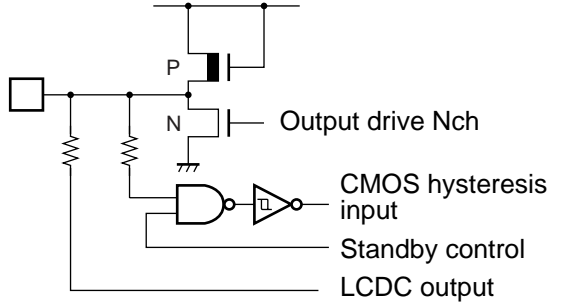
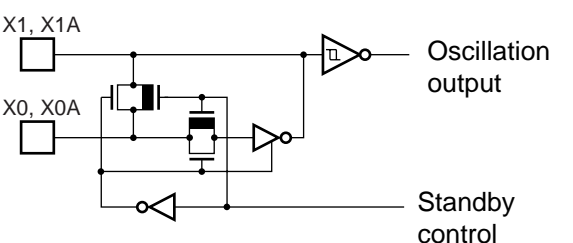
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MB91230 Series

| Type | Circuit type | Remarks |
|------|--|---|
| E |  <p>Output drive Pch Output drive Nch CMOS hysteresis input Standby control Analog input Analog SW control</p> | <p>CMOS level output $I_{OH} = 4 \text{ mA}/I_{OL} = 4 \text{ mA}$ CMOS hysteresis input (with standby control) Also serving as an analog input</p> |
| F |  <p>Output drive Pch Output drive Nch CMOS hysteresis input Standby control Analog input Analog SW control</p> | <p>CMOS level output $I_{OH} = 4 \text{ mA}/I_{OL} = 4 \text{ mA}$ CMOS hysteresis input (with standby control) Also serving as an analog input</p> |
| G |  <p>CMOS hysteresis input</p> | <p>With Pull-up ($50 \text{ k}\Omega$) CMOS hysteresis input</p> |
| H |  <p>Low impedance input High impedance input High voltage detection output</p> | <p>High withstand-voltage input CMOS input (hysteresis level)</p> |

(Continued)

(Continued)

| Type | Circuit type | Remarks |
|------|---|---|
| I |  | <p>CMOS level output $I_{OH} = 4 \text{ mA}/I_{OL} = 4 \text{ mA}$ CMOS hysteresis input (with standby control) LCDC output</p> |
| J |  | <p>CMOS level output (open-drain) $I_{OL} = 20 \text{ mA}$ CMOS hysteresis input (with standby control) LCDC output</p> |
| K |  | <p>Oscillation circuit</p> |

MB91230 Series

■ HANDLING DEVICES

Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage greater than V_{CC} or less than V_{SS} is applied to an input or output pin or if an above-rating voltage is applied between V_{CC} and V_{SS} .

A latch-up, if it occurs, significantly increases the power supply current and may cause thermal destruction of an element. When you use a CMOS IC, be very careful not to exceed the absolute maximum rating.

Treatment of Unused Pins

Do not leave an unused input pin open, since it may cause a malfunction. Handle by, for example, using a pull-up or pull-down resistor.

Treatment of Pins at Unusing LCD

Leave COM0 to COM3 pins open.

V0 to V3 pins should always be pulled up or down through resistance of at least 2 k Ω .

About Power Supply Pins

In products with multiple V_{CC} or V_{SS} pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to external power supply and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the V_{CC} and V_{SS} pins of this device at the low impedance.

It is also advisable to connect a ceramic bypass capacitor of approximately 0.1 μF between V_{CC} and V_{SS} near this device.

About Crystal Oscillator Circuit

Noise near the X0, X1, X0A and X1A pins may cause the device to malfunction. Design the printed circuit board so that X0, X1, X0A and X1A the crystal oscillator (or ceramic oscillator) , and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended to design the PC board artwork with the X0, X1, X0A and X1A pins surrounded by ground plane because stable operation can be expected with such a layout.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

Treatment of NC and OPEN Pins

Pins marked as NC and OPEN must be left open-circuit.

About Mode Pins (MD0 to MD2)

These pins should be connected directly to V_{CC} or V_{SS} .

To prevent the device erroneously switching to test mode due to noise, design the printed circuit board such that the distance between the mode pins and V_{CC} or V_{SS} is as short as possible and the connection impedance is low.

Operation at Start-up

Be sure to execute setting initialized reset (INIT) with $\overline{\text{INIT}}$ pin immediately after start-up.

Also, in order to provide the oscillation stabilization wait time for the oscillation circuit immediately after start-up, hold the “L” level input to the $\overline{\text{INIT}}$ pin for the required stabilization wait time. (For INIT via the $\overline{\text{INIT}}$ pin, the oscillation stabilization wait time setting is initialized to the minimum value) .

About Oscillation Input at Power On

When turning the power on, maintain clock input until the device is released from the oscillation stabilization wait state.

Clock Control Block

Input the “L” signal to the $\overline{\text{INIT}}$ pin to assure the clock oscillation stabilization wait time.

Switch Shared Port Function

To switch between the use as a port and the use as a dedicated pin, use the port function register (PFR) .

Low Power Consumption Mode

To enter the standby mode, use the synchronous standby mode (set with the SYNCS bit as bit 8 in the TBCR : timebase counter control register) and be sure to use the following sequence

```
(LDI    #value_of_standby, R0) : value_of_standby is write data to STCR.
(LDI    #_STCR, R12)          : _STCR is address (481H) of STCR.
STB     R0, @R12              : Writing to standby control register (STCR)
LDUB    @R12, R0              : STCR read for synchronous standby
LDUB    @R12, R0              : Dummy re-read of STCR
NOP                                           : NOP × 5 for arrangement of timing
NOP
NOP
NOP
NOP
```

In addition, please set I flag, ILM, and ICR to diverge to the interruption handler that is the return factor after the standby returns.

- Please do not do the following when the monitor debugger is used.
- Break point setting for above instruction lines
- Step execution for above instruction lines

Power-on sequence for dual-power-supply model

- Notes on the power-on and power-off sequences
 - Power-on sequence : Vcc3B, Vcc3→Vcc→Vcc3IO, AVRH, V0 to V3
 - Power-off sequence : Vcc3IO, AVRH, V0 to V3, Vcc3→Vcc→Vcc3B, Vcc3
- When Vcc is turned on earlier, a potential difference between Vcc and Vcc3 must fall within 3.6 V.
- The LCD power supply V3 must not exceed Vcc in voltage. Apply V3 after turning on Vcc3.
- Turn on Vcc3 before applying the analog power supply AVcc or an analog signal.

Notes on the PS register

As the PS register is processed by some instructions in advance, exception handling below may cause the interrupt handling routine to break when the debugger is used or the display contents of flags in the PS register to be updated.

As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, it performs operations before and after the EIT as specified in either case.

- The following operations may be performed when the instruction immediately followed by a DIVOU/DIVOS instruction is (a) acceptance of a user interrupt, (b) single-stepped, or (c) breaks in response to a data event or emulator menu :
 - 1) The D0 and D1 flags are updated in advance.
 - 2) An EIT handling routine (user interrupt or emulator) is executed.
 - 3) Upon returning from the EIT, the DIVOU/DIVOS instruction is executed, and the D0 and D1 flags are updated to the same values as in 1).
- The following operations are performed when the ORCCR/STILM/MOVRi and PS instructions are executed to allow the interrupt.
 - 1) The PS register is updated in advance.
 - 2) An EIT handling routine (user interrupt) is executed.
 - 3) Upon returning from the EIT, the above instructions are executed, and the PS register is updated to the same value as in 1).

Watchdog Timer

The watchdog timer built in this model monitors a program that it defers a reset within a certain period of time. The watchdog timer resets the CPU if the program runs out of controls, preventing the reset defer function from being executed. Once the function of the watchdog timer is enabled, therefore, the watchdog timer keeps on operating programs until it resets the CPU.

As an exception, the watchdog timer defers a reset automatically under the condition in which the CPU stops program execution.

For those conditions to which this exception applies, see the function description of watchdog timer.

Step execution of RETI instruction

If an interrupt occurs frequently during step execution, the corresponding interrupt handling routine is executed repeatedly after step execution. This will prevent the main routine and low-interrupt-level programs from being executed.

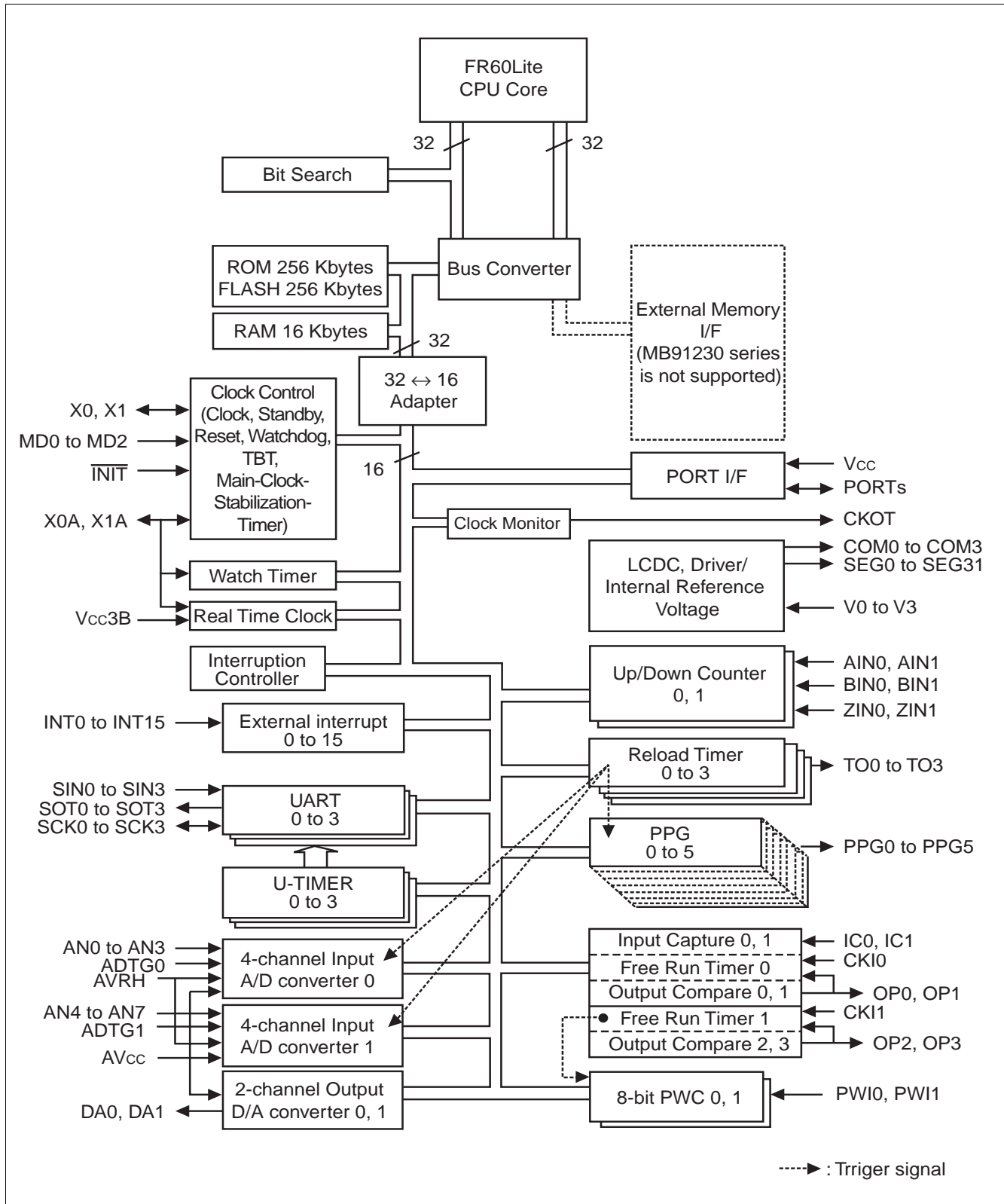
Do not execute step of RETI instruction for escape.

Disable the corresponding interrupt and execute debugger when the corresponding interrupt routine no longer needs debugging.

Operand Break

Do not apply a data event break to access to the area containing the address of a system stack pointer.

■ BLOCK DIAGRAM



MB91230 Series

■ MEMORY SPACE

1. Memory space

FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

- Direct Addressing Areas

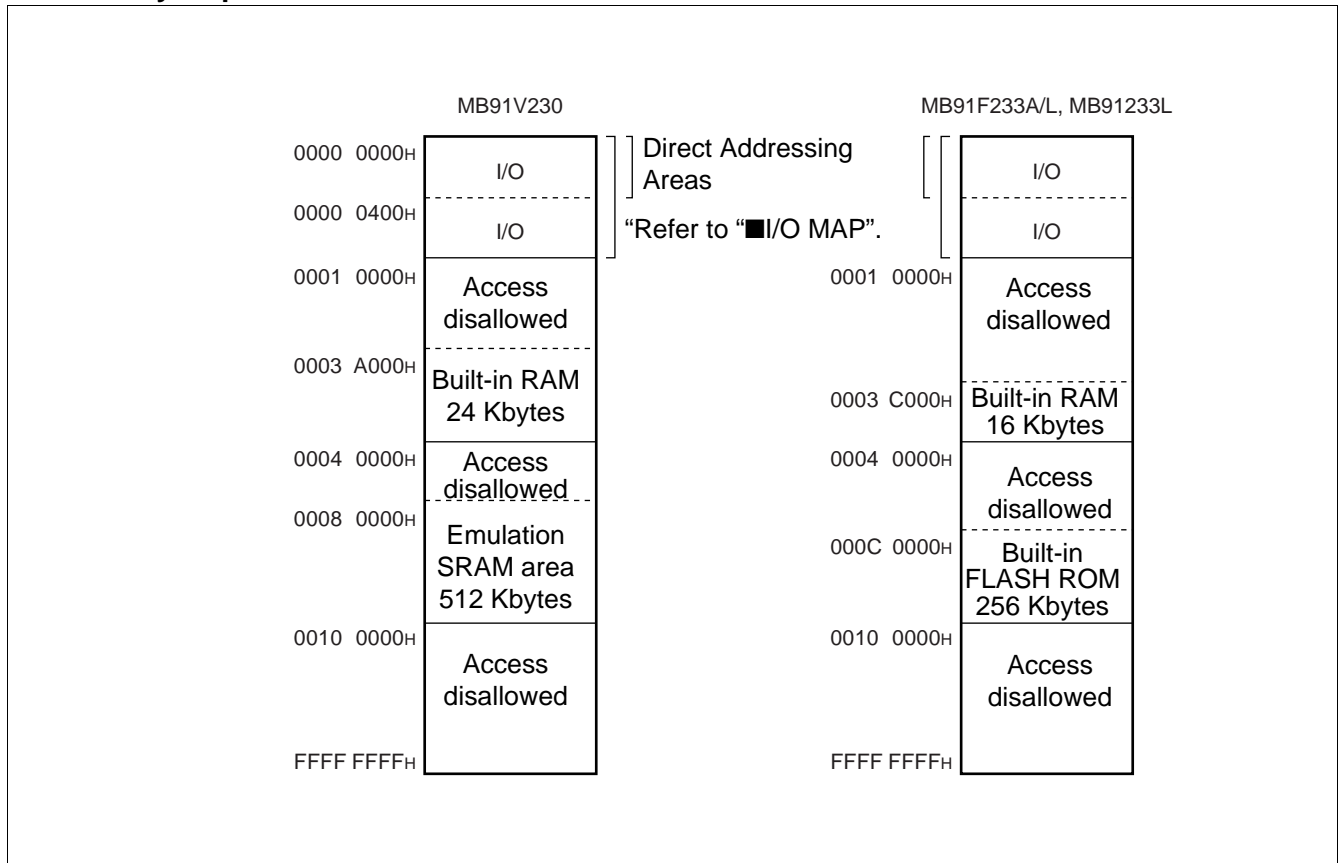
The following address space areas are used as I/O areas.

These areas are called direct addressing areas, in which the address of an operand can be specified directly during an instruction.

The size of directly addressable areas depends on the length of the data being accessed as shown below.

- byte data access : 000_H to 0FF_H
- half word data access : 000_H to 1FF_H
- word data access : 000_H to 3FF_H

2. Memory Map



Note : The external bus mode cannot be used in the MB91230 series.

MODE SETTINGS

The FR family uses mode pins (MD2 to MD0) and a mode data to set the operation mode.

- Mode Pins

The MD2 to MD0 pins specify how the mode vector fetch and reset vector fetch is performed.

Setting is prohibited other than that shown in the following table.

| Mode Pins | | | Mode name | Reset vector access area | Remarks |
|-----------|-----|-----|--------------------------|--------------------------|------------------------------|
| MD2 | MD1 | MD0 | | | |
| 0 | 0 | 0 | Internal ROM mode vector | Internal | |
| 0 | 0 | 1 | External ROM mode vector | External | Not supported by this model. |

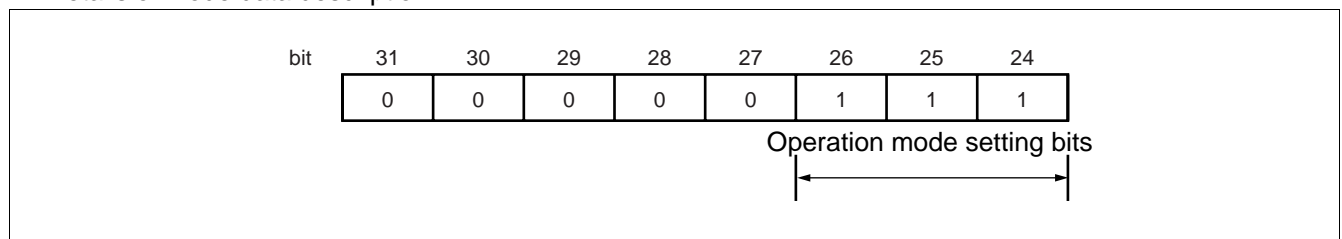
- Mode data

Data written to the internal mode register (MODR) by a mode vector fetch is called mode data.

After an operation mode has been set in the mode register, the device operates in the operation mode.

The mode data is set by all reset source. User programs cannot set data to the mode register.

Details of mode data description



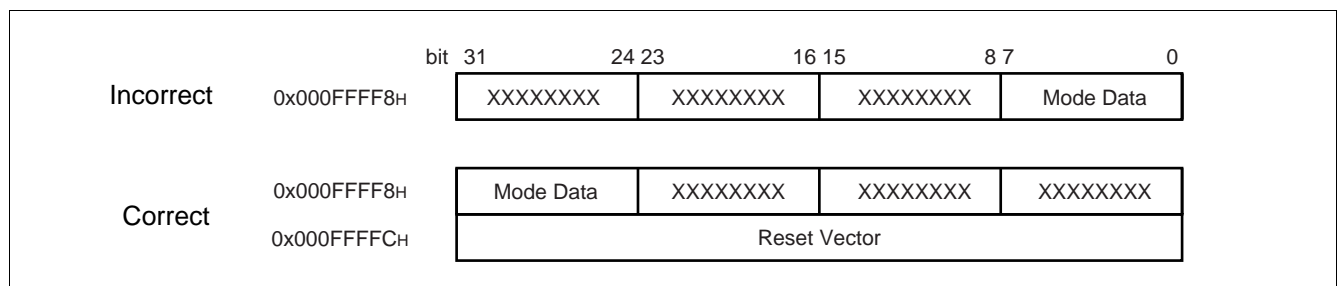
Bit31 to bit24 are all reserved bits.

Be sure to set this bit to "00000111".

Operation is not guaranteed when any value other than "00000111" is set.

Note : Mode data set in the mode vector must be placed as byte data at 0x000FFFF8H.

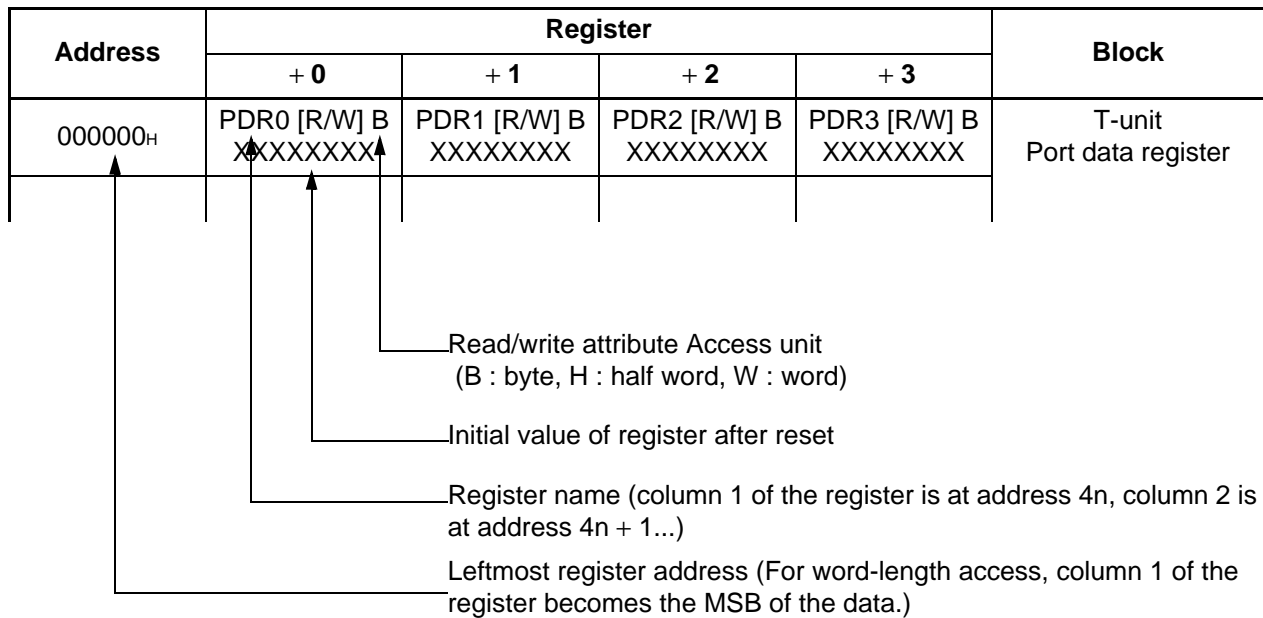
Use the highest byte from bit31 to bit24 for placement as the FR family uses the big endian for byte endian.



MB91230 Series

■ I/O MAP

[How to read the table]



Note : Initial values of register bits are represented as follows :

“ 1 ” : Initial Value “ 1 ”

“ 0 ” : Initial Value “ 0 ”

“ X ” : Initial Value “ undefined ”

“ - ” : No physical register at this location

Access is barred with an undefined data access attribute.

MB91230 Series

| Address | Register | | | | Block |
|--|---|---|--|-----------------------------------|--------------------------------------|
| | + 0 | + 1 | + 2 | + 3 | |
| 000000 _H | PDR0 [R/W] B XXXXXXXX | PDR1 [R/W] B XXXXXXXX | PDR2 [R/W] B XXXXXXXX | PDR3 [R/W] B XXXXXXXX | Port data register |
| 000004 _H | PDR4 [R/W] B XXXXXXXX | PDR5 [R/W] B XXXXXXXX | PDR6 [R/W] B XXXX---- | PDR7 [R/W] B ----XXXX | |
| 000008 _H | PDR8 [R/W] B XXXXXXXX | PDR9 [R/W] B XXXXXXXX | PDRA [R/W] B XXXXXXXX | PDRB [R/W] B ----XXXX | |
| 00000C _H | PDRC [R/W] B XXXXXXXX | PDRD [R/W] B -----XX | — | PDRF [R/W] ---XX--- | |
| 000010 _H to 00003C _H | — | — | — | — | Unused |
| 000040 _H | EIRR0 [R/W] B, H, W 00000000 | ENIR0 [R/W] B, H, W 00000000 | ELVR0 [R/W] B, H, W 00000000 00000000 | | External interrupt (INT0 to INT7) |
| 000044 _H | DICR [R/W] B, H, W -----0 | — | — | | Delay interrupt |
| 000048 _H | TMRLR0 [W] H XXXXXXXX XXXXXXXX | | TMR0 [R] H XXXXXXXX XXXXXXXX | | Reload timer 0 |
| 00004C _H | — | | TMCSR0 [R/W] H ----0000 00000000 | | |
| 000050 _H | TMRLR1 [W] H XXXXXXXX XXXXXXXX | | TMR1 [W] H XXXXXXXX XXXXXXXX | | Reload timer 1 |
| 000054 _H | — | | TMCSR1 [R/W] H ----0000 00000000 | | |
| 000058 _H | TMRLR2 [W] H XXXXXXXX XXXXXXXX | | TMR2 [W] H XXXXXXXX XXXXXXXX | | Reload timer 2 |
| 00005C _H | — | | TMCSR2 [R/W] H ----0000 00000000 | | |
| 000060 _H | SSR0 [R/W] B, H, W 00001000 | SIDR0 [R] B, H, W SODR0 [W] B, H, W XXXXXXXX | SCR0 [R/W] B, H, W 00000100 | SMR0 [R/W] B, H, W 00--0-0- | UART0 |
| 000064 _H | UTIM0 [R] H (UTIMR0 [W] H) 00000000 00000000 | | — | UTIMC0 [R/W] B 0--00001 | U-TIMER0 |
| 000068 _H | SSR1 [R/W] B, H, W 00001000 | SIDR1 [R] B, H, W SODR1 [W] B, H, W XXXXXXXX | SCR1 [R/W] B, H, W 00000100 | SMR1 [R/W] B, H, W 00--0-0- | UART1 |
| 00006C _H | UTIM1 [R] H (UTIMR1 [W] H) 00000000 00000000 | | — | UTIMC1 [R/W] B 0--00001 | U-TIMER1 |

(Continued)

MB91230 Series

| Address | Register | | | | Block |
|---------------------|--|--|--|---------------------------------------|--|
| | + 0 | + 1 | + 2 | + 3 | |
| 000070 _H | SSR2 [R/W] B, H, W 00001000 | SIDR2 [R] B, H, W SODR2 [W] B, H, W XXXXXXXXXX | SCR2 [R/W] B, H, W 00000100 | SMR2 [R/W] B, H, W 00--0-0- | UART2 |
| 000074 _H | UTIM2 [R] H (UTIMR1 [W] H) 00000000 00000000 | | — | UTIMC2 [R/W] B 0--00001 | U-TIMER2 |
| 000078 _H | ADCS0 [R/W] H, W XXXXXXXXXX XXXXXXXXXX | | ADCT0 [R/W] H, W 000-0000 -000--00 | | A/D converter 0 (series-parallel type) |
| 00007C _H | ADT00 (ADTH00/ADTL00) [R] B, H, W 000000XX XXXXXXXXXX | ADT01 (ADTH01/ADTL01) [R] B, H, W 000000XX XXXXXXXXXX | | | |
| 000080 _H | ADT02 (ADTH02/ADTL02) [R] B, H, W 000000XX XXXXXXXXXX | ADT03 (ADTH03/ADTL03) [R] B, H, W 000000XX XXXXXXXXXX | | | |
| 000084 _H | ADCS1 [R/W] H, W XXXXXXXXXX XXXXXXXXXX | | ADCT1 [R/W] H, W 000-0000 --000--00 | | A/D converter 1 (series-parallel type) |
| 000088 _H | ADT10 (ADTH10/ADTL10) [R] B, H, W 000000XX XXXXXXXXXX | ADT11 (ADTH11/ADTL11) [R] B, H, W 000000XX XXXXXXXXXX | | | |
| 00008C _H | ADT12 (ADTH12/ADTL12) [R] B, H, W 000000XX XXXXXXXXXX | ADT13 (ADTH13/ADTL13) [R] B, H, W 000000XX XXXXXXXXXX | | | |
| 000090 _H | — | — | DACR1 [R/W] B, H, W -----0 | DACR0 [R/W] B, H, W -----0 | D/A converter |
| 000094 _H | — | — | DADR1 [R/W] B, H, W XXXXXXXXXX | DADR0 [R/W] B, H, W XXXXXXXXXX | |
| 000098 _H | LCDCMR [R/W] B, H, W ----0000 | — | LCR0 [R/W] B, H, W 00010000 | LCR1 [R/W] B, H, W 00000000 | LCD controller/ driver |
| 00009C _H | VRAM0 [R/W] B, H, W XXXXXXXXXX | VRAM1 [R/W] B, H, W XXXXXXXXXX | VRAM2 [R/W] B, H, W XXXXXXXXXX | VRAM3 [R/W] B, H, W XXXXXXXXXX | |
| 0000A0 _H | VRAM4 [R/W] B, H, W XXXXXXXXXX | VRAM5 [R/W] B, H, W XXXXXXXXXX | VRAM6 [R/W] B, H, W XXXXXXXXXX | VRAM7 [R/W] B, H, W XXXXXXXXXX | |
| 0000A4 _H | VRAM8 [R/W] B, H, W XXXXXXXXXX | VRAM9 [R/W] B, H, W XXXXXXXXXX | VRAM10 [R/W] B, H, W XXXXXXXXXX | VRAM11 [R/W] B, H, W XXXXXXXXXX | |
| 0000A8 _H | VRAM12 [R/W] B, H, W XXXXXXXXXX | VRAM13 [R/W] B, H, W XXXXXXXXXX | VRAM14 [R/W] B, H, W XXXXXXXXXX | VRAM15 [R/W] B, H, W XXXXXXXXXX | |
| 0000AC _H | CKR [R/W] B, H, W ----0000 | — | — | — | Clock monitor |

(Continued)

MB91230 Series

| Address | Register | | | | Block |
|---------------------|--|--|--|------------------------------------|---------------------------------------|
| | + 0 | + 1 | + 2 | + 3 | |
| 0000B0 _H | RCR1 [W] B, H, W 00000000 | RCR0 [W] B, H, W 00000000 | UDCR1 [R] B, H, W 00000000 | UDCR0 [R] B, H, W 00000000 | Up/down counter0, 1 |
| 0000B4 _H | CCR0 [R/W] B, H, W 00000000 | CCRL0 [R/W] B, H, W 00001000 | — | CSR0 [R/W] B, H, W 00000000 | |
| 0000B8 _H | CCR1 [R/W] B, H, W 00000000 | CCRL1 [R/W] B, H, W 00001000 | — | CSR1 [R/W] B, H, W 00000000 | |
| 0000BC _H | — | — | — | — | unused |
| 0000C0 _H | SSR3 [R/W] B, H, W 00001000 | SIDR3 [R] B, H, W SODR3 [W] B, H, W XXXXXXXX | SCR3 [R/W] B, H, W 00000100 | SMR3 [R/W] B, H, W 00--0-0- | UART3 |
| 0000C4 _H | UTIM3 [R] H (UTIMR [W] H) 00000000 00000000 | | — | UTIMC3 [R/W] B 0--00001 | U-TIMER3 |
| 0000C8 _H | TMRLR3 [W] H XXXXXXXX XXXXXXXX | | TMR3 [W] H XXXXXXXX XXXXXXXX | | Reload timer 3 |
| 0000CC _H | — | | TMCSR3 [R/W] H ---00000 00000000 | | |
| 0000D0 _H | EIRR1 [R/W] B, H, W 00000000 | ENIR1 [R/W] B, H, W 00000000 | ELVR1 [R/W] B, H, W 00000000 00000000 | | External interrupt (INT8 to INT15) |
| 0000D4 _H | TCDT0 [R/W] H, W 00000000 00000000 | | — | TCCS0 [R/W] B, H, W 00000000 | Free-run timer 0 |
| 0000D8 _H | TCDT1 [R/W] H, W 00000000 00000000 | | — | TCCS1 [R/W] B, H, W 00000000 | Free-run timer 1 |
| 0000DC _H | IPCP1 [R] H, W XXXXXXXX XXXXXXXX | | IPCP0 [R] H, W XXXXXXXX XXXXXXXX | | Input capture 0, 1 |
| 0000E0 _H | — | — | — | ICS01 [R/W] B, H, W 00000000 | |
| 0000E4 _H | OCCP1 [R/W] H, W XXXXXXXX XXXXXXXX | | OCCP0 [R/W] H, W XXXXXXXX XXXXXXXX | | |
| 0000E8 _H | OCCP3 [R/W] H, W XXXXXXXX XXXXXXXX | | OCCP2 [R/W] H, W XXXXXXXX XXXXXXXX | | Output compare 0 to 3 |
| 0000EC _H | OCS23 [R/W] B, H, W ---0--00 0000--00 | | OCS01 [R/W] B, H, W ---0-00 0000--00 | | |

(Continued)

MB91230 Series

| Address | Register | | | | Block |
|--|------------------------------------|----------------------------------|--------------------------------------|----------------------------------|-----------------|
| | + 0 | + 1 | + 2 | + 3 | |
| 0000F0 _H | PWCC0 [R/W] B, H, W 0---00-0 | PWCD0 [R] B, H, W XXXXXXXX | PWCC1 [R/W] B, H, W 0---00-0 | PWCD1 [R] B, H, W XXXXXXXX | PWC0, 1 |
| 0000F4 _H | — | WTDBL [R/W] B -----0 | WTCR [R/W] B, H 00000000 000-00-X | | Real-time clock |
| 0000F8 _H | — | WTBR0 [R/W] B ---XXXX | WTBR1 [R/W] B XXXXXXXX | WTBR2 [R/W] B XXXXXXXX | |
| 0000FC _H | WTHR [R/W] B, H ---XXXX | WTMR [R/W] B, H --XXXX | WTSR [R/W] B --XXXX | — | |
| 000100 _H to 000114 _H | — | — | — | — | Unused |
| 000118 _H | GCN10 [R/W] H 00110010 00010000 | | — | GCN20 [R/W] B 00000000 | PPG |
| 00011C _H | — | | — | | Unused |
| 000120 _H | PTMR0 [R] H 11111111 11111111 | | PCSR0 [W] H XXXXXXXX XXXXXXXX | | PPG0 |
| 000124 _H | PDUT0 [W] H XXXXXXXX XXXXXXXX | | PCNH0 [R/W] B, H 00000000 | PCNL0 [R/W] B, H 00000000 | |
| 000128 _H | PTMR1 [R] H 11111111 11111111 | | PCSR1 [W] H XXXXXXXX XXXXXXXX | | PPG1 |
| 00012C _H | PDUT1 [W] H XXXXXXXX XXXXXXXX | | PCNH1 [R/W] B, H 00000000 | PCNL1 [R/W] B, H 00000000 | |
| 000130 _H | PTMR2 [R] H 11111111 11111111 | | PCSR2 [W] H XXXXXXXX XXXXXXXX | | PPG2 |
| 000134 _H | PDUT2 [W] H XXXXXXXX XXXXXXXX | | PCNH2 [R/W] B, H 00000000 | PCNL2 [R/W] B, H 00000000 | |
| 000138 _H | PTMR3 [R] H 11111111 11111111 | | PCSR3 [W] H XXXXXXXX XXXXXXXX | | PPG3 |
| 00013C _H | PDUT3 [W] H XXXXXXXX XXXXXXXX | | PCNH3 [R/W] B, H 00000000 | PCNL3 [R/W] B, H 00000000 | |
| 000140 _H | PTMR4 [R] H 11111111 11111111 | | PCSR4 [W] H XXXXXXXX XXXXXXXX | | PPG4 |
| 000144 _H | PDUT4 [W] H XXXXXXXX XXXXXXXX | | PCNH4 [R/W] B, H 00000000 | PCNL4 [R/W] B, H 00000000 | |

(Continued)

MB91230 Series

| Address | Register | | | | Block |
|--|---|--------------------------|----------------------------------|---------------------------------|----------------------------|
| | + 0 | + 1 | + 2 | + 3 | |
| 000148 _H | PTMR5 [R] H 11111111 11111111 | | PCSR5 [W] H XXXXXXXX XXXXXXXX | | PPG5 |
| 00014C _H | PDUT5 [W] H XXXXXXXX XXXXXXXX | | PCNH5 [R/W] B, H 00000000 | PCNL5 [R/W] B, H 00000000 | |
| 000150 _H to 0001FC _H | — | — | — | — | Unused |
| 000200 _H to 0003EC _H | — | — | — | — | Unused |
| 0003F0 _H | BSD0 [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | Bit search |
| 0003F4 _H | BSD1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 0003F8 _H | BSDC [W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 0003FC _H | BSRR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 000400 _H | DDR0 [R/W] B 00000000 | DDR1 [R/W] B 00000000 | DDR2 [R/W] B 00000000 | DDR3 [R/W] B00000000 | Data direction register |
| 000404 _H | DDR4 [R/W] B 00000000 | DDR5 [R/W] B 00000000 | DDR6 [R/W] B 0000---- | DDR7 [R/W] B ----0000 | |
| 000408 _H | DDR8 [R/W] B 00000000 | DDR9 [R/W] B 00000000 | DDRA [R/W] B 00000000 | DDRB [R/W] B ----0000 | |
| 00040C _H | DDRC [R/W] B 00000000 | DDRD [R/W] B -----00 | — | DDRF [R/W] B ---00--- | |
| 000410 _H to 00041C _H | — | — | — | — | Unused |
| 000420 _H | PFR0 [R/W] B --00-00- | PFR1 [R/W] B ----- | PFR2 [R/W] B -00-0000 | PFR3 [R/W] B -----00 | Port function register |
| 000424 _H | PFR4 [R/W] B 00000000 | PFR5 [R/W] B ---00--- | PFR6 [R/W] B 0000---- | PFR7 [R/W] B ----0000 | |
| 000428 _H | PFR8 [R/W] B 00000000 | PFR9 [R/W] B 00000000 | PFRA [R/W] B 00000000 | PFRB [R/W] B ----0000 | |
| 00042C _H | PFRC [R/W] B ----- | PFRD [R/W] B -----00 | — | PFRF [R/W] B ----0--- | |
| 000430 _H to 00043C _H | — | — | — | — | Unused |

(Continued)

MB91230 Series

| Address | Register | | | | Block | |
|--|------------------------------------|------------------------------------|------------------------------------|------------------------------------|----------------------|--------|
| | + 0 | + 1 | + 2 | + 3 | | |
| 000440 _H | ICR00 [R/W] B, H, W ---11111 | ICR01 [R/W] B, H, W ---11111 | ICR02 [R/W] B, H, W ---11111 | ICR03 [R/W] B, H, W ---11111 | Interrupt controller | |
| 000444 _H | ICR04 [R/W] B, H, W ---11111 | ICR05 [R/W] B, H, W ---11111 | ICR06 [R/W] B, H, W ---11111 | ICR07 [R/W] B, H, W ---11111 | | |
| 000448 _H | ICR08 [R/W] B, H, W ---11111 | ICR09 [R/W] B, H, W ---11111 | ICR10 [R/W] B, H, W ---11111 | ICR11 [R/W] B, H, W ---11111 | | |
| 00044C _H | ICR12 [R/W] B, H, W ---11111 | ICR13 [R/W] B, H, W ---11111 | ICR14 [R/W] B, H, W ---11111 | ICR15 [R/W] B, H, W ---11111 | | |
| 000450 _H | ICR16 [R/W] B, H, W ---11111 | ICR17 [R/W] B, H, W ---11111 | ICR18 [R/W] B, H, W ---11111 | ICR19 [R/W] B, H, W ---11111 | | |
| 000454 _H | ICR20 [R/W] B, H, W ---11111 | ICR21 [R/W] B, H, W ---11111 | ICR22 [R/W] B, H, W ---11111 | ICR23 [R/W] B, H, W ---11111 | | |
| 000458 _H | ICR24 [R/W] B, H, W ---11111 | ICR25 [R/W] B, H, W ---11111 | ICR26 [R/W] B, H, W ---11111 | ICR27 [R/W] B, H, W ---11111 | | |
| 00045C _H | ICR28 [R/W] B, H, W ---11111 | ICR29 [R/W] B, H, W ---11111 | ICR30 [R/W] B, H, W ---11111 | ICR31 [R/W] B, H, W ---11111 | | |
| 000460 _H | ICR32 [R/W] B, H, W ---11111 | ICR33 [R/W] B, H, W ---11111 | ICR34 [R/W] B, H, W ---11111 | ICR35 [R/W] B, H, W ---11111 | | |
| 000464 _H | ICR36 [R/W] B, H, W ---11111 | ICR37 [R/W] B, H, W ---11111 | ICR38 [R/W] B, H, W ---11111 | ICR39 [R/W] B, H, W ---11111 | | |
| 000468 _H | ICR40 [R/W] B, H, W ---11111 | ICR41 [R/W] B, H, W ---11111 | ICR42 [R/W] B, H, W ---11111 | ICR43 [R/W] B, H, W ---11111 | | |
| 00046C _H | ICR44 [R/W] B, H, W ---11111 | ICR45 [R/W] B, H, W ---11111 | ICR46 [R/W] B, H, W ---11111 | ICR47 [R/W] B, H, W ---11111 | | |
| 000470 _H to 00047C _H | — | — | — | — | | Unused |

(Continued)

MB91230 Series

(Continued)

| Address | Register | | | | Block |
|--|--------------------------------|--------------------------------|---------------------------------|---------------------------------|--|
| | + 0 | + 1 | + 2 | + 3 | |
| 000480 _H | RSRR [R/W] B, H 10000000 | STCR [R/W] B, H 00110011 | TBCR [R/W] B 00XXXX00 | CTBR [W] B XXXXXXXX | Clock control |
| 000484 _H | CLKR [R/W] B 00000000 | WPR [R/W] B XXXXXXXX | DIVR0 [R/W] B, H 00000011 | DIVR1 [R/W] B, H 00000000 | |
| 000488 _H | — | — | OSCCR [R/W] B XXXXXXXX0 | — | |
| 00048C _H | WPCR [R/W] B 00---000 | — | — | — | Watch timer |
| 000490 _H | OSCR [R/W] B 00---000 | — | — | — | Main clock oscillation stabilization wait timer |
| 000494 _H to 0004FC _H | — | — | — | — | Unused |
| 000500 _H | — | PCR1 [R/W] B 00000000 | — | PCR3 [R/W] B 00000000 | Pull-up control register |
| 000504 _H to 00051C _H | — | — | — | — | Unused |
| 000520 _H to 0007F8 _H | — | — | — | — | Unused |
| 0007FC _H | — | MODR* XXXXXXXX | — | — | Operation mode |
| 000800 _H to 000AFC _H | — | — | — | — | Unused |
| 000B00 _H to 000FFC _H | — | — | — | — | Unused |
| 001000 _H to 006FFC _H | — | — | — | — | Unused |
| 007000 _H | FLCR [R/W] B 01101000 | — | — | — | FLASH |
| 007004 _H | FLWC [R/W] B 00000011 | — | — | — | |
| 007008 _H to 00FFFC _H | — | — | — | — | Unused |

* : This register is set when the mode vector is fetched. Not user-accessible.

MB91230 Series

■ INTERRUPT VECTOR

| Interrupt source | Interrupt number | | Interrupt level | Offset | TBR default address |
|--|------------------|----|----------------------------|------------------|-----------------------|
| | 10 | 16 | | | |
| Reset | 0 | 00 | — | 3FC _H | 000FFFFC _H |
| Mode vector | 1 | 01 | — | 3F8 _H | 000FFFF8 _H |
| System reserved | 2 | 02 | — | 3F4 _H | 000FFFF4 _H |
| System reserved | 3 | 03 | — | 3F0 _H | 000FFFF0 _H |
| System reserved | 4 | 04 | — | 3EC _H | 000FFFE _C |
| System reserved | 5 | 05 | — | 3E8 _H | 000FFFE8 _H |
| System reserved | 6 | 06 | — | 3E4 _H | 000FFFE4 _H |
| Coprocessor absent trap | 7 | 07 | — | 3E0 _H | 000FFFE0 _H |
| Coprocessor error trap | 8 | 08 | — | 3DC _H | 000FFFD _C |
| INTE instruction | 9 | 09 | — | 3D8 _H | 000FFFD8 _H |
| Instruction break exception | 10 | 0A | — | 3D4 _H | 000FFFD4 _H |
| Operand break trap | 11 | 0B | — | 3C0 _H | 000FFFD0 _H |
| Step trace trap | 12 | 0C | — | 3CC _H | 000FFFC _C |
| NMI request (tool) | 13 | 0D | — | 3C8 _H | 000FFFC8 _H |
| Undefined instruction exception | 14 | 0E | — | 3C4 _H | 000FFFC4 _H |
| NMI request (This model has no NMI request) | 15 | 0F | 15 (F _H) fixed | 3C0 _H | 000FFFC0 _H |
| External interrupt 0 | 16 | 10 | ICR00 | 3BC _H | 000FFFB _C |
| External interrupt 1 | 17 | 11 | ICR01 | 3B8 _H | 000FFFB8 _H |
| External interrupt 2 | 18 | 12 | ICR02 | 3B4 _H | 000FFFB4 _H |
| External interrupt 3 | 19 | 13 | ICR03 | 3B0 _H | 000FFFB0 _H |
| External interrupt 4 | 20 | 14 | ICR04 | 3AC _H | 000FFFA _C |
| External interrupt 5 | 21 | 15 | ICR05 | 3A8 _H | 000FFFA8 _H |
| External interrupt 6 | 22 | 16 | ICR06 | 3A4 _H | 000FFFA4 _H |
| External interrupt 7 | 23 | 17 | ICR07 | 3A0 _H | 000FFFA0 _H |
| Reload timer 0 | 24 | 18 | ICR08 | 39C _H | 000FFF9 _C |
| Reload timer 1 | 25 | 19 | ICR09 | 398 _H | 000FFF98 _H |
| Reload timer 2 | 26 | 1A | ICR10 | 394 _H | 000FFF94 _H |
| UART0(Reception completed) | 27 | 1B | ICR11 | 390 _H | 000FFF90 _H |
| UART0 (Transmission completed) | 28 | 1C | ICR12 | 38C _H | 000FFF8 _C |
| UART1 (Reception completed) | 29 | 1D | ICR13 | 388 _H | 000FFF88 _H |
| UART1 (Transmission completed) | 30 | 1E | ICR14 | 384 _H | 000FFF84 _H |
| UART2 (Reception completed) | 31 | 1F | ICR15 | 380 _H | 000FFF80 _H |
| UART2 (Transmission completed) | 32 | 20 | ICR16 | 37C _H | 000FFF7 _C |

(Continued)

MB91230 Series

| Interrupt source | Interrupt number | | Interrupt level | Offset | TBR default address |
|---|------------------|----|-----------------|------------------|-----------------------|
| | 10 | 16 | | | |
| UART3 (Reception completed) | 33 | 21 | ICR17 | 378 _H | 000FFF78 _H |
| UART3 (Transmission completed) | 34 | 22 | ICR18 | 374 _H | 000FFF74 _H |
| A/D ch0 | 35 | 23 | ICR19 | 370 _H | 000FFF70 _H |
| A/D ch1 | 36 | 24 | ICR20 | 36C _H | 000FFF6C _H |
| External interrupt8 | 37 | 25 | ICR21 | 368 _H | 000FFF68 _H |
| External interrupt9 | 38 | 26 | ICR22 | 364 _H | 000FFF64 _H |
| External interrupt 10 | 39 | 27 | ICR23 | 360 _H | 000FFF60 _H |
| External interrupt 11 | 40 | 28 | ICR24 | 35C _H | 000FFF5C _H |
| External interrupt 12 | 41 | 29 | ICR25 | 358 _H | 000FFF58 _H |
| External interrupt 13 | 42 | 2A | ICR26 | 354 _H | 000FFF54 _H |
| External interrupt 14 | 43 | 2B | ICR27 | 350 _H | 000FFF50 _H |
| External interrupt 15 | 44 | 2C | ICR28 | 34C _H | 000FFF4C _H |
| Real-time clock | 45 | 2D | ICR29 | 348 _H | 000FFF48 _H |
| Main clock oscillation stabilization wait timer | 46 | 2E | ICR30 | 344 _H | 000FFF44 _H |
| Timebase timer | 47 | 2F | ICR31 | 340 _H | 000FFF40 _H |
| Reload timer 3 | 48 | 30 | ICR32 | 33C _H | 000FFF3C _H |
| Watch timer | 49 | 31 | ICR33 | 338 _H | 000FFF38 _H |
| UD Counter 0 | 50 | 32 | ICR34 | 334 _H | 000FFF34 _H |
| UD Counter 1 | 51 | 33 | ICR35 | 330 _H | 000FFF30 _H |
| PPG 0/1 | 52 | 34 | ICR36 | 32C _H | 000FFF2C _H |
| PPG 2/3 | 53 | 35 | ICR37 | 328 _H | 000FFF28 _H |
| PPG 4/5 | 54 | 36 | ICR38 | 324 _H | 000FFF24 _H |
| Free-run timer 0 | 55 | 37 | ICR39 | 320 _H | 000FFF20 _H |
| Free-run timer 1 | 56 | 38 | ICR40 | 31C _H | 000FFF1C _H |
| ICU 0 (capture) | 57 | 39 | ICR41 | 318 _H | 000FFF18 _H |
| ICU 1 (capture) | 58 | 3A | ICR42 | 314 _H | 000FFF14 _H |
| OCU 0 (match) | 59 | 3B | ICR43 | 310 _H | 000FFF10 _H |
| OCU 1 (match) | 60 | 3C | ICR44 | 30C _H | 000FFF0C _H |
| OCU 2 (match) | 61 | 3D | ICR45 | 308 _H | 000FFF08 _H |
| OCU 3 (match) | 62 | 3E | ICR46 | 304 _H | 000FFF04 _H |
| Delay interrupt source bit | 63 | 3F | ICR47 | 300 _H | 000FFF00 _H |
| System reserved (Used by REALOS) | 64 | 40 | — | 2FC _H | 000FFEFC _H |
| System reserved (Used by REALOS) | 65 | 41 | — | 2F8 _H | 000FFE8 _H |
| System reserved | 66 | 42 | — | 2F4 _H | 000FEF4 _H |

(Continued)

MB91230 Series

(Continued)

| Interrupt source | Interrupt number | | Interrupt level | Offset | TBR default address |
|-------------------------|------------------|----------------|-----------------|--|--|
| | 10 | 16 | | | |
| System reserved | 67 | 43 | — | 2F0 _H | 000FFE0 _H |
| System reserved | 68 | 44 | — | 2EC _H | 000FEEC _H |
| System reserved | 69 | 45 | — | 2E8 _H | 000FEE8 _H |
| System reserved | 70 | 46 | — | 2E4 _H | 000FEE4 _H |
| System reserved | 71 | 47 | — | 2E0 _H | 000FEE0 _H |
| System reserved | 72 | 48 | — | 2DC _H | 000FEDC _H |
| System reserved | 73 | 49 | — | 2D8 _H | 000FED8 _H |
| System reserved | 74 | 4A | — | 2D4 _H | 000FED4 _H |
| System reserved | 75 | 4B | — | 2D0 _H | 000FED0 _H |
| System reserved | 76 | 4C | — | 2CC _H | 000FECC _H |
| System reserved | 77 | 4D | — | 2C8 _H | 000FEC8 _H |
| System reserved | 78 | 4E | — | 2C4 _H | 000FEC4 _H |
| System reserved | 79 | 4F | — | 2C0 _H | 000FEC0 _H |
| Used by INT instruction | 80 to 255 | 50 to FF | — | 2BC _H to 000 _H | 000FEBC _H to 000FC00 _H |

■ PIN STATUS IN EACH CPU STATE

Terms used as the status of pins mean as follows.

- Input enabled
Indicates that the input function can be used.
- Input 0 fixed
Indicates that the input level has been internally fixed to be “0” to prevent leakage when the input is released.
- Output Hi-Z
Means the placing of a pin in a high impedance state by preventing the transistor for driving the pin from driving.
- Output is maintained
Indicates the output in the output state existing immediately before this mode is established. If the device enters this mode with an internal output peripheral operating or while serving as an output port, the output is performed by the internal peripheral or the port output is maintained, respectively.
- State existing immediately before is maintained
When the device serves for output or input immediately before entering this mode, the device maintains the output or is ready for the input, respectively.

MB91230 Series

• Pin Status List

| Pin no. | Pin name | Port name | Specified function name | | | At initializing | | At sleep mode | At Stop mode | | Remarks |
|---------|--------------|-----------|-------------------------|----------|--------------|-----------------|-------------------------------------|---|---|-------------------------------------|--|
| | | | Input | Output | Input/Output | Function name | Reset initialization | | HIZ = 0 | HIZ = 1 | |
| 1 | P26/ SCK2 | P26 | — | — | SCK2 | P26 | Output Hi-Z/ Input enabled | Retention of the immediately prior state | Retention of the immediately prior state | Output Hi-Z/ Input 0 fixed | |
| 2 | P27/ SIN3 | P27 | SIN3 | — | — | P27 | | | | | |
| 3 | P30/ SOT3 | P30 | — | SOT3 | — | P30 | | | | | Pull-up options can be selected |
| 4 | P31/ SCK3 | P31 | — | — | SCK3 | P31 | | | | | Pull-up options can be selected |
| 5 | P32/ AIN0 | P32 | AIN0 | — | — | P32 | | | | | Pull-up options can be selected |
| 6 | P33/ BIN0 | P33 | BIN0 | — | — | P33 | | | | | Pull-up options can be selected |
| 7 | P34/ ZIN0 | P34 | ZIN0 | — | — | P34 | | | | | Pull-up options can be selected |
| 8 | P35/ AIN1 | P35 | AIN1 | — | — | P35 | | | | | Pull-up options can be selected |
| 9 | P36/ BIN1 | P36 | BIN1 | — | — | P36 | | | | | Pull-up options can be selected |
| 10 | P37/ ZIN1 | P37 | ZIN1 | — | — | P37 | | | | | Pull-up options can be selected |
| 11 | P40/ PPG0 | P40 | — | PPG 0 | — | P40 | | | | | |
| 12 | P41/ PPG1 | P41 | — | PPG 1 | — | P41 | | | | | |

(Continued)

MB91230 Series

| Pin no. | Pin name | Port name | Specified function name | | | At initializing | | At sleep mode | At Stop mode | | Remarks | |
|---------|------------------------|-----------|-------------------------|--------|--------------|-----------------|-------------------------------------|---|---|---|--|--|
| | | | Input | Output | Input/Output | Function name | Reset initialization | | HIZ = 0 | HIZ = 1 | | |
| 13 | X0A | — | — | — | — | — | — | — | — | | | |
| 14 | X1A | — | — | — | — | — | — | — | — | | | |
| 15 | V _{cc3B} | — | — | — | — | — | — | — | — | | | |
| 16 | V _{ss} | — | — | — | — | — | — | — | — | | | |
| 17 | V _{cc3} | — | — | — | — | — | — | — | — | | | |
| 18 | P42/ PPG2 | P42 | — | PPG2 | — | P42 | Output Hi-Z/ Input enabled | Retention of the immediately prior state | Retention of the immediately prior state | Output Hi-Z/ Input 0 fixed | | |
| 19 | P43/ PPG3 | P43 | — | PPG3 | — | P43 | | | | | | |
| 20 | P44/ TOT0 | P44 | — | TOT0 | — | P44 | | | | | | |
| 21 | P45/ TOT1 | P45 | — | TOT1 | — | P45 | | | | | | |
| 22 | P46/ TOT2 | P46 | — | TOT2 | — | P46 | | | | | | |
| 23 | P47/ CKOT | P47 | — | CKOT | — | P47 | | | | | | |
| 24 | P50/ INT8 | P50 | INT8 | — | — | P50 | | | Retention of the immediately prior state | P : Retention of the immediately prior state F : Input enabled | P : Output Hi-Z F : Input enabled | |
| 25 | P51/ INT9 | P51 | INT9 | — | — | P51 | | | | | | |
| 26 | P52/ INT10 | P52 | INT10 | — | — | P52 | | | | | | |
| 27 | P53/ INT11/ PPG4 | P53 | INT11 | PPG4 | — | P53 | | | | | | |
| 28 | P54/ INT12/ PPG5 | P54 | INT12 | PPG5 | — | P54 | | | | | | |
| 29 | P55/ INT13/ TIN2 | P55 | INT13 TIN2 | — | — | P55 | | | | | | |
| 30 | P56/ INT14/ TIN1 | P56 | INT14 TIN1 | — | — | P56 | | | | | | |

Note : P : Port selected, F : Specified function selected

(Continued)

MB91230 Series

| Pin no. | Pin name | Port name | Specified function name | | | At initializing | | At sleep mode | At Stop mode | | Re- marks | |
|---------|----------------------------------|-----------|-------------------------|--------|------------------|-----------------|-------------------------------------|---|--|---|--------------|-------------------------------------|
| | | | Input | Output | Input/ Output | Function name | Reset initialization | | HIZ = 0 | HIZ = 1 | | |
| 31 | P57/ INT15/ TIN0/ ADTG0 | P57 | INT15 TIN0 ADTG0 | — | — | P57 | Output Hi-Z/ Input enabled | Retention of the immediately prior state | P : Retention of the immediately prior state | P : Output Hi-Z | | |
| 32 | PF3/ TOT3 | PF3 | — | TOT3 | — | PF3 | | | Retention of the immediately prior state | F : Input enabled | | F : Input 0 enabled |
| 33 | PF4/ TIN3/ ADTG1 | PF4 | TIN3 ADTG1 | — | — | PF4 | | | | Retention of the immediately prior state | | Output Hi-Z/ Input 0 fixed |
| 34 | PD0/ DA0 | PD0 | — | DA0 | — | PD0 | | | | | | |
| 35 | PD1/ DA1 | PD1 | — | DA1 | — | PD1 | | | | | | |
| 36 | AV _{cc} | — | — | — | — | — | — | — | — | | | |
| 37 | AVRH | — | — | — | — | — | — | — | — | | | |
| 38 | AV _{ss} | — | — | — | — | — | — | — | — | | | |
| 39 | PC0/ AN0 | PC0 | AN0 | — | — | PC0 | Output Hi-Z/ Input enabled | Retention of the immediately prior state | Retention of the immediately prior state | Output Hi-Z/ Input 0 fixed | | |
| 40 | PC1/ AN1 | PC1 | AN1 | — | — | PC1 | | | | | | |
| 41 | PC2/ AN2 | PC2 | AN2 | — | — | PC2 | Output Hi-Z/ Input enabled | Retention of the immediately prior state | Retention of the immediately prior state | Output Hi-Z/ Input 0 fixed | | |
| 42 | PC3/ AN3 | PC3 | AN3 | — | — | PC3 | | | | | | |
| 43 | PC4/ AN4 | PC4 | AN4 | — | — | PC4 | | | | | | |
| 44 | PC5/ AN5 | PC5 | AN5 | — | — | PC5 | | | | | | |
| 45 | PC6/ AN6 | PC6 | AN6 | — | — | PC6 | | | | | | |
| 46 | PC7/ AN7 | PC7 | AN7 | — | — | PC7 | | | | | | |

Note : P : Port selected, F : Specified function selected

(Continued)

MB91230 Series

| Pin no. | Pin name | Port name | Specified function name | | | At initializing | | At sleep mode | At Stop mode | | Re-remarks |
|---------|--------------------|-----------|-------------------------|--------|--------------|-----------------|-------------------------------------|---|---|--|------------|
| | | | Input | Output | Input/Output | Function name | Reset initialization | | HIZ = 0 | HIZ = 1 | |
| 47 | V _{SS} | — | — | — | — | — | — | — | — | | |
| 48 | V _{CC3IO} | — | — | — | — | — | — | — | — | | |
| 49 | P80/ SEG0 | P80 | — | SEG0 | — | P80 | Output Hi-Z/ Input enabled | Retention of the immediately prior state | Retention of the immediately prior state | P : Output Hi-Z/ Input 0 fixed F : Retention of the immediately prior state | |
| 50 | P81/ SEG1 | P81 | — | SEG1 | — | P81 | | | | | |
| 51 | P82/ SEG2 | P82 | — | SEG2 | — | P82 | | | | | |
| 52 | P83/ SEG3 | P83 | — | SEG3 | — | P83 | | | | | |
| 53 | P84/ SEG4 | P84 | — | SEG4 | — | P84 | | | | | |
| 54 | P85/ SEG5 | P85 | — | SEG5 | — | P85 | | | | | |
| 55 | P86/ SEG6 | P86 | — | SEG6 | — | P86 | | | | | |
| 56 | P87/ SEG7 | P87 | — | SEG7 | — | P87 | | | | | |
| 57 | P90/ SEG8 | P90 | — | SEG8 | — | P90 | | | | | |
| 58 | P91/ SEG9 | P91 | — | SEG9 | — | P91 | | | | | |
| 59 | P92/ SEG10 | P92 | — | SEG10 | — | P92 | | | | | |
| 60 | P93/ SEG11 | P93 | — | SEG11 | — | P93 | | | | | |
| 61 | P94/ SEG12 | P94 | — | SEG12 | — | P94 | | | | | |
| 62 | P95/ SEG13 | P95 | — | SEG13 | — | P95 | | | | | |
| 63 | P96/ SEG14 | P96 | — | SEG14 | — | P96 | | | | | |

Note : P : Port selected, F : Specified function selected

(Continued)

MB91230 Series

| Pin no. | Pin name | Port name | Specified function name | | | At initializing | | At sleep mode | At Stop mode | | Re- marks |
|---------|-----------------|-----------|-------------------------|--------|------------------|-----------------|-------------------------------------|---|---|--|--------------|
| | | | Input | Output | Input/ Output | Function name | Reset initialization | | HIZ = 0 | HIZ = 1 | |
| 64 | P97/ SEG15 | P97 | — | SEG15 | — | P97 | Output Hi-Z/ Input enabled | Retention of the immediately prior state | Retention of the immediately prior state | P : Output Hi-Z/ Input 0 fixed F : Retention of the immediately prior state | |
| 65 | PA0/ SEG16 | PA0 | — | SEG16 | — | PA0 | | | | | |
| 66 | PA1/ SEG17 | PA1 | — | SEG17 | — | PA1 | | | | | |
| 67 | PA2/ SEG18 | PA2 | — | SEG18 | — | PA2 | | | | | |
| 68 | PA3/ SEG19 | PA3 | — | SEG19 | — | PA3 | | | | | |
| 69 | PA4/ SEG20 | PA4 | — | SEG20 | — | PA4 | | | | | |
| 70 | PA5/ SEG21 | PA5 | — | SEG21 | — | PA5 | | | | | |
| 71 | PA6/ SEG22 | PA6 | — | SEG22 | — | PA6 | | | | | |
| 72 | PA7/ SEG23 | PA7 | — | SEG23 | — | PA7 | | | | | |
| 73 | PB0/ SEG24 | PB0 | — | SEG24 | — | PB0 | | | | | |
| 74 | PB1/ SEG25 | PB1 | — | SEG25 | — | PB1 | | | | | |
| 75 | V _{CC} | — | — | — | — | — | — | — | — | | |
| 76 | V _{SS} | — | — | — | — | — | — | — | — | | |
| 77 | PB2/ SEG26 | PB2 | — | SEG26 | — | PB2 | Output Hi-Z/ Input enabled | Retention of the immediately prior state | Retention of the immediately prior state | P : Output Hi-Z/ Input 0 fixed F : Retention of the immediately prior state | |
| 78 | PB3/ SEG27 | PB3 | — | SEG27 | — | PB3 | | | | | |
| 79 | P64/ SEG28 | P64 | — | SEG28 | — | P64 | | | | | |

Note : P : Port selected, F : Specified function selected

(Continued)

MB91230 Series

| Pin no. | Pin name | Port name | Specified function name | | | At initializing | | At sleep mode | At Stop mode | | Re- marks |
|---------|---------------|-----------|-------------------------|--------|------------------|-----------------|-------------------------------------|---|---|---|--|
| | | | Input | Output | Input/ Output | Function name | Reset initialization | | HIZ = 0 | HIZ = 1 | |
| 80 | P65/ SEG29 | P65 | — | SEG29 | — | P65 | Output Hi-Z/ Input enabled | Retention of the immediately prior state | Retention of the immediately prior state | P : Output Hi-Z/ Input 0 fixed F : Retention of the immediately prior state | open- drain pin, I _{OL} = 20 mA |
| 81 | P66/ SEG30 | P66 | — | SEG30 | — | P66 | | | | | open- drain pin, I _{OL} = 20 mA |
| 82 | P67/ SEG31 | P67 | — | SEG31 | — | P67 | | | | | open- drain pin, I _{OL} = 20 mA |
| 83 | P70/ COM0 | P70 | — | COM0 | — | P70 | | | | | |
| 84 | P71/ COM1 | P71 | — | COM1 | — | P71 | | | | | |
| 85 | P72/ COM2 | P72 | — | COM2 | — | P72 | | | | | |
| 86 | P73/ COM3 | P73 | — | COM3 | — | P73 | | | | | |
| 87 | MD2 | — | — | — | — | — | — | — | — | — | |
| 88 | MD1 | — | — | — | — | — | — | — | — | — | |
| 89 | MD0 | — | — | — | — | — | — | — | — | — | |
| 90 | INIT | — | — | — | — | — | — | — | — | — | |
| 91 | V0 | — | — | — | — | — | — | — | — | — | |
| 92 | V1 | — | — | — | — | — | — | — | — | — | |
| 93 | V2 | — | — | — | — | — | — | — | — | — | |
| 94 | V3 | — | — | — | — | — | — | — | — | — | |

Note : P : Port selected, F : Specified function selected

(Continued)

MB91230 Series

| Pin no. | Pin name | Port name | Specified function name | | | At initializing | | At sleep mode | At Stop mode | | Remarks |
|---------|-----------------|-----------|-------------------------|--------|--------------|-----------------|-------------------------------------|---|---|-------------------------------------|---------|
| | | | Input | Output | Input/Output | Function name | Reset initialization | | HIZ = 0 | HIZ = 1 | |
| 95 | P00/ SIN0 | P00 | SIN0 | — | — | P00 | Output Hi-Z/ Input enabled | Retention of the immediately prior state | Retention of the immediately prior state | Output Hi-Z/ Input 0 fixed | |
| 96 | P01/ SOT0 | P01 | — | SOT0 | — | P01 | | | | | |
| 97 | P02/ SCK0 | P02 | — | — | SCK0 | P02 | | | | | |
| 98 | P03/ SIN1 | P03 | SIN1 | — | — | P03 | | | | | |
| 99 | P04/ SOT1 | P04 | — | SOT1 | — | P04 | | | | | |
| 100 | P05/ SCK1 | P05 | — | — | SCK1 | P05 | | | | | |
| 101 | P06/ IC0 | P06 | IC0 | — | — | P06 | | | | | |
| 102 | P07/ IC1 | P07 | IC1 | — | — | P07 | | | | | |
| 103 | P10/ INT0 | P10 | INT0 | — | — | P10 | | | | | |
| 104 | P11/ INT1 | P11 | INT1 | — | — | P11 | | | | | |
| 105 | V _{CC} | — | — | — | — | — | — | — | — | | |
| 106 | V _{SS} | — | — | — | — | — | — | — | — | | |
| 107 | X1 | — | — | — | — | — | — | — | — | | |
| 108 | X0 | — | — | — | — | — | — | — | — | | |

Note : P : Port selected, F : Specified function selected

(Continued)

(Continued)

| Pin no. | Pin name | Port name | Specified function name | | | At initializing | | At sleep mode | At Stop mode | | Remarks |
|---------|----------------------|-----------|-------------------------|--------|--------------|-----------------|-------------------------------------|---|---|--|--|
| | | | Input | Output | Input/Output | Function name | Reset initialization | | HIZ = 0 | HIZ = 1 | |
| 109 | P12/ INT2 | P12 | INT2 | — | — | P12 | Output Hi-Z/ Input enabled | Retention of the immediately prior state | P : Retention of the immediately prior state F : Input enabled | P : Output Hi-Z F : Input enabled | Pull-up options can be selected |
| 110 | P13/ INT3 | P13 | INT3 | — | — | P13 | | | | | Pull-up options can be selected |
| 111 | P14/ INT4 | P14 | INT4 | — | — | P14 | | | | | Pull-up options can be selected |
| 112 | P15/ INT5 | P15 | INT5 | — | — | P15 | | | | | Pull-up options can be selected |
| 113 | P16/ INT6 | P16 | INT6 | — | — | P16 | | | | | Pull-up options can be selected |
| 114 | P17/ INT7 | P17 | INT7 | — | — | P17 | | | | | Pull-up options can be selected |
| 115 | P20/ CKI0/ OP0 | P20 | CKI0 | OP0 | — | P20 | | | Retention of the immediately prior state | Output Hi-Z/ Input 0 fixed | |
| 116 | P21/ CKI1/ OP1 | P21 | CKI1 | OP1 | — | P21 | | | | | |
| 117 | P22/ PWI0/ OP2 | P22 | PWI0 | OP2 | — | P22 | | | | | |
| 118 | P23/ PWI1/ OP3 | P23 | PWI1 | OP3 | — | P23 | | | | | |
| 119 | P24/ SIN2 | P24 | SIN2 | — | — | P24 | | | | | |
| 120 | P25/ SOT2 | P25 | — | SOT2 | — | P25 | | | | | |

Note : P : Port selected, F : Specified function selected

MB91230 Series

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

MB91V230, MB91F233A

| Parameter | Symbol | Rating | | Unit | Remarks |
|-------------------------------|-------------|--------------|-----------------|------|---------|
| | | Min | Max | | |
| Power supply voltage* | V_{CC} | $V_{SS}-0.5$ | $V_{SS} + 6.0$ | V | |
| | V_{CC3} | $V_{SS}-0.5$ | $V_{SS} + 4.0$ | V | |
| | V_{CC3IO} | $V_{SS}-0.5$ | $V_{SS} + 4.0$ | V | |
| Analog power supply voltage* | AV_{CC} | $V_{SS}-0.5$ | $V_{SS} + 4.0$ | V | |
| Input voltage* | V_I | $V_{SS}-0.5$ | $V_{CC} + 0.5$ | V | |
| Input voltage* (open-drain) | V_{IND} | $V_{SS}-0.5$ | $V_{CC} + 0.5$ | V | |
| Analog pin input voltage* | V_{IA} | $V_{SS}-0.5$ | $AV_{CC} + 0.5$ | V | |
| Output voltage* | V_O | $V_{SS}-0.5$ | $V_{CC} + 0.5$ | V | |
| Operating ambient temperature | T_a | -40 | + 85 | °C | |
| Storage temperature | T_{stg} | -55 | + 125 | °C | |

* : This parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

MB91F233L, MB91233L

| Parameter | Symbol | Rating | | Unit | Remarks |
|-------------------------------|-------------|--------------|-----------------|------|---------|
| | | Min | Max | | |
| Power supply voltage* | V_{CC} | $V_{SS}-0.5$ | $V_{SS} + 4.0$ | V | |
| | V_{CC3} | $V_{SS}-0.5$ | $V_{SS} + 4.0$ | V | |
| | V_{CC3IO} | $V_{SS}-0.5$ | $V_{SS} + 4.0$ | V | |
| Analog power supply voltage* | AV_{CC} | $V_{SS}-0.5$ | $V_{SS} + 4.0$ | V | |
| Input voltage* | V_I | $V_{SS}-0.5$ | $V_{CC} + 0.5$ | V | |
| Input voltage* (open-drain) | V_{IND} | $V_{SS}-0.5$ | $V_{CC} + 0.5$ | V | |
| Analog pin input voltage* | V_{IA} | $V_{SS}-0.5$ | $AV_{CC} + 0.5$ | V | |
| Output voltage* | V_O | $V_{SS}-0.5$ | $V_{CC} + 0.5$ | V | |
| Operating ambient temperature | T_a | -40 | + 85 | °C | |
| Storage temperature | T_{stg} | -55 | + 125 | °C | |

* : This parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

MB91V230, MB91F233A

($V_{SS} = AV_{SS} = 0.0\text{ V}$)

| Parameter | Symbol | Value | | Unit | Remarks |
|-------------------------------|--------------------|-------|------|------|---------|
| | | Min | Max | | |
| Operating ambient temperature | Ta | -40 | + 85 | °C | |
| Power supply voltage | V _{CC} | 4.00 | 5.25 | V | *1 |
| | V _{CC3} | 3.00 | 3.60 | V | *4 |
| | V _{CC3B} | 3.00 | 3.60 | V | |
| | | 2.20 | 3.60 | V | *2 |
| | V _{CC3IO} | 3.00 | 3.60 | V | |
| Analog power supply voltage | AV _{CC} | 3.00 | 3.60 | V | |
| LCD reference voltage | V3 | — | 5.25 | V | *3 |

MB91F233L, MB91233L

($V_{SS} = AV_{SS} = 0.0\text{ V}$)

| Parameter | Symbol | Value | | Unit | Remarks |
|-------------------------------|--------------------|-------|------|------|---------|
| | | Min | Max | | |
| Operating ambient temperature | Ta | -40 | + 85 | °C | |
| Power supply voltage | V _{CC} | 3.00 | 3.60 | V | *1 |
| | V _{CC3} | 3.00 | 3.60 | V | *4 |
| | V _{CC3B} | 3.00 | 3.60 | V | |
| | | 2.20 | 3.60 | V | *2 |
| | V _{CC3IO} | 3.00 | 3.60 | V | |
| Analog power supply voltage | AV _{CC} | 3.00 | 3.60 | V | |
| LCD reference voltage | V3 | — | 3.60 | V | *3 |

*1 : The standard power-supply voltage varies with the model of product.

*2 : Only for backup. Set $V_{CC3} = AV_{CC} = V_{CC3IO}$.

*3 : V3 must not exceed V_{CC}.

*4 : For the relationships between V_{CC3} and operating frequencies, see section “4. AC Characteristics (3) Operation Assurance Range”.

For the MB91V230, please inquire separately.

Note : For normal use, set $V_{CC3} = V_{CC3B} = AV_{CC} = V_{CC3IO}$.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

MB91230 Series

3. DC Characteristics

MB91V230, MB91F233A

($V_{CC} = 4.0\text{ V to }5.25\text{ V}$, $V_{CC3} = V_{CC3B} = V_{CC3IO} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|-----------------------------------|--------------------|------------------|---|-------------------------|-----|-----------------------|------|--|
| | | | | Min | Typ | Max | | |
| Power supply current | I _{CC} | V _{CC3} | FLASH model normal operation, T _a = +25 °C, F _{CP} = 33 MHz, F _{CPP} = 16.5 MHz | — | 65 | 75 | mA | |
| | | | FLASH model normal operation, T _a = +25 °C, F _{CP} = 33 MHz, F _{CPP} = 33 MHz | — | 73 | 83 | mA | |
| | I _{CC(T)} | | RTC mode, T _a = +25 °C, F _{CP} = 32 kHz | — | 20 | 50 | μA | Watch timer, RTC, LCDC V _{CC3} = V _{CC3B} = 2.4 V |
| | I _{CC(H)} | | STOP mode, T _a = +25 °C, F _{CP} = 0 kHz | — | 5 | 50 | μA | |
| | I _{CC(S)} | | SLEEP mode F _{CP} = 33 MHz, F _{CPP} = 16.5 MHz | — | 21 | 25 | mA | |
| | | | SLEEP mode F _{CP} = 33 MHz, F _{CPP} = 33 MHz | — | 30 | 35 | mA | |
| "H" level input voltage | V _{IH} | — | — | V _{CC} × 0.8 | — | V _{CC} | V | |
| | | X0A | V _{CC3B} = 2.2 V to 3.6 V | V _{CC3B} × 0.8 | — | V _{CC3B} | V | When external clock is used |
| "L" level input voltage | V _{IL} | — | — | V _{SS} | — | V _{CC} × 0.2 | V | |
| | | X0A | V _{CC3B} = 2.2 V to 3.6 V | V _{SS} | — | V _{SS} + 0.4 | V | When external clock is used |
| "H" level output voltage | V _{OH} | — | I _{OH} = -4 mA | V _{CC} - 0.5 | — | V _{CC} | V | |
| "L" level output voltage | V _{OL} | — | I _{OL} = 4 mA | V _{SS} | — | 0.4 | V | |
| | | P64 to P67 | I _{OL} = 20 mA | | | | | |
| Input leakage current | I _{IL} | — | — | -5 | — | 5 | μA | |
| Open-drain output leakage current | I _{leak} | — | — | -10 | — | 10 | μA | |

(Continued)

MB91230 Series

(Continued)

($V_{CC} = 4.0 \text{ V to } 5.25 \text{ V}$, $V_{CC3} = V_{CC3B} = V_{CC3IO} = AV_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_a = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|----------------------------------|------------|--|------------------|-------|-----|-----|---------------|---------|
| | | | | Min | Typ | Max | | |
| LCD internal division resistance | R_{LCD} | V0 - V1, V1 - V2, V2 - V3 | — | 50 | 100 | 200 | $k\Omega$ | |
| COM0 to COM3 output impedance | R_{VCOM} | COM0 to COM3 | V1 to V3 = 5.0 V | — | — | 2.5 | $k\Omega$ | |
| SEG00 to SEG31 output impedance | R_{VSEG} | SEG00 to SEG31 | | — | — | 15 | $k\Omega$ | |
| LCDC leakage current | I_{LCDC} | V0 to V3, COM0 to COM3, SEG00 to SEG31 | — | -5 | — | 5 | μA | |

MB91230 Series

MB91F233L, MB91233L

($V_{CC} = V_{CC3} = V_{CC3B} = V_{CC3IO} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|--------------------------|--------------------|------------------|---|-------------------------|-----|------------------------|------|--|
| | | | | Min | Typ | Max | | |
| Power supply current | I _{CC} | V _{CC3} | FLASH model normal operation, T _a = +25 °C, F _{CP} = 33 MHz, F _{CPP} = 16.5 MHz | — | 65 | 75 | mA | |
| | | | FLASH model normal operation, T _a = +25 °C, F _{CP} = 33 MHz, F _{CPP} = 33 MHz | — | 73 | 83 | mA | |
| | I _{CC} | | ROM model normal operation, T _a = +25 °C, F _{CP} = 33 MHz, F _{CPP} = 16.5 MHz | — | 45 | 55 | mA | |
| | | | ROM model normal operation, T _a = +25 °C, F _{CP} = 33 MHz, F _{CPP} = 33 MHz | — | 55 | 65 | mA | |
| | I _{CC(T)} | | RTC mode, T _a = +25 °C, F _{CP} = 32 kHz | — | 20 | 50 | μA | Watch timer, RTC, LCDC V _{CC3} = V _{CC3B} = 2.4 V |
| | I _{CC(H)} | | STOP mode, T _a = +25 °C, F _{CP} = 0 MHz | — | 5 | 50 | μA | |
| | I _{CC(S)} | | SLEEP mode F _{CP} = 33 MHz, F _{CPP} = 16.5 MHz | — | 21 | 25 | mA | |
| | | | SLEEP mode F _{CP} = 33 MHz, F _{CPP} = 33 MHz | — | 30 | 35 | mA | |
| "H" level input voltage | V _{IH} | — | — | V _{CC} × 0.8 | — | V _{CC} | V | |
| | | X0A | V _{CC3B} = 2.2 V to 3.6 V | V _{CC3B} × 0.8 | — | V _{CC3B} | V | When external clock is used |
| "L" level input voltage | V _{IL} | — | — | V _{SS} | — | V _{CC} × 0.15 | V | |
| | | X0A | V _{CC3B} = 2.2 V to 3.6 V | V _{SS} | — | V _{SS} + 0.4 | V | When external clock is used |
| "H" level output voltage | V _{OH} | — | V _{CC} = 3.3 V, I _{OH} = -2 mA | V _{CC} - 0.5 | — | V _{CC} | V | |

(Continued)

MB91230 Series

(Continued)

($V_{CC} = V_{CC3} = V_{CC3B} = V_{CC3IO} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_a = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|-----------------------------------|------------|--|-------------------------|----------|-----|-----|------------------|---------|
| | | | | Min | Typ | Max | | |
| "L" level output voltage | V_{OL} | — | $I_{OL} = 2\text{ mA}$ | V_{SS} | — | 0.4 | V | |
| | | P64 to 67 | $I_{OL} = 10\text{ mA}$ | | | | | |
| Input leakage current | I_{IL} | — | — | -5 | — | 5 | μA | |
| Open-drain output leakage current | I_{leak} | — | — | -10 | — | 10 | μA | |
| LCD internal division resistance | R_{LCD} | V0 - V1, V1 - V2, V2 - V3 | — | 50 | 100 | 200 | $\text{k}\Omega$ | |
| COM0 to COM3 output impedance | R_{VCOM} | COM0 to COM3 | V1 to V3 = 5.0 V | — | — | 2.5 | $\text{k}\Omega$ | |
| SEG00 to SEG31 output impedance | R_{VSEG} | SEG00 to SEG31 | | — | — | 15 | $\text{k}\Omega$ | |
| LCDC leakage current | I_{LCDC} | V0 to V3, COM0 to COM3, SEG00 to SEG31 | — | -5 | — | -5 | μA | |

MB91230 Series

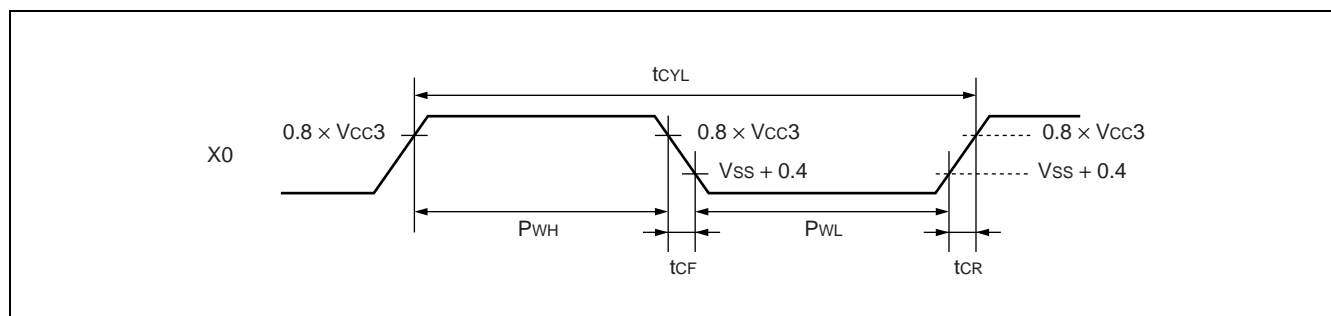
4. AC Characteristics

(1) Main clock input standard

(MB91V230, MB91F233A : $V_{CC} = 4.0\text{ V to } 5.25\text{ V}$, $V_{CC3} = V_{CC3B} = V_{CC3IO} = AV_{CC} = 3.0\text{ V to } 3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}$)

(MB91F233L, MB91233L : $V_{CC} = V_{CC3} = V_{CC3B} = V_{CC3IO} = AV_{CC} = 3.0\text{ V to } 3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|-------------------------------------|----------------------|----------|--------------------------------------|-------|-----|------|------|---|
| | | | | Min | Typ | Max | | |
| Input frequency | F_C | X0 | — | 3.6 | 4 | 4.2 | MHz | |
| Input clock cycle | t_{CYL} | | — | — | 250 | — | ns | |
| Input clock pulse width | — | | P_{WH}/t_{CYL} P_{WL}/t_{CYL} | 40 | — | 60 | % | |
| Input clock rise time and fall time | t_{CR} t_{CF} | | — | — | — | 5 | ns | At external clock |
| Internal operating clock frequency | F_{CP} | — | — | — | — | 33.6 | MHz | |
| Internal operating clock cycle time | t_{CP} | — | — | 29.7 | — | — | ns | |
| Peripheral clock frequency | F_{CPP} | — | — | — | — | 33.6 | MHz | Peripheral clock is derived from internal operating clock divided by 1/1 to 1/16. |
| Peripheral clock cycle time | t_{CYCP} | — | — | 29.7 | — | — | ns | |

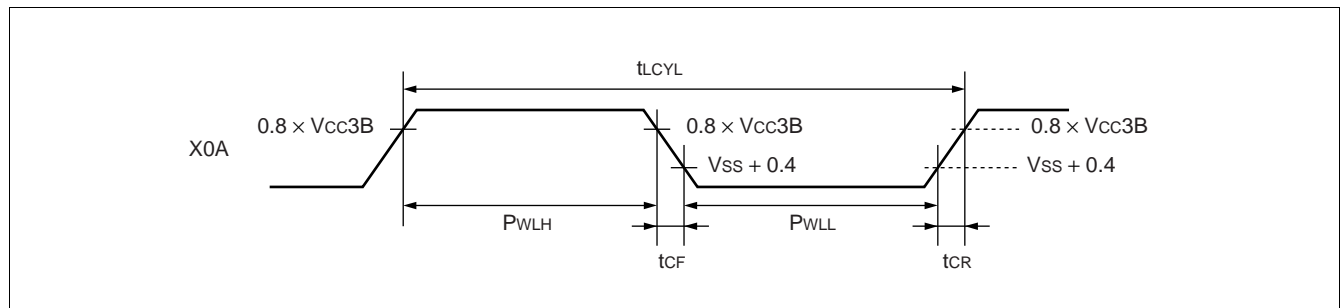


(2) Subclock input standard

(MB91V230, MB91F233A : $V_{CC} = 4.0\text{ V to }5.25\text{ V}$, $V_{CC3} = V_{CC3B} = V_{CC3IO} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$,
 $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

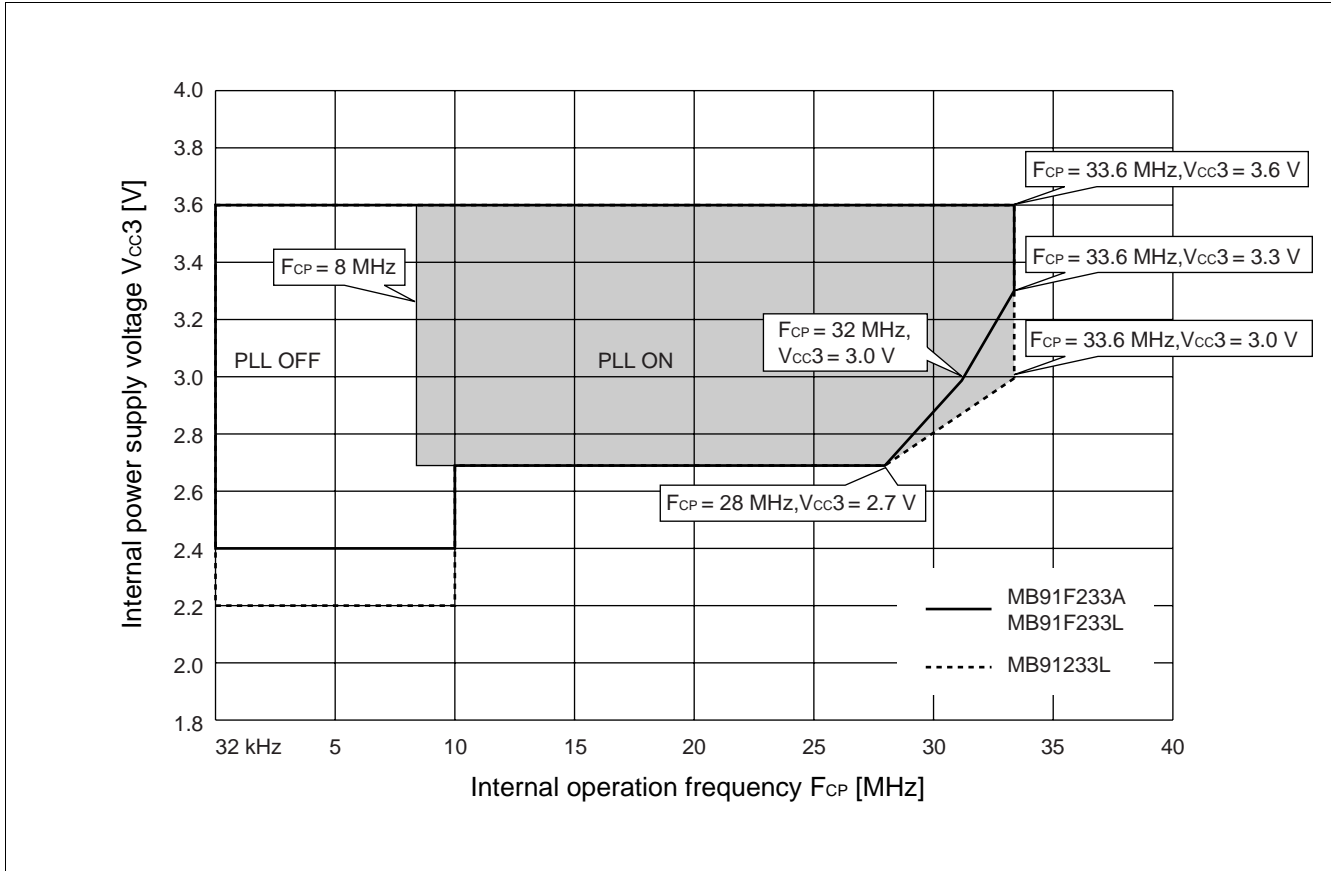
(MB91F233L, MB91233L : $V_{CC} = V_{CC3} = V_{CC3B} = V_{CC3IO} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$,
 $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|-------------------------------------|------------|--|--|--------|--------|--------|-------------------|-------------------|
| | | | | Min | Typ | Max | | |
| Input frequency | F_{CL} | X0A | — | — | 32.768 | — | kHz | At external clock |
| | | | | 28.571 | 32.768 | 35.714 | | |
| Input clock cycle | t_{LCYL} | | — | 28.0 | — | 35.0 | μs | |
| Input clock pulse width | — | | $\frac{P_{WLH}}{t_{LCYL}}$ $\frac{P_{WLL}}{t_{LCYL}}$ | 45 | — | 55 | % | |
| Input clock rise time and fall time | — | $\frac{t_{CR}}{t_{LCYL}}$ $\frac{t_{CF}}{t_{LCYL}}$ | — | — | 5 | % | At external clock | |



MB91230 Series

(3) Operation Assurance Range



(4) PLL oscillation stabilization time (LOCK UP time)

(MB91V230, MB91F233A : $V_{CC} = 4.0\text{ V to }5.25\text{ V}$, $V_{CC3} = V_{CC3B} = V_{CC3IO} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$,
 $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

(MB91F233L, MB91233L : $V_{CC} = V_{CC3} = V_{CC3B} = V_{CC3IO} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$,
 $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Value | | Unit | Remarks |
|--|-------------------|-------|-----|---------------|--|
| | | Min | Max | | |
| PLL oscillation stabilization (LOCK UP time) | t_{LOCK} | 500 | — | μs | Time from when the PLL starts operating to when its oscillation becomes stable |

(5) Reset input standards

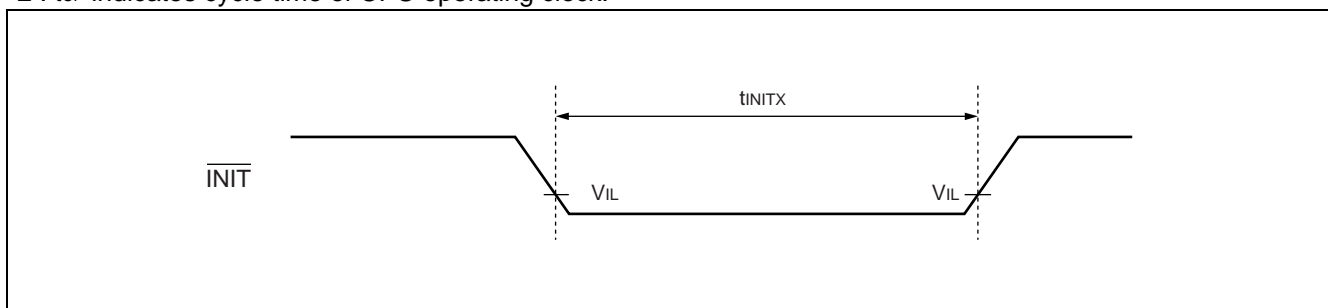
(MB91V230, MB91F233A : $V_{CC} = 4.0\text{ V to }5.25\text{ V}$, $V_{CC3} = V_{CC3B} = V_{CC3IO} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$,
 $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

(MB91F233L, MB91233L : $V_{CC} = V_{CC3} = V_{CC3B} = V_{CC3IO} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$,
 $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condi-tions | Value | | Unit | Remarks |
|--|--------------------|--------------------------|-------------|---------------------------|-----|------|---------|
| | | | | Min | Max | | |
| $\overline{\text{INIT}}$ input time (at power-on) | t_{INITX} | $\overline{\text{INIT}}$ | — | — | — | ns | *1 |
| $\overline{\text{INIT}}$ input time (other than at power-on) | | | | $t_{\text{CP}} \times 10$ | — | ns | *2 |

*1 : When turning the power on, keep $\overline{\text{INIT}}$ input until the oscillation circuit provides stable oscillation.

*2 : t_{CP} indicates cycle time of CPU operating clock.



MB91230 Series

(6)UART timing

(MB91V230, MB91F233A : $V_{CC} = 4.0\text{ V to }5.25\text{ V}$, $V_{CC3} = V_{CC3B} = V_{CC3IO} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$,
 $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

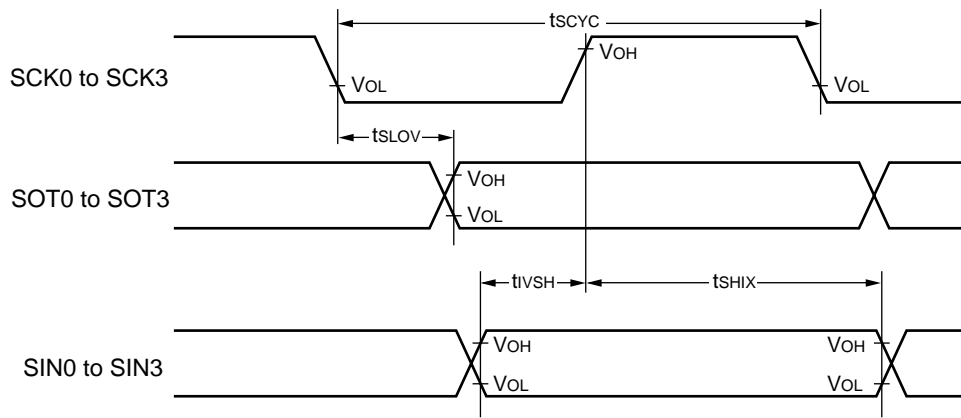
(MB91F233L, MB91233L : $V_{CC} = V_{CC3} = V_{CC3B} = V_{CC3IO} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$,
 $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|------------------------------|------------|-------------------------------|--------------------------------|-----------------------|-----|------|---------|
| | | | | Min | Max | | |
| Serial clock cycle time | t_{SCYC} | SCK0 to SCK3 | Internal shift clock operation | $t_{CYCP}^* \times 8$ | — | ns | |
| SCK ↓ → SOT delay time | t_{SLOV} | SCK0 to SCK3, SOT0 to SOT3 | | -80 | 80 | ns | |
| Valid SIN → SCK ↑ | t_{IVSH} | SCK0 to SCK3, SIN0 to SIN3 | | 100 | — | ns | |
| SCK ↑ → Valid SIN hold time | t_{SHIX} | SCK0 to SCK3, SIN0 to SIN3 | | 60 | — | ns | |
| Serial clock "H" pulse width | t_{SHSL} | SCK0 to SCK3 | External shift clock operation | $t_{CYCP}^* \times 4$ | — | ns | |
| Serial clock "L" pulse width | t_{SLSH} | SCK0 to SCK3 | | $t_{CYCP}^* \times 4$ | — | ns | |
| SCK ↓ → SOT delay time | t_{SLOV} | SCK0 to SCK3, SOT0 to SOT3 | | — | 150 | ns | |
| Valid SIN → SCK ↑ | t_{IVSH} | SCK0 to SCK3, SIN0 to SIN3 | | 60 | — | ns | |
| SCK ↑ → Valid SIN hold time | t_{SHIX} | SCK0 to SCK3, SIN0 to SIN3 | | 60 | — | ns | |

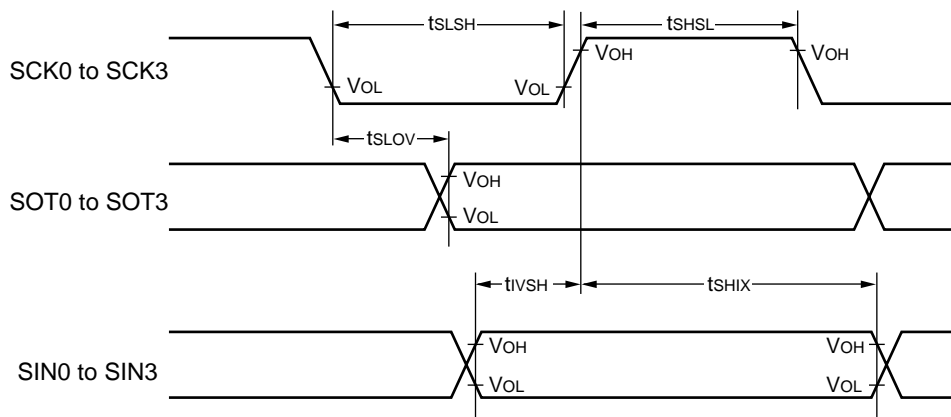
* : t_{CYCP} represents the cycle time of peripheral operating clock.

Note : The above specification applies to clock synchronous mode operation.

- Internal shift clock mode



- External shift clock mode



MB91230 Series

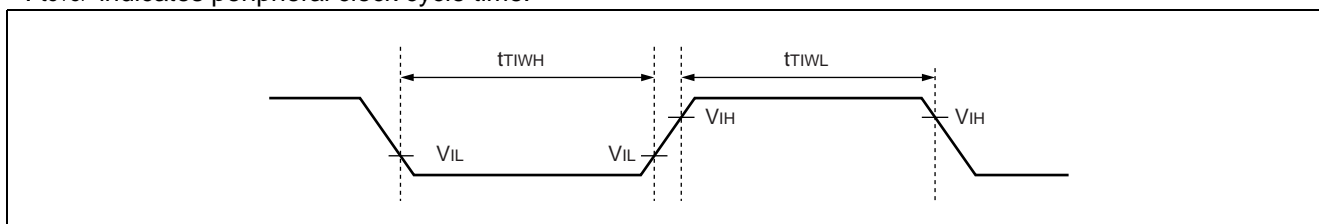
(7) Free-run timer clock, Reload timer event input, Up/down counter input, Input capture input, Interrupt input timing

(MB91V230, MB91F233A : $V_{CC} = 4.0\text{ V to }5.25\text{ V}$, $V_{CC3} = V_{CC3B} = V_{CC3IO} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

(MB91F233L, MB91233L : $V_{CC} = V_{CC3} = V_{CC3B} = V_{CC3IO} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condi-tions | Value | | Unit | Re-marks |
|-------------------|------------|--|-------------|---------------------|-----|------|----------|
| | | | | Min | Max | | |
| Input pulse width | t_{TIWH} | CKI0, CKI1 TIN0 to TIN3 IC0, IC1 AIN0, AIN1 BIN0, BIN1 ZIN0, ZIN1 | — | $t_{CYCP} \times 2$ | — | ns | * |
| | t_{TIWL} | INT0 to INT15 | | $t_{CYCP} \times 3$ | — | ns | * |

* : t_{CYCP} indicates peripheral clock cycle time.



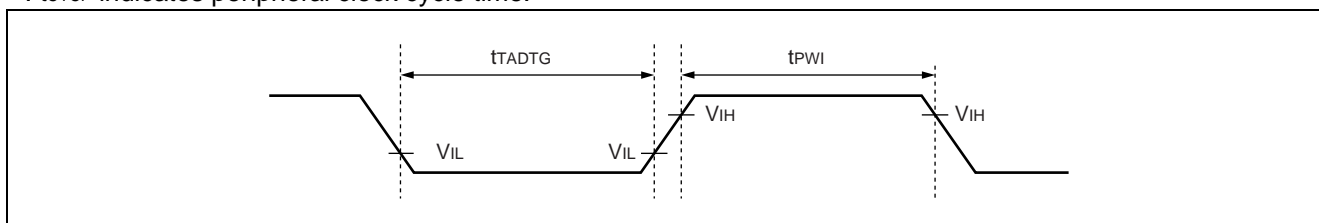
(8) A/D trigger, PWI (PWC) input timing

(MB91V230, MB91F233A : $V_{CC} = 4.0\text{ V to }5.25\text{ V}$, $V_{CC3} = V_{CC3B} = V_{CC3IO} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

(MB91F233L, MB91233L : $V_{CC} = V_{CC3} = V_{CC3B} = V_{CC3IO} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_a = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condi-tions | Value | | Unit | Remarks |
|-----------------------------|-------------|----------------|-------------|---------------------|-----|------|---------|
| | | | | Min | Max | | |
| A/D trigger input (falling) | t_{TADTG} | ADTG0 ADTG1 | — | $t_{CYCP} \times 2$ | — | ns | * |
| PWI (PWC) input (rising) | t_{PWI} | PWI0, PWI1 | — | $t_{CYCP} \times 2$ | — | ns | * |

* : t_{CYCP} indicates peripheral clock cycle time.



5. Electrical Characteristics for the A/D Converter

($V_{CC3IO} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $AVRH = 3.0\text{ V to }3.6\text{ V}$, $T_a = 0\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$)

| Parameter | Value | | | Unit | Remarks |
|---|----------|----------|----------|------|---|
| | Min | Typ | Max | | |
| Resolution | — | — | 10 | bit | AV _{CC} = 3.3 V, At AVRH = 3.3 V At CPU sleep mode |
| Total error*1 | -5.0 | — | +5.0 | LSB | |
| Nonlinear error*1 | -3.5 | — | +3.5 | LSB | |
| Differential linear error*1 | -2.5 | — | +2.5 | LSB | |
| Zero transition voltage*1 | -2.0 | +1.0 | +6.0 | LSB | |
| Full transition voltage*1 | AVRH-5.5 | AVRH-1.0 | AVRH+3.0 | LSB | |
| Conversion time | 1.69*2 | — | — | μs | |
| Power supply voltage (analog+digital) | — | 3.6 | — | mA | |
| | — | — | 5 | μA | |
| Reference power supply current (between AVRH and AVRL) | — | 470 | — | μA | AVRH = 3.0 V, At AVRL = 0.0 V*3 |
| | — | — | 10 | μA | At power-down*4 |
| Analog input capacitance | — | 40 | — | pF | |
| Inter-channel disparity | — | — | 4 | LSB | |

*1 : Measured in the CPU sleep state

*2 : It depends on the clock cycle supplied to peripheral resources.

*3 : AVRL pin is only for FLGA package product. AVRL pin is connected to AV_{SS} inside the IC on LQFP package product.

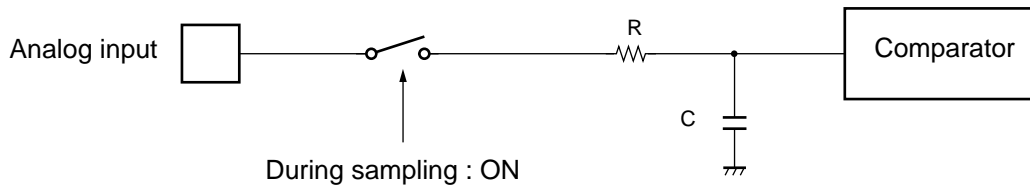
*4 : The current when the CPU is in stop mode and the A/D converter is not operating.

MB91230 Series

- **About the external impedance of the analog input and its sampling time**

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sampling and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- Analog input circuit model

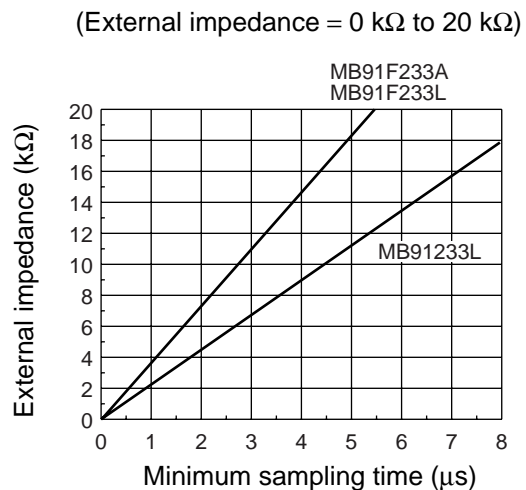
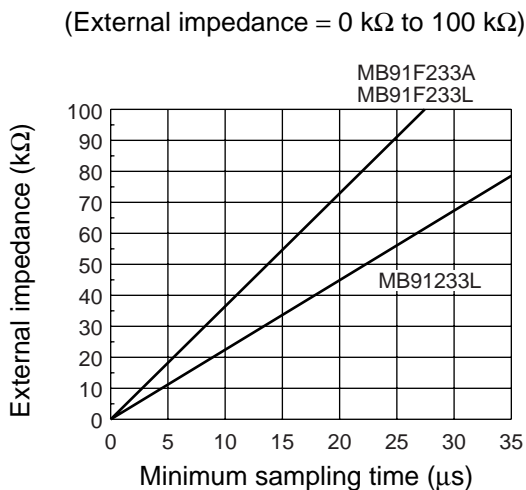


| | R | C |
|-----------|---------------|---------------|
| MB91233L | 0.18 kΩ (Max) | 63.0 pF (Max) |
| MB91F233A | 0.18 kΩ (Max) | 39.0 pF (Max) |
| MB91F233L | 0.18 kΩ (Max) | 39.0 pF (Max) |

Note : The values are reference values.

- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

- The relationship between the external impedance and minimum sampling time



- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

- About errors

As $|AVRH - AV_{SS}|$ becomes smaller, values of relative errors grow larger.

6. Electrical Characteristics for the D/A Converter

($V_{CC3IO} = AV_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_a = 0\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$)

| Parameter | Value | | | Unit | Remarks |
|---------------------------|-------|-----|------|---------------|--|
| | Min | Typ | Max | | |
| Resolution | — | — | 8 | bit | |
| Nonlinear error | -2.0 | — | +2.0 | LSB | When the output is unloaded |
| Differential linear error | -1.0 | — | +1.0 | LSB | When the output is unloaded |
| Conversion speed | — | 0.6 | — | μs | When load capacitance (C_L) = 20 pF |
| | — | 3.0 | — | μs | When load capacitance (C_L) = 100 pF |
| Output impedance | 2.0 | 2.9 | 3.8 | k Ω | |
| Analog current | — | 40 | — | μA | 10 μs conversion, when the output is unloaded |
| | — | — | 460* | μA | When the input digital code is fixed at 7A _H or 85 _H |
| | — | 0.1 | — | μA | At power-down |

* : The current consumption by D/A converter varies with input digital code.

The standard value indicates the current consumed when the digital code that maximizes the current consumption is input.

7. Flash Memory Write/Erase Characteristics

| Parameter | Conditions | Value | | | Unit | Remarks |
|---------------------------|--|--------|-----|-------|---------------|--|
| | | Min | Typ | Max | | |
| Sector erase time | $T_a = +25\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V}$ | — | 1 | 15 | s | Excludes 00 _H programming prior erasure |
| Chip erase time | $T_a = +25\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V}$ | — | 10 | — | s | Excludes 00 _H programming prior erasure |
| Byte write time | $T_a = +25\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V}$ | — | 8 | 3,600 | μs | Not including system-level overhead time. |
| Chip write time | $T_a = +25\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V}$ | — | 2.1 | — | s | Not including system-level overhead time. |
| Erase/write cycle | — | 10,000 | — | — | cycle | |
| Flash data retention time | Average $T_a = +85\text{ }^{\circ}\text{C}$ | 20 | — | — | year | * |

* : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C).

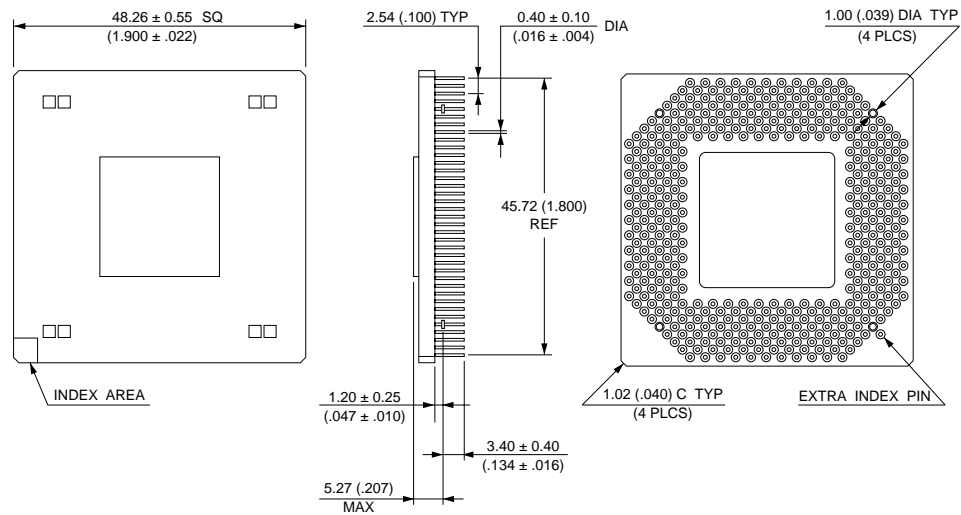
MB91230 Series

■ ORDERING INFORMATION

| Part number | Package | Remarks |
|-------------------------|--|---------|
| MB91V230CR-ES | 401-pin ceramic PGA (PGA-401C-A02) | |
| MB91F233APFF-GE1 | 120-pin plastic LQFP (FPT-120P-M05) | |
| MB91F233LPFF-GE1 | 120-pin plastic LQFP (FPT-120P-M05) | |
| MB91F233LLGA-GE1 | 128-pin plastic FLGA (LGA-128P-M01) | |
| MB91233LPFF-G-xxx-BNDE1 | 120-pin plastic LQFP (FPT-120P-M05) | |
| MB91233LLGA-G-xxx-BNDE1 | 128-pin plastic FLGA (LGA-128P-M01) | |

■ PACKAGE DIMENSIONS

401-pin Ceramic PGA
(PGA-401C-A02)



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Dimensions in mm (inches) .

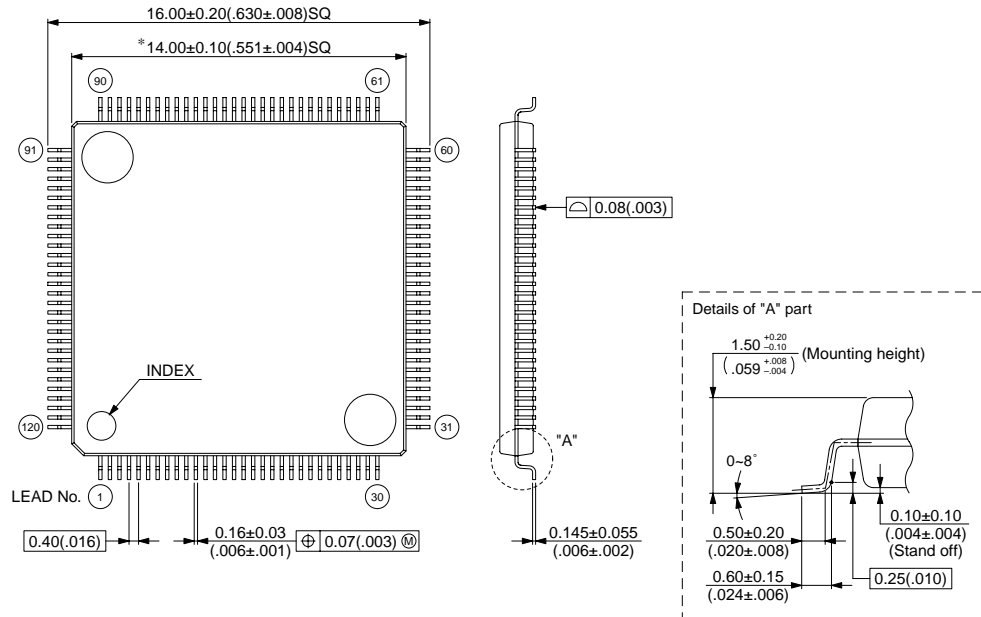
Note : The values in parentheses are reference values.

(Continued)

MB91230 Series

120-pin Plastic LQFP
(FPT-120P-M05)

Note 1) * : These dimensions do not include resin protrusion.
 Note 2) Pins width and pins thickness include plating thickness.
 Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches) .

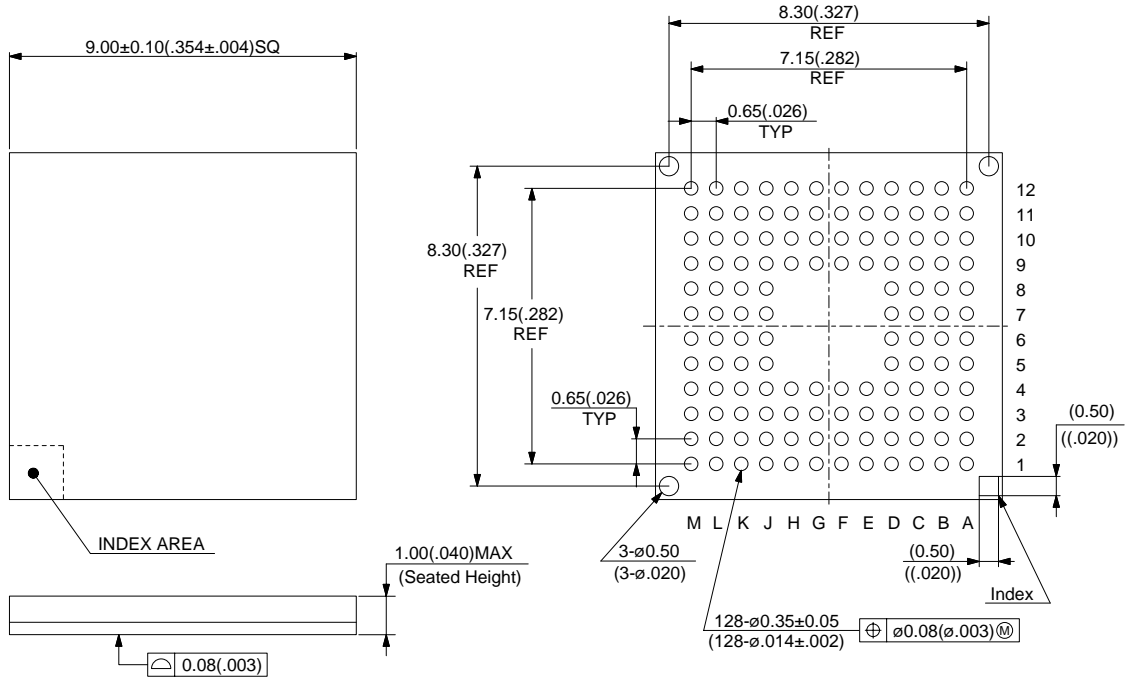
Note : The values in parentheses are reference values.

(Continued)

MB91230 Series

(Continued)

128-pin plastic FLGA
(LGA-128P-M01)



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Dimensions in mm (inches) .

Note : The values in parentheses are reference values.

MB91230 Series

The information for microcontroller supports is shown in the following homepage.
<http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html>

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