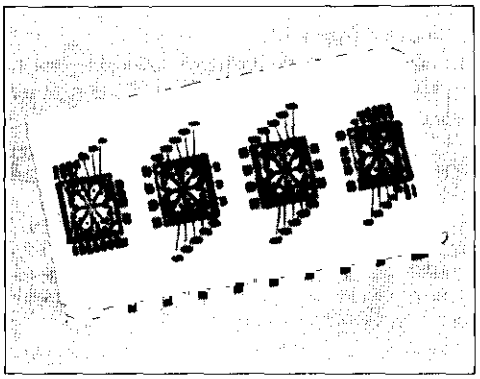
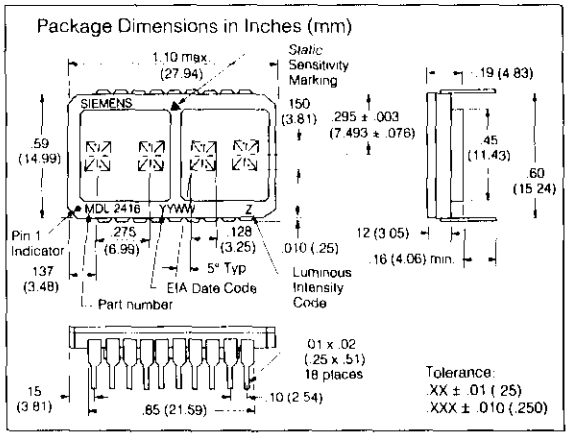
SIEMENS

MDL2416C
MDL2416TXVB

.15" Red, 4-Digit, 16 Segment Plus Decimal HI-REL Alphanumeric Intelligent Display® With Memory/Decoder/Driver





FEATURES

- **150 Mil High, Non-Magnified Monolithic Character**
- **Rugged Ceramic Package, Hermetically Sealed Flat Glass Window**
- **Low Profile Package**
- **Dual In Line Configuration**
- **Close Vertical Row Spacing, 0.600"**
- **100 Mil Pin Spacing**
- **Wide Viewing Angle**
- **Wide Temperature Operating Range, -55°C to +100°C**
- **Fully Integrated CMOS Drive Electronics**
- **Direct Access to Each Digit Independently and Asynchronously**
- **TTL Compatible, 5 Volt Power Supply**
- **Independent Cursor Function**
- **17th Segment for Improved Punctuation Marks**
- **Two Chip Enables**
- **Interdigit Blanking**
- **Display Blank Function**
- **Memory Clear Function**
- **End-Stackable, Four Character Package**
- **Intensity Coded for Display Uniformity**
- **MDL2416C Process Conforms to MIL-D-87157 Quality Level A Test Tables I, II and also can meet Groups B and C Testing Specified in MIL-D-87157**
- **MDL2416 TXVB Process Conforms to MIL-D-87157 Quality Level A Test Tables I, II, IIIa and IVa (See High Reliability Test Tables)**

DESCRIPTION

The MDL2416 is a military alphanumeric four digit display module with a 17 segment font and a built-in CMOS drive circuitry that is TTL and microprocessor compatible.

The integrated circuit contains memory, ASCII ROM decoder, multiplexing circuitry and drivers. The MDL2416 is designed for use in extremely harsh environments where only the most reliable product is acceptable.

Data entry is asynchronous and can be random. A display system can be built using any number of MDL2416s since each digit in any MDL2416 can be addressed independently and will continue to display the character last stored until replaced by another.

System interconnection is straightforward. The least significant two address bits (A0, A1) are normally connected to the like named inputs of all MDL2416s in the system. With two chip enables ($\overline{CE1}$ and $\overline{CE2}$), four MDL2416s (16 characters) can easily be interconnected without an external decoder.

Important: *Since this is a CMOS device, normal precautions should be taken to avoid static damage due to high static voltages or electric fields. See Appnote 18 for further information.*

Optoelectronic Characteristics at 25°C

Absolute Maximum Ratings

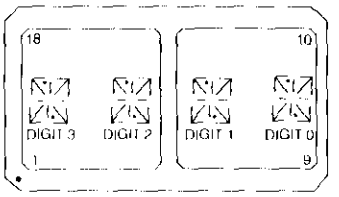
DC Supply Voltage ..... -0.5 to +6.0 VDC
Input Voltage Relative to Gnd
(all inputs) ..... 0.5 to V_{CC} +0.5 VDC
Operating Temperature ..... -55°C to +100°C
Storage Temperature ..... -65°C to +125°C

Optical Characteristics

Spectral Peak Wavelength ..... 660 nm typ.
Spectral Line Half-Width ..... 40 nm typ.
Viewing Angle (see Note) ..... ±50°
Digit Size ..... 0.15"
Luminous Intensity (typ.) ..... 0.1 mcd/segment at V_{CC}=5 V
Intensity Matching,
Segment to Segment ..... 1.8:1 at V_{CC}=5 V

Note: "Off axis viewing angle" is defined as, the minimum angle in any direction from the normal to the display surface at which any part of any segment in the display is not visible

Top View



Pin	Function	Pin	Function
1	$\overline{CE1}$ Chip Enable	10	GND
2	$\overline{CE2}$ Chip Enable	11	D0 Data Input
3	$\overline{CLR}$ Clear	12	D1 Data Input
4	$\overline{CUE}$ Cursor Enable	13	D2 Data Input
5	$\overline{CU}$ Cursor Select	14	D3 Data Input
6	$\overline{WR}$ Write	15	D6 Data Input
7	A1 Digit Select	16	D5 Data Input
8	A0 Digit Select	17	D4 Data Input
9	V_{CC}	18	BL Display Blank

DC Characteristics at 25°C

Parameter	Min.	Typ.	Max.	Units	Conditions
V_{CC}	4.5	5.0	5.5	V	25°C
I_{CC} (Blank)[1]	0.10	1.5	4.0	mA	V_{CC}=5 V, $\overline{WR}$=V_{CC}, V_{IN}= 0 V all other pins
I_{CC} (10 segments/character 4 digits on)	65	85	115	mA	V_{CC}=5 V
I_{CC} (all segments on cursor in 4 digits)[1,2]	85	120	165	mA	V_{CC}=5 V meausred at 5 sec., 60 sec. max.
V_{IL} (all inputs)			0.6	V	V_{CC}=5 V ±0.5 V
V_{IH} (all inputs)	2.4			V	V_{CC}=5 V ±0.5 V
I_{IL} (all inputs)		60	160	µA	V_{CC}=5 V, V_{IN}=0.8 V

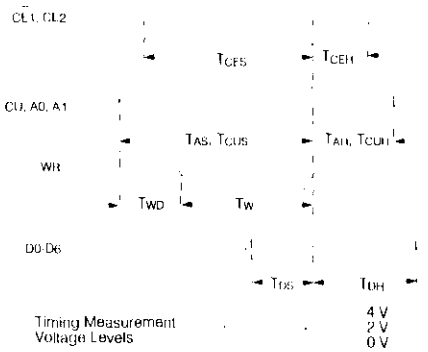
1. Measured at 5 seconds.
2. 60 seconds maximum duration.

AC Characteristics

Parameter	Symbol	–55°C	+25°C	+100°C	Units
Chip Enable Set Up Time	T_{CES}	190	275	410	ns
Address Set Up Time	T_{AS}	190	275	410	ns
Cursor Set Up Time	T_{CUS}	190	275	410	ns
Chip Enable Hold Time	T_{CEH}	25	25	25	ns
Address Hold Time	T_{AH}	25	25	25	ns
Cursor Hold Time	T_{CUH}	25	25	25	ns
Write Delay Time	T_{WD}	40	50	60	ns
Write Pulse	T_{W}	150	225	350	ns
Data Set Up Time	T_{DS}	100	150	300	ns
Data Hold Time	T_{DH}	25	25	25	ns
Clear Pulse	T_{CLR}	0.9	1	1.2	µs

Note: 1. Unused inputs must be tied to an appropriate logic voltage level (either V+ or V-).

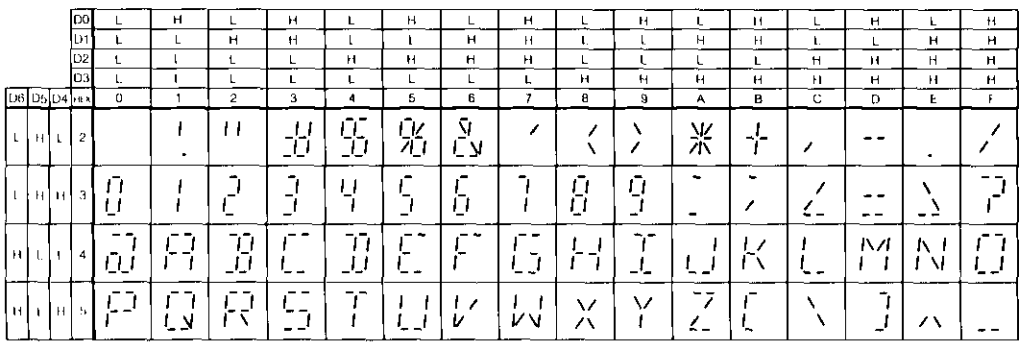
Timing Characteristics
Write Cycle Waveforms



Timing Measurement Voltage Levels . . . 4 V / 2 V / 0 V

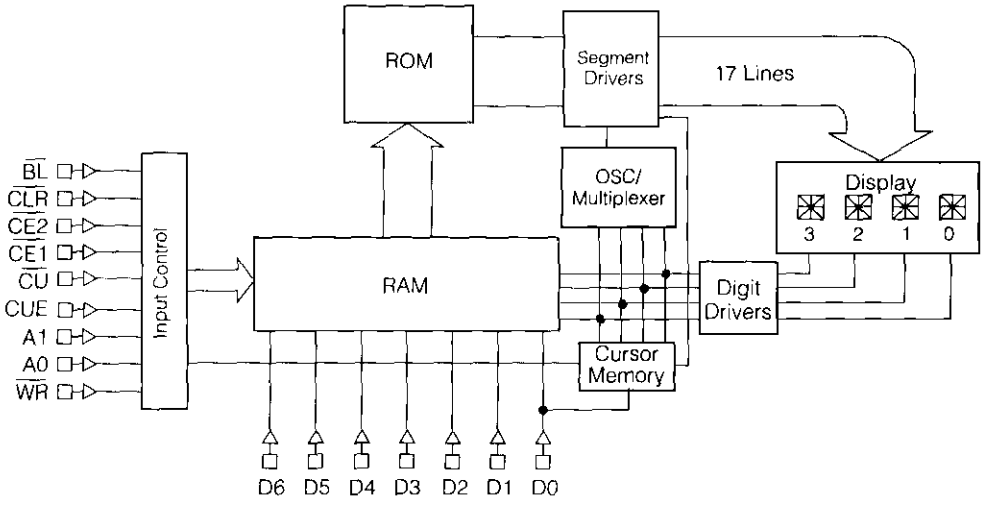
(for tester calibration only)

Character Set

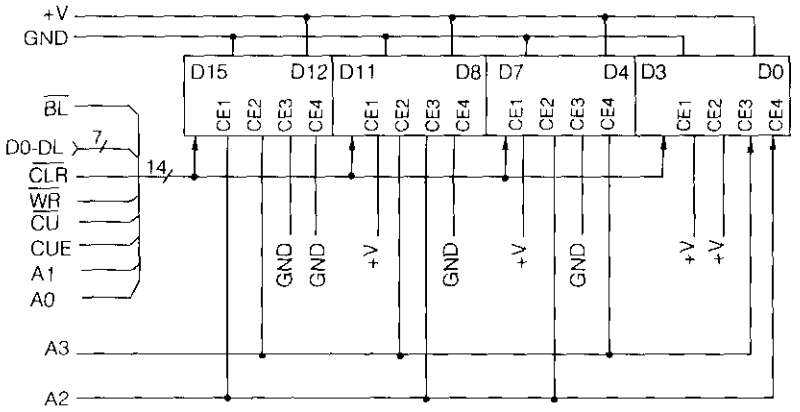


All other input codes display "blank"

Internal Block Diagram



Typical Schematic for 16 Digit System



Loading Data

Setting the chip enable ($\overline{CE1}$, $\overline{CE2}$) to their true state will enable data loading. The desired data code (D0-D6) and digit address (A0, A1) must be held stable during the write cycle for storing new data.

Data entry may be asynchronous and random. (Digit 0 is defined as right hand digit with A1 = A2 = 0.)

Clearing the entire internal four-digit memory can be accomplished by holding the clear ($\overline{CLR}$) low for one μS minimum. The clear function will clear both the ASCII RAM and the cursor RAM. Loading an illegal data code will display a blank.

Loading Cursor

Setting the chip enables ($\overline{CE1}$, $\overline{CE2}$) and cursor select ($\overline{CU}$) to their true state will enable cursor loading. A write ($\overline{WR}$) pulse will now store or remove a cursor into the digit location addressed by A0, A1, as defined in data entry. A cursor will be stored if D0=1; and will be removed if D0=0. The cursor ($\overline{CU}$) pulse width should not be less than the write ($\overline{WR}$) pulse or erroneous data may appear in the display.

If the cursor isn't required, the cursor enable signal (CUE) may be tied low to disable the display of the cursor function. For a flashing cursor, simply pulse CUE. If the cursor has been loaded to any or all positions in the display, then CUE will control whether the cursor(s) or the characters appear. CUE does not affect the contents of cursor memory.

Display Blanking

To blank the display, load a blank or space into each digit of the display or use the ($\overline{BL}$) display blank input.

Setting the ($\overline{BL}$) input low does not affect the contents of either data or cursor memory. A flashing display will result by pulsing ($\overline{BL}$).

A flashing circuit can be easily constructed using a 555 astable multivibrator. Figure 1 illustrates a circuit in which varying R1 (100K~10K) will have a flash rate of 1Hz~10Hz.

The display can be dimmed by pulse width modulating the ($\overline{BL}$) at a frequency sufficiently fast not to interfere with the internal clock. This clock frequency may vary from 200 Hz to 1.3KHz. The dimming signal frequency should be 2.5KHz or higher. Dimming the display also reduces power consumption.

Typical Loading Data State Table

Control							Address		Data							Display Digit			
$\overline{BL}$	$\overline{CE1}$	$\overline{CE2}$	CUE	$\overline{CU}$	$\overline{WR}$	$\overline{CLR}$	A1	A0	D6	D5	D4	D3	D2	D1	D0	3	2	1	0
H	X	X	L	X	H	H	previously loaded display									G	R	E	Y
H	H	X	L	X	X	H	X	X	X	X	X	X	X	X	X	G	R	E	Y
H	X	H	L	X	X	H	X	X	X	X	X	X	X	X	X	G	R	E	Y
H	L	L	L	H	L	H	L	L	H	L	L	L	H	L	H	G	R	E	E
H	L	L	L	H	L	H	L	H	H	L	H	L	H	L	H	G	R	U	E
H	L	L	L	H	L	H	H	L	H	L	L	H	H	L	L	G	L	U	E
H	L	L	L	H	L	H	H	H	H	L	L	L	L	H	L	B	L	U	E
L	X	X	X	X	H	H	X	X	blank display										
H	L	L	L	H	L	H	H	H	H	L	L	L	H	H	H	G	L	U	E
H	X	X	L	X	H	L	X	X	clears character displays							see character set			
H	L	L	L	H	L	H	X	X	see character code										

X = don't care

Loading Cursor State Table

Control							Address		Data							Display Digit			
$\overline{BL}$	$\overline{CE1}$	$\overline{CE2}$	CUE	$\overline{CU}$	$\overline{WR}$	$\overline{CLR}$	A1	A0	D6	D5	D4	D3	D2	D1	D0	3	2	1	0
H	X	X	L	X	H	H	previously loaded display									B	E	A	R
H	X	X	H	X	H	H	display previously stored cursors									B	E	A	R
H	L	L	H	L	L	H	L	L	X	X	X	X	X	X	H	B	E	A	■
H	L	L	H	L	L	H	L	H	X	X	X	X	X	X	H	B	E	■	■
H	L	L	H	L	L	H	H	L	X	X	X	X	X	X	H	B	■	■	■
H	L	L	H	L	L	H	H	H	X	X	X	X	X	X	H	■	■	■	■
H	L	L	H	L	L	H	H	L	X	X	X	X	X	X	L	■	F	■	■
H	X	X	L	X	H	H	disable cursor display									B	F	A	R
H	L	L	L	L	L	H	H	H	X	X	X	X	X	X	L	B	F	A	R
H	X	X	H	X	H	H	display stored cursors									B	F	■	■

■ = X