BURR-BROWN®

ADC601

ABRIDGED DATA SHEET
For Additional Technical Information, Request PDS-867.

12-Bit 900ns ANALOG-TO-DIGITAL CONVERTER

FEATURES

- FAST CONVERSION: 900ns
- CAN BE SHORT-CYCLED
- INPUT RANGES: ±5V, ±10V, 0 to –10V
- HIGH SIGNAL/NOISE RATIO: 68dB
- LOW IMD: 75dB
- PARALLEL AND SERIAL OUTPUT
- 32-PIN CERAMIC DIP PACKAGE

APPLICATIONS

- DIGITAL SIGNAL PROCESSING
- HIGH-SPEED DATA ACQUISITION SYSTEMS
- MEDICAL INSTRUMENTATION
- ANALYTICAL INSTRUMENTATION
- TEST AND IMAGING SYSTEMS
- WAVEFORM ANALYZERS

DESCRIPTION

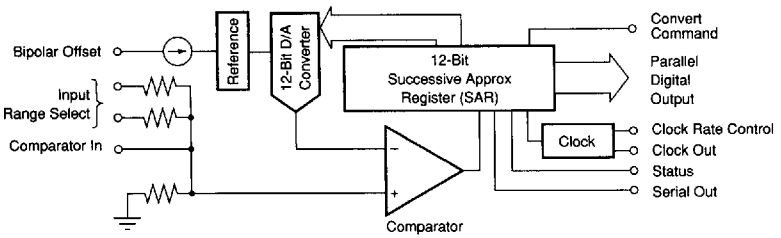
The ADC601 is a high-speed Duolithic™ (two chips) successive approximation analog-to-digital converter. This unique two-chip design utilizes a bipolar technology with on-chip thin film resistors to preserve analog accuracy and a high-speed CMOS chip to perform digital logic control. Outstanding linearity, noise, and dynamic range are achieved by this converter design. The ADC601 has been tested with several sample/hold amplifiers and distortion results are documented in this data sheet.

The ADC601 is complete with internal reference, clock, and comparator and is packaged in a 32-pin ceramic DIP. Conversion time is set at the factory to 900ns. Serial and parallel output performance is guaranteed with no missing codes over the full input voltage, power supply, and operating temperature range. The gain and offset errors are laser trimmed to specification. Optionally they may be externally adjusted to zero.

Internal scaling resistors are provided for the selection of analog signal input ranges of ±5V, ±10V and 0V to –10V. The ADC601's input is specifically designed to be easily driven with minimal disturbance to the driving amplifier.

Output codes are available in complementary binary for unipolar inputs and bipolar offset binary for bipolar inputs.

All digital inputs and outputs are TTL-compatible. Power supply requirements are ±15V and +5V.



Duolithic™ Burr-Brown Corporation

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_{CASE} = +25°C, 900ns conversion time, $\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, and 6-minute warm-up in a normal convection environment unless otherwise noted.

PARAMETER	CONDITIONS	ADC601JG MIN	ADC601JG TYP	ADC601JG MAX	ADC601KG MIN	ADC601KG TYP	ADC601KG MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG CHARACTERISTICS								
INPUTS								
Voltage Ranges: Bipolar	Full Scale(FSR)[1][2]		±5, ±10			*		V
Unipolar	Full Scale(FSR)[1][2]		0 to –10			*		V
Impedance: –10V to 0V, ±5V			1.4			*		kΩ
±10V			2.4			*		kΩ
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error[3]	990ns Conversion Time		±0.08	±0.55		*	±0.2	%
Input Offset Error[3]: Unipolar	990ns Conversion Time		±0.12	±1.2		*	±0.5	% of FSR
Bipolar	990ns Conversion Time		±0.08	±0.8		*	±0.25	% of FSR
Integral Linearity Error	990ns Conversion Time			±0.024			±0.012	% of FSR
Differential Linearity Error	990ns Conversion Time			±0.024			±0.012	% of FSR
No Missing Codes				Guaranteed				
Power Supply Rejection of Offset and Gain	$\Delta +V_{CC}$ = ±5%		±0.0036			*		%FSR/%V_{CC}
	$\Delta -V_{CC}$ = ±5%		±0.0005			*		%FSR/%V_{CC}
	$\Delta +V_{DD}$ = ±5%		±0.001				*	%FSR/%V_{DD}
DIGITAL CHARACTERISTICS								
INPUT								
Logic Family				TTL-Compatible CMOS				
Convert Command Logic Voltages	Logic Low	0		+0.8	*		*	V
	Logic High	+2		$+V_{DD}$	*		*	V
Convert Command Currents	Logic Low			–150				µA
	Logic High			–150				µA
Convert Command				High Level When Converting				
CONVERSION TIME								
Factory Set	Without User Adjustment		0.9	1		*	*	µs
Power Supply Rejection of Conversion Time	D $+V_{DD}$ = ±5%		±1			*		ns/%V_{DD}
OUTPUT								
Logic Family				TTL-Compatible CMOS				
Bits 1 through 12, Serial, Status, Clock Out	Logic Low, I_{OL} = 3.2mA		+0.1	+0.4		*	*	V
	Logic High, I_{OH} = –1mA	+2.7	+4.9		*	*	*	V
Internal Clock Frequency			13			*		MHz
Status				Low Level When Data Valid				
DYNAMIC CHARACTERISTICS [4][5][6] Tested using Sample/Hold Amplifier SHC804 and ADC601 (See Typical Performance Curves)								
Differential Linearity Error	f_C = 10kHz: 68.3% of All Codes		0.5			0.4		LSB
	99.7% of All Codes		0.8			0.6		LSB
	100% of All Codes		1.0			0.7		LSB
Total Harmonic Distortion	f_C = 10kHz, f_S = 500kHz		–70			*		dBc
	f_C = 10kHz, f_S = 1MHz		–74			*		dBc
	f_C = 250kHz, f_S = 500kHz		–70			*		dBc
	f_C = 500kHz, f_S = 1MHz		–68			*		dBc
Two-Tone Intermodulation Distortion[7]	f_C = 11kHz and 15kHz, f_S = 500kHz		–79			*		dBc
	f_C = 50kHz and 55kHz, f_S = 500kHz		–78			*		dBc
	f_C = 90kHz and 110kHz, f_S = 500kHz		–77			*		dBc
Signal-to-Noise and Distortion	f_C = 250kHz, f_S = 500kHz		66			*		dB
(SINAD) Ratio	f_C = 500kHz, f_S = 1MHz		65			*		dB
Signal-to-Noise Ratio (SNR)	f_C = 250kHz, f_S = 500kHz		68			*		dB
	f_C = 500kHz, f_S = 1MHz		67			*		dB
PERFORMANCE OVER TEMPERATURE								
Gain	T_{MIN} to T_{MAX}		±10	±30		*	*	ppm of FSR/°C
Input Offset: Unipolar	T_{MIN} to T_{MAX}		±2	±7		*	*	ppm of FSR/°C
Bipolar	T_{MIN} to T_{MAX}		±3	±10		*	*	ppm of FSR/°C
Internal Linearity Error	0.9µs Conversion Time T_{MIN} to T_{MAX}		±0.02			±0.015		% of FSR
Differential Linearity Error	0.9µs Conversion Time T_{MIN} to T_{MAX}		±0.02			±0.015		% of FSR
No Missing Codes	0.9µs Conversion Time T_{MIN} to T_{MAX}			Guaranteed				
Conversion Drift			2			*		ns/°C

SPECIFICATIONS (CONT)

ELECTRICAL

T_{CASE} = +25°C, 900ns conversion time, $\pm V_{CC}$ = ±15V, $+V_{DD}$ = +5V, and 6-minute warm-up in a normal convection environment unless otherwise noted.

PARAMETER	CONDITIONS	ADC601JG			ADC601KG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$		+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		−14.25	−15	−15.75	*	*	*	V
$+V_{DD}$		+4.75	+5	+5.25	*	*	*	V
Supply Currents: $+I_{CC}$			5.4	7.0		*	*	mA
$-I_{CC}$			−65	−84.5		*	*	mA
$+I_{DD}$			53	68.9		*	*	mA
Power Consumption	Nominal $\pm V_{CC}$ and $+V_{DD}$		1.3	1.7		*	*	W
Thermal Resistance, θ_{JC}			25			*	*	°C/W
TEMPERATURE RANGE[8]								
Specification		0		+70	*		*	°C
Operating		−25		+85	*		*	°C

* Same specifications as for ADC601JG.

NOTES: (1) Over or under range on the analog input results in constant maximum or minimum digital output. (2) FSR = Full Scale Range. (3) Adjustable to zero. (4) Dynamic tests are performed using SHC804 with ADC601 unless otherwise specified. Performance may vary depending upon choice of sample/hold. (5) See Typical Performance Curves. (6) dBc = level referred to carrier input signal = 0dB; f_c = input frequency; f_s = sampling frequency. (7) IMD is referred to the larger of the two input test signals. If referred to the peak envelope signal (=0dB), the intermodulation products will be 6dB lower. For example, unit connected for ±10V has 20V FSR. (8) Temperature ranges refer to case temperature. Thermal resistance was measured on a small (5" diameter) handwired circuit board; with the test device in a (zero insertion force) socket. Thermal resistance will be lower if the ADC601 is soldered into the PC board, a ground plane is used directly underneath the package, multiple PC board layers are used, or forced air cooling is employed. Use heat sinking if necessary to keep the case at specified and operating temperatures.

ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±18V
$+V_{DD}$	+7V
Digital Inputs	+5.5V
Analog Inputs	$\pm V_{CC}$
Comparator Input	−3.7V to +0.7V
Case Temperature	+125°C
Junction Temperature	+165°C
Storage Temperature	−65°C to +150°C

Stresses above these ratings may permanently damage the device.

ORDERING INFORMATION

ADC601 ( ) G

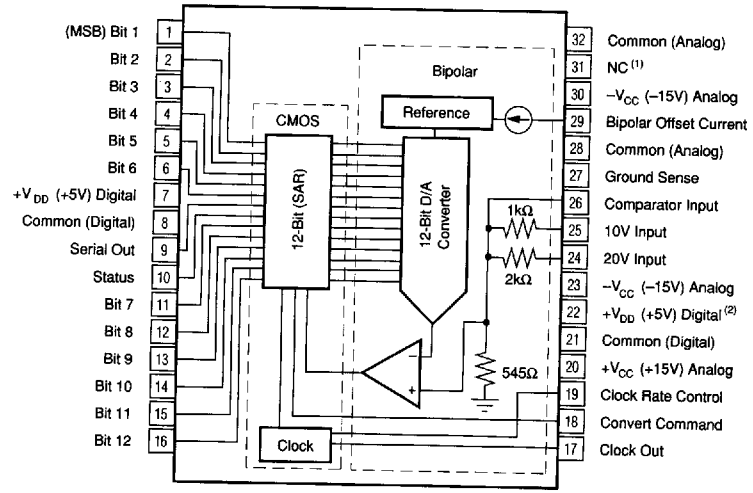
- Basic Model Number
- Performance Grade Code
  - J, K: 0°C to +70°C Case Temperature
- Package Code
  - G: Ceramic DIP

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADC601JG	32-Pin Hermetic DIP	172-2
ADC601KG	32-Pin Hermetic DIP	172-2

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN CONFIGURATION



(1) NC = No internal connection. Any voltage may be connected to pin 31, however.
(2) Pin 22 must be very cleanly decoupled to keep digital noise out of the analog circuits.

PIN DEFINITIONS

PIN NUMBER	DESIGNATION	DESCRIPTION
1-6 and 11-16	Bit 1 to Bit 12	12-bit parallel output data capable of sinking 3.2mA.
9	Serial Out	12-bit serial data output synchronized with the negative edge of each appropriate clock cycle.
10	Status	Conversion status strobe is high during data conversion; low when parallel data is valid. Negative edge may be used to latch parallel data, however, appropriate latch set-up time must be provided. Refer to t_{BEL} in the ADC601 timing diagram.
17	Clock Out	Negative edge indicates when serial data is valid. After convert command goes high, fist cycle clocks bit 1 (MSB). The clock continues to run when convert command is high and resets low with convert command.
18	Convert Command	High transition starts conversion; and should remain high during conversion. Low will reset clock and SAR logic.
19	Clock Rate Control	May be used to increase clock speed, by increasing the positive portion of the clock. High is normal operation.
24	20V Input	20V input range allows ±10Vp-p analog input signal. Short to ground when not used.
25	10V Input	10V input range allows 0 to –10Vp-p or ±5Vp-p input range.
26	Comparator In	Only used in bipolar mode when it is connected to bipolar offset pin through short lead with low resistance.
27	Ground Sense	Ground Sense pin. (See text for use).
29	Bipolar Offset Current	Bipolar offset current short to comparator In through very short lead with very low resistance for bipolar operation. Short to ground for unipolar operation.