VITESSE

VSC830
Data Sheet

2.7Gb/s Asynchronous Dual 2x2 Crosspoint Switch

FEATURES

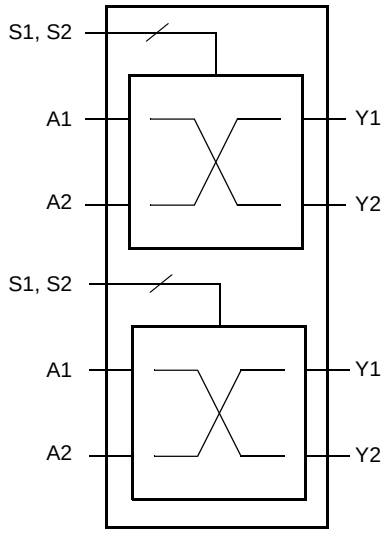
- Dual 2x2 Crosspoint Switch
- 2.7Gb/s NRZ Data Bandwidth, 2.7GHz Signal Bandwidth
- PECL/TTL-Compatible Control Inputs
- PECL-Compatible High-Speed I/O
- 50Ω Source Terminated Output Driver and Programmable Input Terminations
- Single 3.3V Supply, 1W Typical Dissipation
- Power-Down Capability for Unused Outputs
- Compact 44-Pin PQFP, 10mm x 10mm Package

GENERAL DESCRIPTION

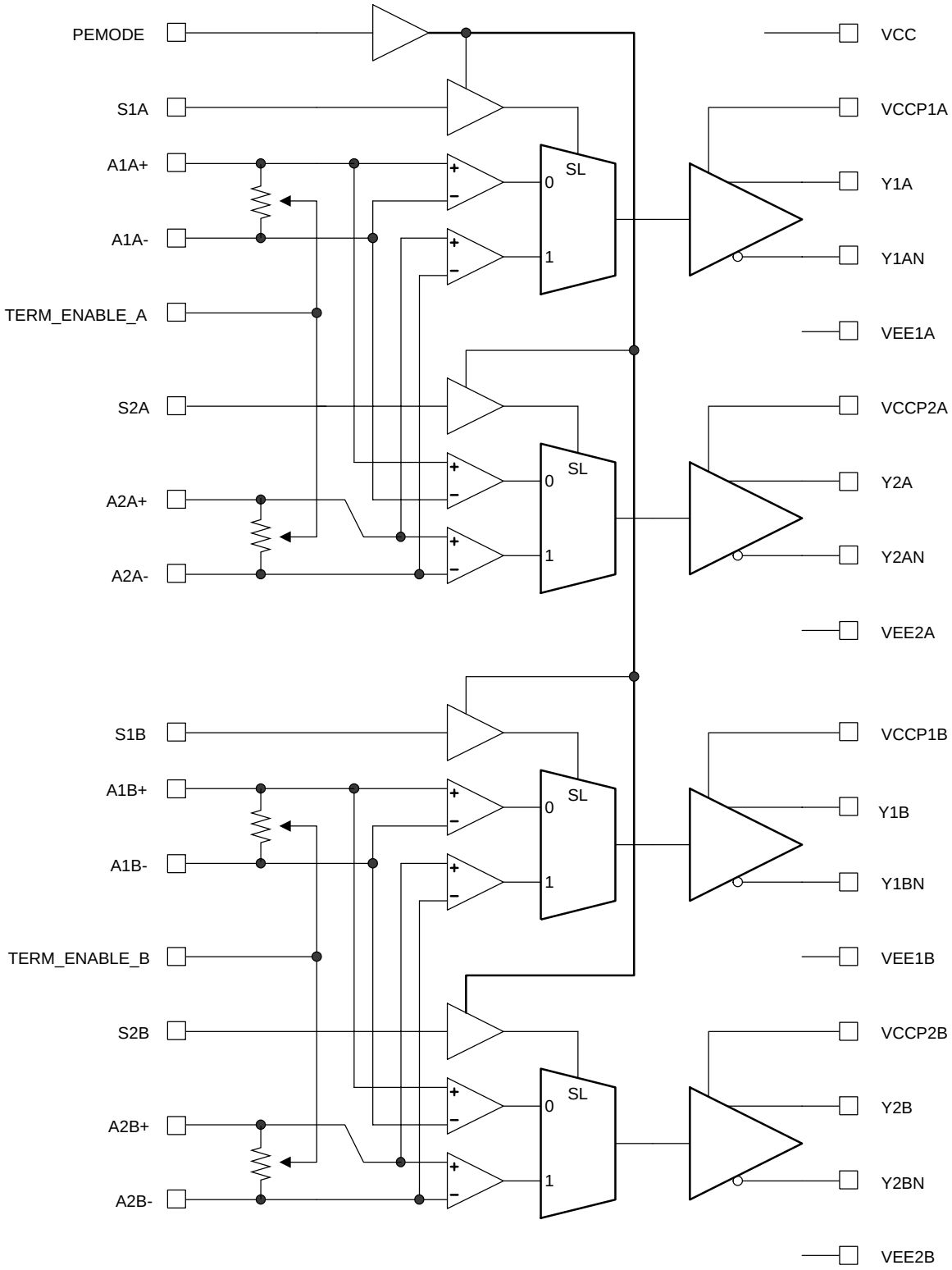
The VSC830 is a monolithic dual 2x2 asynchronous crosspoint switch, designed for critical signal path control and buffering applications, such as loopback, protection switching, and multi-channel backplane driver/receivers. Signal path delay is tightly matched between each output channel to eliminate the need for delay path compensation when switching between signal sources.

The crosspoint function is based on a multiplexer tree architecture. Each 2x2 switch can be considered as a pair of 2:1 multiplexers that share the same inputs. The signal path through each switch is fully differential and delay matched. The signal path is unregistered, so there are no restrictions on the phase, frequency, or signal pattern at each input. Unused outputs can be independently powered off, thereby eliminating power on unused sections (see “Termination Schemes” on page 5). The switch control inputs can be configured to be compatible with PECL or TTL levels. The high-speed input and output levels are nominally PECL compatible and capable of interfacing with a wide range of termination schemes.

VSC830 Block Diagram



VSC830 Functional Block Diagram



FUNCTIONAL DESCRIPTION

Select

As shown in Figure 1, each output can be treated as a 2:1 multiplexer, with the A1 and A2 inputs common to both multiplexers. The select input S1 independently controls the state of the multiplexer that drives output Y1, and select input S2 independently controls the output of Y2. Table 1 specifies the function of the select inputs.

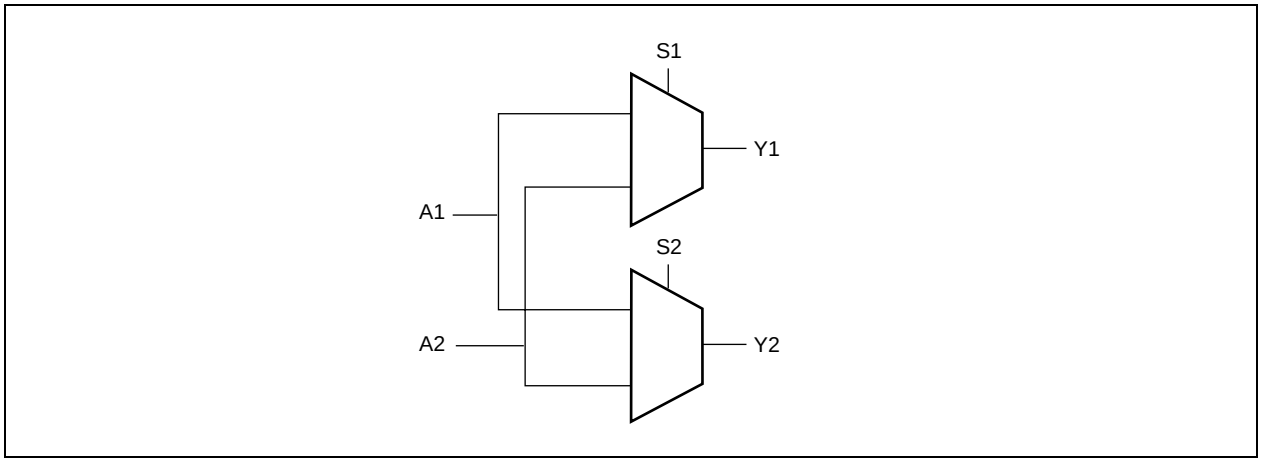


Figure 1. Select Functional Block Diagram

Table 1. Select Function

S1	S2	Y1	Y2
0	0	A1	A1
1	0	A2	A1
0	1	A1	A2
1	1	A2	A2

MODE

The interface level of the select pins, S1 and S2, can be programmed to either TTL or PECL levels by shorting the MODE pin to either V_{CC} or V_{EE}. Note that the MODE pin must be tied to either V_{CC} or V_{EE}. The function of MODE is specified in Table 2.

Table 2. MODE Function

MODE	S1, S2
V_{EE}	TTL
V_{CC}	PECL

Power-Down

Power to each output stage is provided through V_{CC}, V_{CCP}, and V_{EE}. V_{CC} is common to all outputs. To power off unused outputs, tie the respective V_{EE} and V_{CCP} pin to V_{CC}, as shown in Figure 2. Minimum power configuration requires output channel 1A active, so power must be applied to V_{CCP}1A and V_{EE}1A at all times.

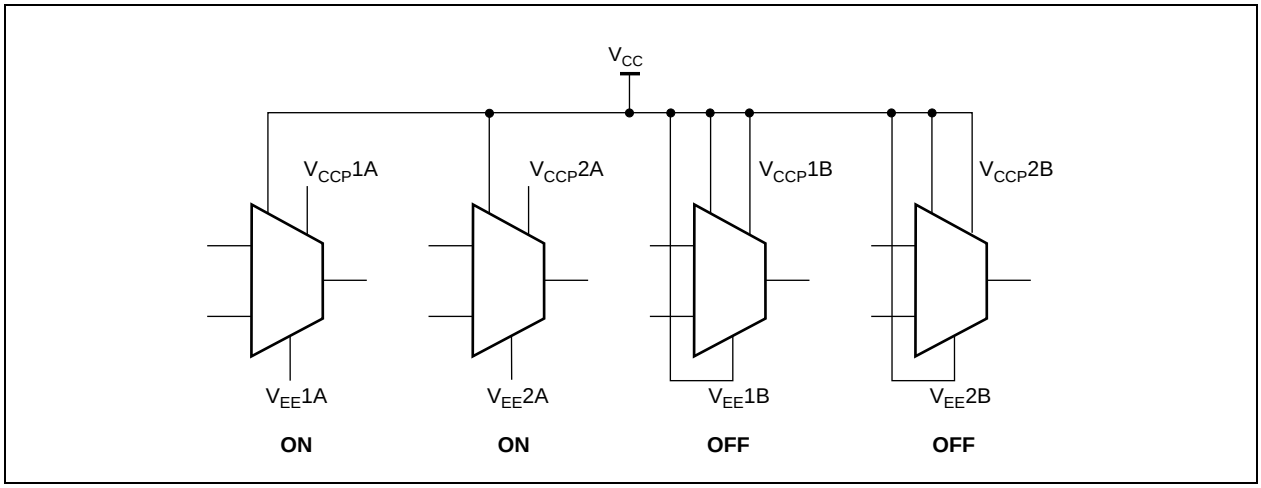


Figure 2. Power-Down Mode Example

Programmable Input Termination

Across each differential input (from the + input to the - input) of the VSC830 is a switched 100Ω termination resistor. Using the TERM_ENABLE pin, the termination can be optionally disabled. To enable the input termination, connect the respective TERM_ENABLE pin to V_{CC}. To disable the internal termination, connect TERM_ENABLE to V_{EE}. If unconnected, the TERM_ENABLE pin will self-bias to V_{EE} and disable the internal termination. Independent termination controls are provided for the A and B switches.

Termination Schemes

Signal Terminations

The high-speed inputs (A1A±, A1B±, A2A± and A2B±) on the VSC830 are internally terminated with a programmable 100Ω termination between the true and complement input. The input termination can be disabled by connecting the TERM_ENABLE pin to VEE. High impedance internal biasing resistors provide the correct bias voltage at the inputs for AC-coupled applications as shown in Figure 3.

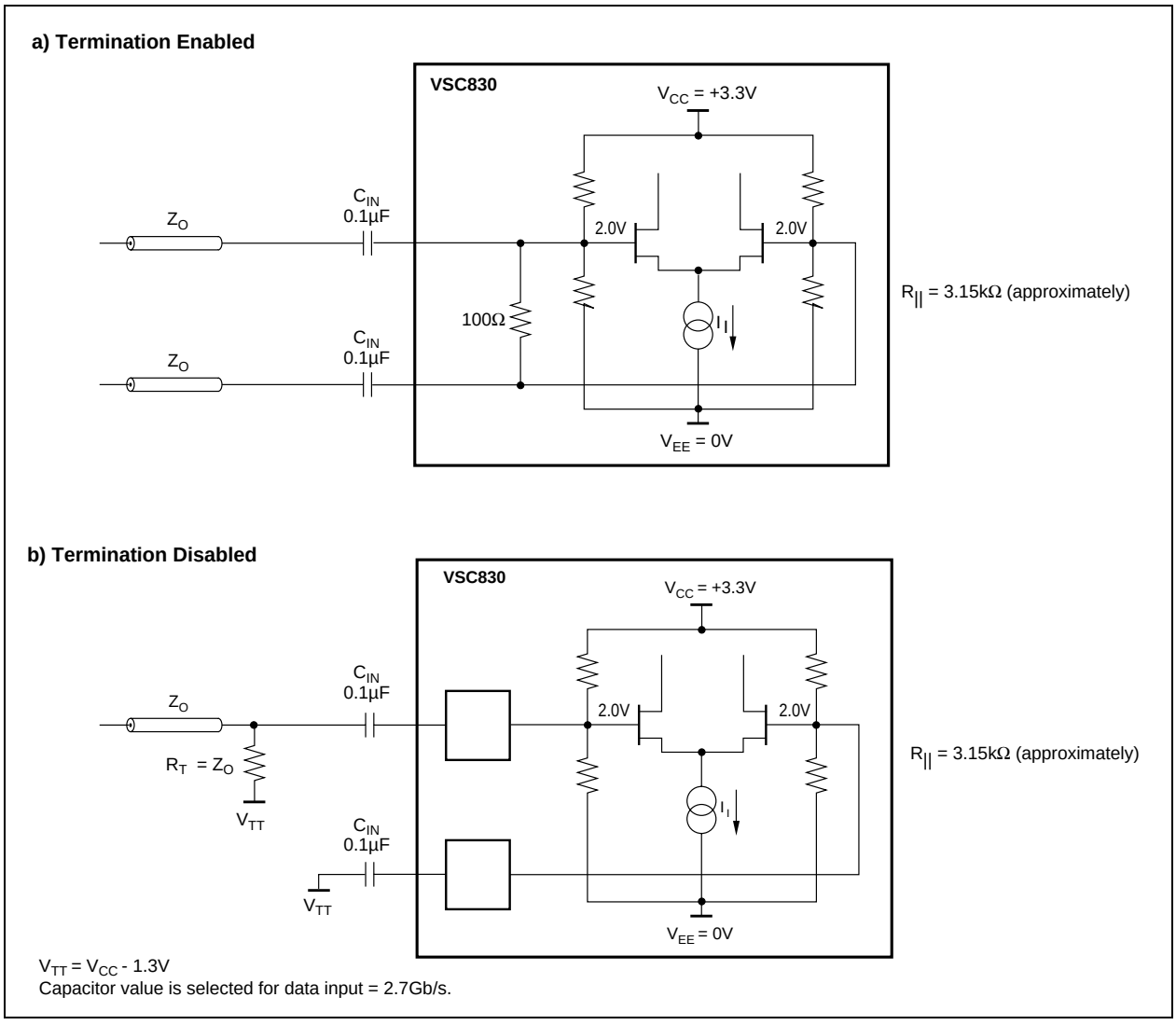


Figure 3. High-Speed Input Termination

The high-speed outputs (Y1A±, Y1B±, Y2A± and Y2B±) each consist of a differential pair designed to drive a 50Ω transmission line. The transmission line should be terminated with a 100Ω resistor at the receiver of the downstream device between the true and complement outputs. No connection to a termination voltage is required. The output driver is source terminated to 50Ω on-chip, providing a snubbing of any reflections. Output power can be cut by tying V_{EE} to V_{CC}. In single-ended mode, the unused output must be terminated with 50Ω. Examples of output terminations are shown in Figure 4 on page 6.

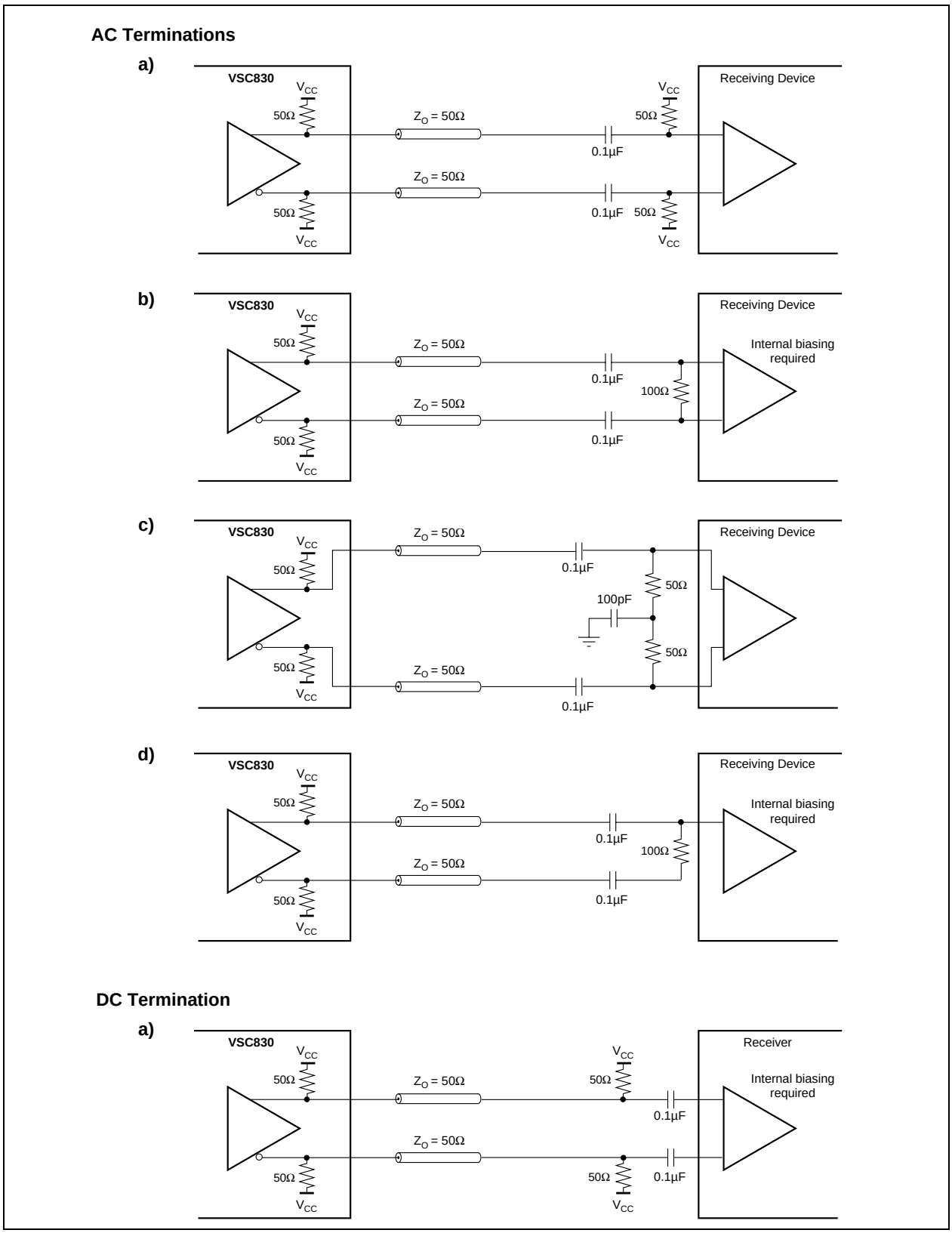


Figure 4. Termination Examples of High-Speed Outputs (Y1A±, Y1B±, Y2A±, Y2B±)

LAYOUT CONSIDERATIONS

Power Supply

The VSC830 is a single supply part, requiring only a 3.3V supply. The location and hook-up of the bypass capacitors is critical to providing the VSC830 with a clean 3.3V power supply. V_{CC} that are adjacent can share a 0.027µF capacitor connected to V_{EE}.

Normally the four channel specific V_{CC} pins (V_{CC}P1A, V_{CC}P1B, V_{CC}P2A, V_{CC}P2B) are connected to one common V_{CC} plane. In the same way the four channel specific V_{EE} pins are connected to the common V_{EE} plane. A suggested decoupling schematic for this configuration is shown in Figure 4d. However, a slightly higher signal integrity can be achieved if these pins are treated as different power supplies. In this case, V_{CC}P1A should then be decoupled to V_{EE}1A, etc, as shown in Figure 4b.

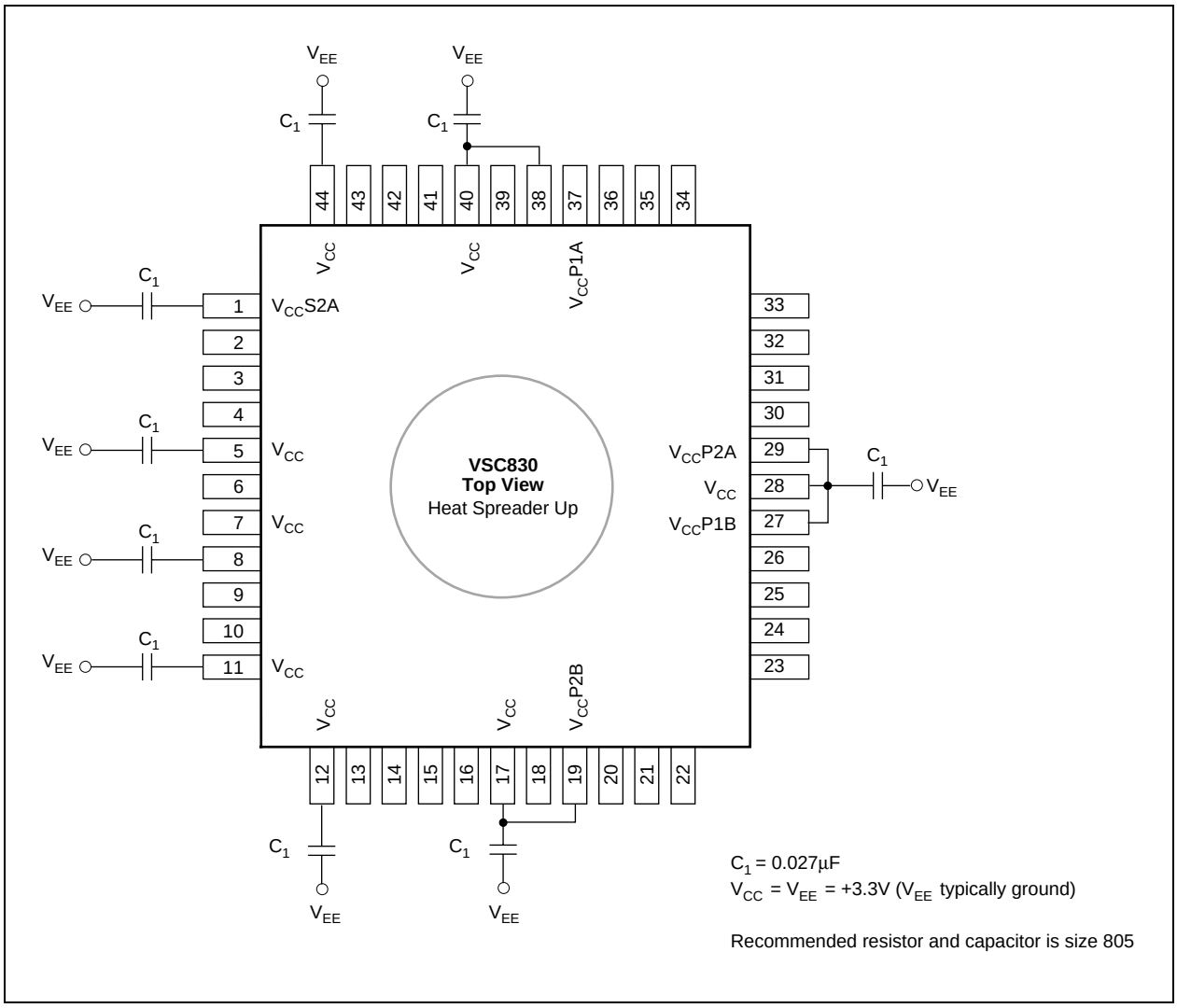


Figure 5. Decoupling Example: Common V_{CC} and V_{EE} Planes

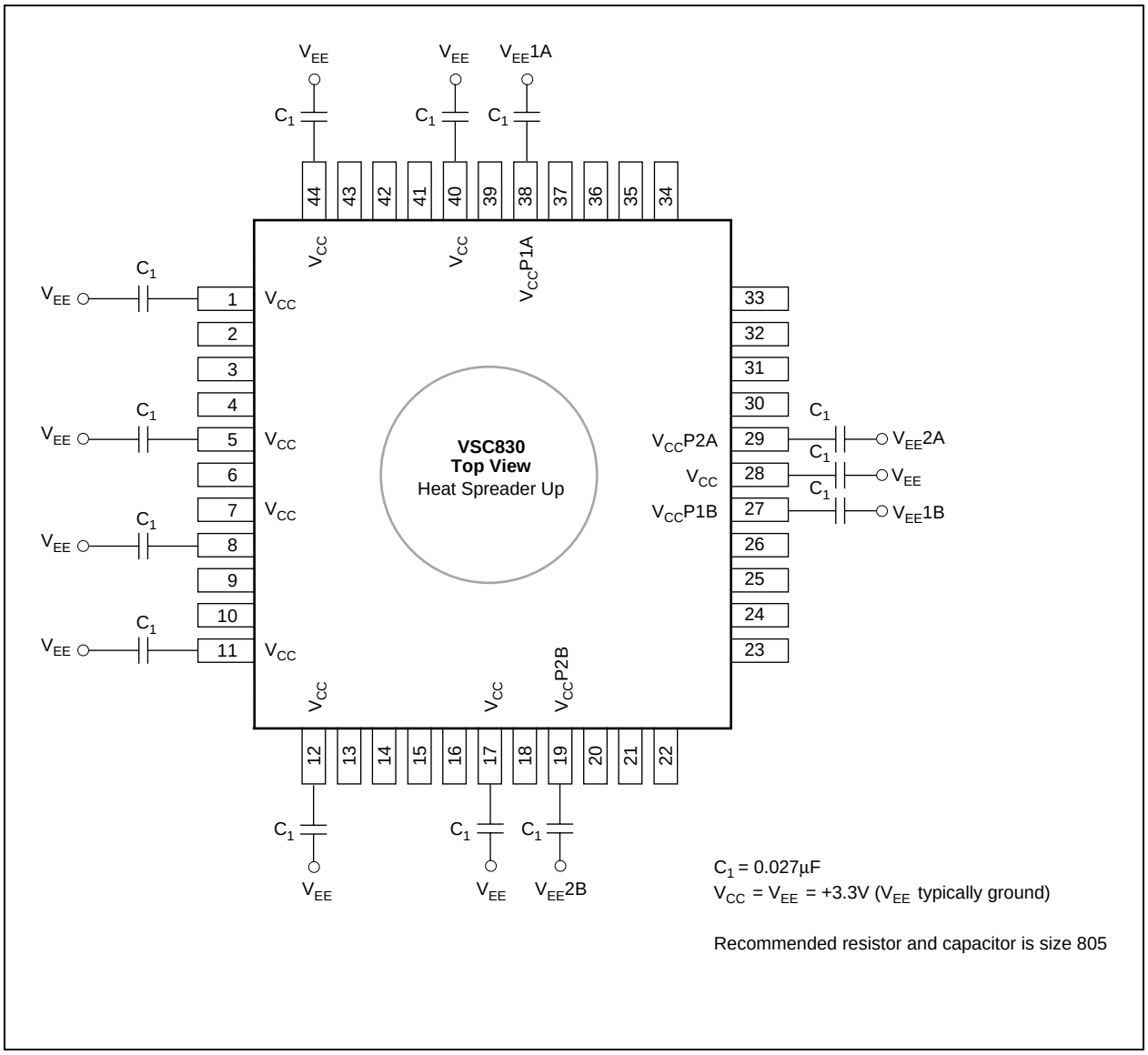


Figure 6. Decoupling Example: Separate V_{CC} and V_{EE} Planes

High-Speed Serial Inputs/Outputs

The high-speed serial signals contain digital data at fundamental frequencies up to 2.488GHz clock rate. Given that, in order to preserve the edges of such data sequences, it is necessary to have excellent frequency and phase response up to at least the 3rd harmonic, if not the 7th harmonic. Improved signal quality will result should the reader follow the general design rules below:

1. Keep traces as short as possible. Initial component placement should be very carefully considered.
2. The impedance of the traces must match that of the terminations, connectors and cable(s) in order to reduce reflections and impedance mismatches. Reflections can create standing waves that will increase the signal jitter.
3. Differential transmission line impedance must be maintained at 100Ω.
4. When routing differential pairs, keep the lengths identical for both traces. Differences in trace length translate directly into signal skew and can add to the signal jitter. Remember also that the differential impedance is affected by the separation between the traces.
5. Keep differential pair traces on the same side of the PCB to minimize impedance discontinuity, such as the one caused when using printed-circuit board vias.
6. Eliminate or reduce stubs.
7. Use rounded corners rather than 45° or 90° corners.
8. Keep signal traces far from other signals which might capacitively couple noise into the signals. This includes the other trace of a differential pair or the traces of the parallel PECL or TTL interface.
9. Do not cut up the power or ground planes in an effort to steer current paths. This usually produces more noise, not less.

SPECIFICATIONS

DC Characteristics

Over recommended operating cnditions unless stated otherwise.

Table 3. Power Supply

Symbol	Parameter	Min	Typ	Max	Units	Condition
I_{CC}	Total $V_{CC(P)}$ supply current			350	mA	
P_D	Power dissipation per output (Y1A±, Y2A±, Y1B±, Y2B±)			300	mW	
P_T	Total chip power (all outputs powered on)			1.2	W	

NOTE: *Specified with outputs terminated, 100Ω between true and complement, V_{CC} = 3.45V.*

Table 4. Select Input Levels, TTL

Symbol	Parameter	Min	Typ	Max	Units	Condition
V_{IH}	Input HIGH voltage	2.0			V	
V_{IL}	Input LOW voltage			0.8	V	
I_{IH}	Input HIGH current			500	µA	V_{IN} = 2.4V
I_{IL}	Input LOW current			–500	µA	V_{IN} = 0.5V

Table 5. Select Input Levels, PECL

Symbol	Parameter	Min	Typ	Max	Units	Condition
V_{IH}	Input HIGH voltage	V_{CC} – 1.0			V	
V_{IL}	Input LOW voltage			V_{CC} – 1.6	V	
I_{IH}	Input HIGH current			500	µA	V_{IN} = 2.5V
I_{IL}	Input LOW current			–500	µA	V_{IN} = 1.5V

Table 6. Control Inputs

Symbol	Parameter	Min	Typ	Max	Units	Condition
R_{PEMODE}	PEMODE pin impedance		3100		Ω	

Table 7. A Input Levels, Differential PECL

Symbol	Parameter	Min	Typ	Max	Units	Condition
V_{ID}	Input differential voltage(1)	200		1000	mV	
V_{ICM}	Input common-mode voltage	V_{CC} – 1.7		V_{CC} – 0.9	V	

1. *Peak-to-peak swing of each side of the differential input.*

Table 8. Y Output Levels, Differential PECL

Symbol	Parameter	Min	Typ	Max	Units	Condition
V_{OD1}	Output differential voltage (data)(1)	400	700	1000	mV	
V_{OD2}	Output differential voltage (clock)(2)	400	550	850	mV	
V_{OCM}	Output common-mode voltage	V_{CC} – 1.6		V_{CC} – 1.0	V	

1. *Peak-to-peak swing of each side of the differential output with 2^{23}-1 PRBS data.*
2. *Peak-to-peak swing of each side of the differential output using alternating 1, 0 pattern.*

AC Characteristics

Table 9. AC Timing

Symbol	Parameter	Min	Typ	Max	Units	Condition
F_{RATE}	Signal path data rate			2.7	Gb/s	
F_{BW}	Signal path bandwidth (-3dB)			2.7	GHz	
T_{SKW}	Channel-to-channel delay skew		50		ps	
T_{CON}	Switch configuration setup time(1)			1	ns	
t_R, t_F	High-speed output rise/fall times(2)			150	ps	20% to 80%
t_{Jp-p}	Signal path added jitter, peak-to-peak(1)			40	ps	

1. *Tested on a sample basis only with 2^{23}-1 PRBS data, input signal rise/fall time <150ps. Value stated in table is added to measurement system jitter.*
2. *Input signal rise/fall time <150ps, measured using alternating 1, 0 pattern.*

Table 10. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{CC}, V_{CCP}	Power supply voltage	3.135	3.3	3.465	V	
T	Operating temperature range(1) **VSC830** **VSC830-01**	 0 –40		 +85 +85	 °C °C	

1. *Lower limit of specification is ambient temperature and upper limit is case temperature.*

Table 11. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Condition
V_{CC}	Power supply voltage, potential to ground	–0.5	+4.0	V	
	DC input voltage (TTL, ECL inputs)	-0.5	V_{CC} +0.5	V	
	Output current		50	mA	
T_C	Case temperature under bias	–55	+125	°C	
T_S	Storage temperature	–65	+150	°C	
V_{ESD}	ESD (human body model)		1500	V	

Stresses listed under “Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliabiility of the device.

PACKAGE INFORMATION

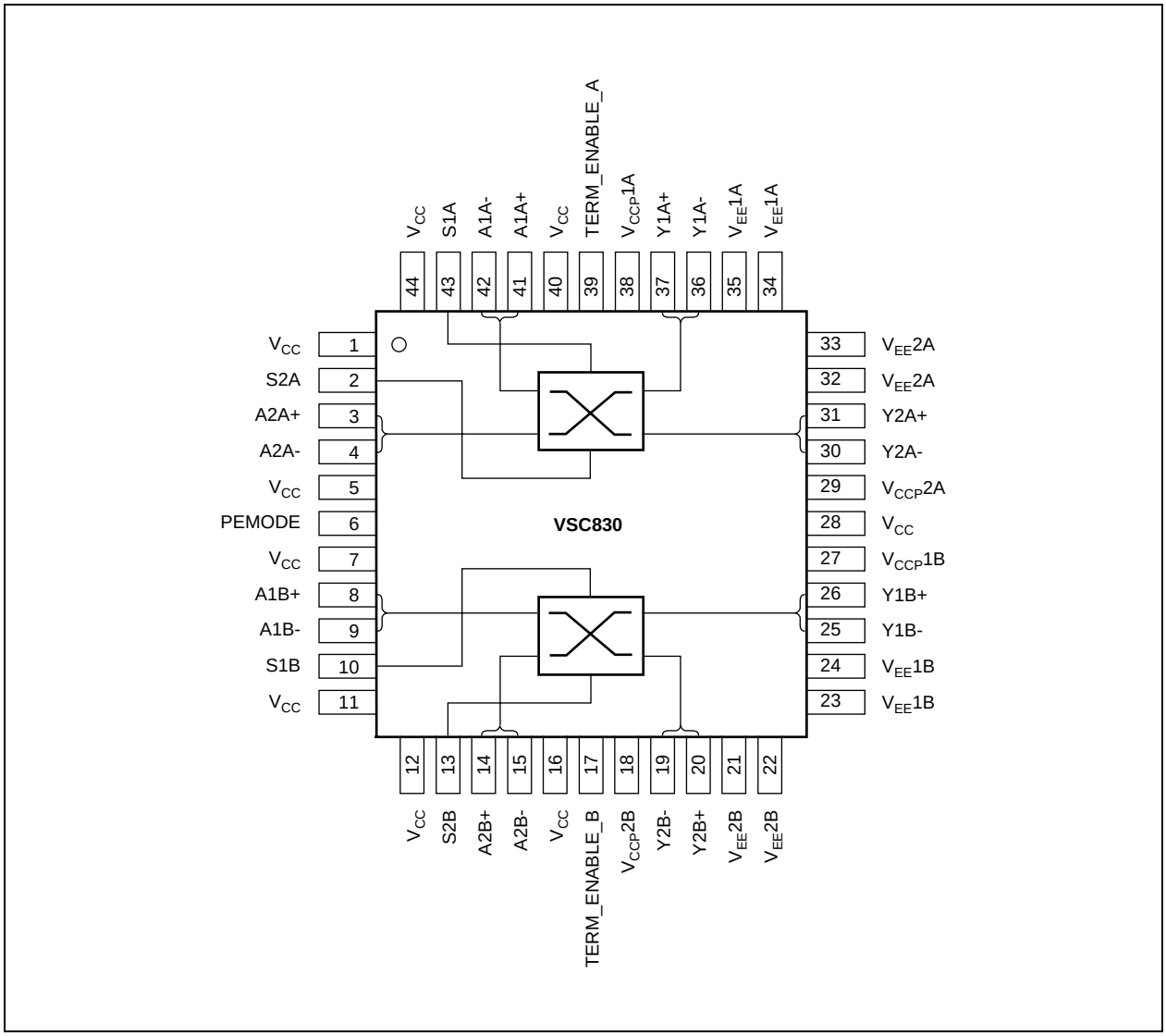


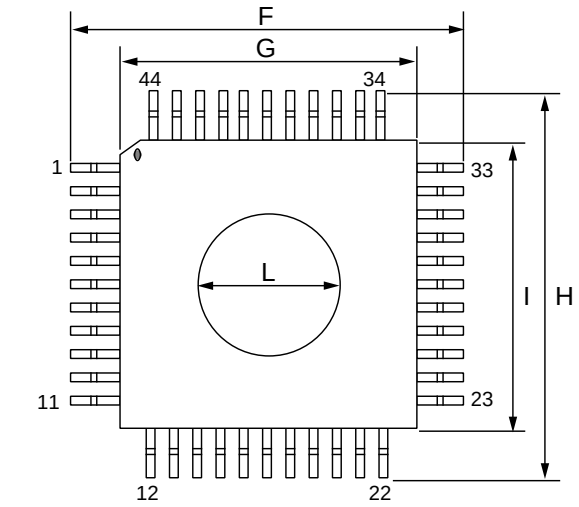
Figure 7. Pin DIagram for 44-Pin PQFP (QZ)

Table 12. Pin Identification for 44-Pin PQFP (QZ)

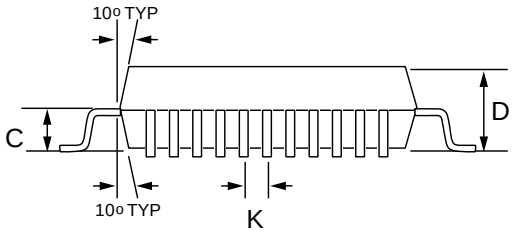
Pin Number	Signal	I/O	Type	Description
1	V_{CC}		Pwr	Power Supply, 3.3V
2	S2A	I	PECL, TTL	Channel 2A Input Selector
3	A2A+	I	PECL	Channel 2A Signal Input, True.
4	A2A–	I	PECL	Channel 2A Signal Input, Complement
5	V_{CC}		Pwr	Power Supply, 3.3V
6	PEMODE		Control	
7	V_{CC}		Pwr	Power Supply, 3.3V
8	A1B+	I	PECL	Channel 1B Signal Input, True.
9	A1B–	I	PECL	Channel 1B Signal Input, Complement.
10	S1B	I	PECL, TTL	Channel 1B Input Selector
11	V_{CC}		Pwr	Power Supply, 3.3V
12	V_{CC}		Pwr	Power Supply, 3.3V
13	S2B	I	PECL, TTL	Channel 2B Input Selector
14	A2B+	I	PECL	Channel 2B Signal Input, True.
15	A2B–	I	PECL	Channel 2B Signal Input, Complement.
16	V_{CC}		Pwr	Power Supply, 3.3V
17	TERM_ENABLE_B	I	Control	Input Termination Enable for B Switch. Normally LOW (V_{EE}). Connect to V_{CC} to enable internal 100Ω termination between AxA± inputs.
18	V_{CCP}2B		Pwr	Output driver power supply for channel 2B.
19	Y2B–	O	PECL	Channel 2B Output, Complement
20	Y2B+	O	PECL	Channel 2B Output, True
21	V_{EE}2B		Pwr	Ground for Channel 2B
22	V_{EE}2B		Pwr	Ground for Channel 2B
23	V_{EE}1B		Pwr	Ground for Channel 1B
24	V_{EE}1B		Pwr	Ground for Channel 1B
25	Y1B–	O	PECL	Channel 1B Output, Complement
26	Y1B+	O	PECL	Channel 1B Output, True
27	V_{CCP}1B		Pwr	Output Driver Power Supply for Channel 1B
28	V_{CC}		Pwr	Power Supply, 3.3V
29	V_{CCP}2A		Pwr	Output Driver Power Supply for Channel 2A
30	Y2A–	O	PECL	Channel 2A Output, Complement
31	Y2A+	O	PECL	Channel 2A Output, True
32	V_{EE}2A		Pwr	Ground for Channel 2A
33	V_{EE}2A		Pwr	Ground for Channel 2A
34	V_{EE}1A		Pwr	Ground for Channel 1A
35	V_{EE}1A		Pwr	Ground for Channel 1A

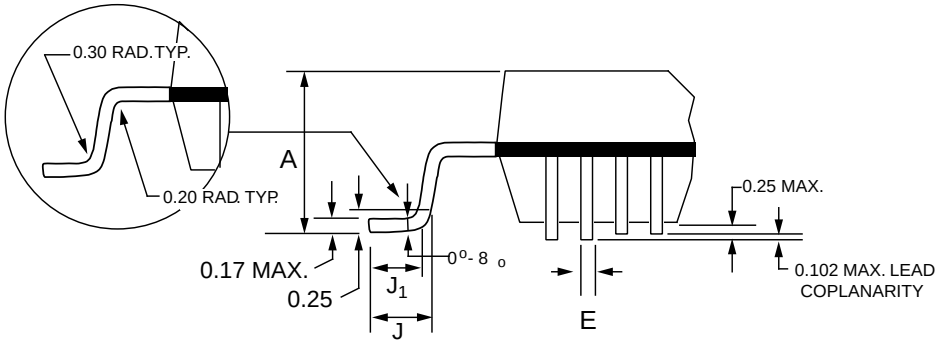
Table 12. Pin Identification for 44-Pin PQFP (QZ) (continued)

Pin Number	Signal	I/O	Type	Description
36	Y1A–	O	PECL	Channel 1A Output, Complement
37	Y1A+	O	PECL	Channel 1A Output, True
38	V_{CCP}1A		Pwr	Output Driver Power Supply for Channel 1A
39	TERM_ENABLE_A	I	Control	Input Termination Enable for A Switch. Normally LOW (V_{EE}). Connect to V_{CC} to enable internal 100Ω termination between AxA± inputs.
40	V_{CC}		Pwr	Power Supply, 3.3V
41	A1A+	I	PECL	Channel 1A Signal Input, True
42	A1A–	I	PECL	Channel 1A Signal Input, Complement
43	S1A	I	PECL, TTL	Channel 1A Input Selector
44	V_{CC}		Pwr	Power Supply, 3.3V



Item	mm	Tolerance
A	2.45	MAX
D	2.00	+0.10 / –0.05
E	0.35	±0.05
F	13.20	±0.25
G	10.00	±0.10
H	13.20	±0.25
I	10.00	±0.10
J	0.88	+0.15 / –0.10
J1	0.80	+0.15 / –0.10
K	0.80	BASIC
L	3.56	±0.50 DIA.





NOTES:
Drawing not to scale.
Heat spreader up.
All units in mm unless otherwise noted.

Figure 8. Package Drawing for 44-Pin PQFP (QZ)

Thermal Considerations

The VSC830 is package in a standard plastic quad flatpack (PQFP) with an embedded, but unexposed thermal slug. This package adheres to industry-standard EIAJ footprints for 10mm x 10mm body, 44-pin PQFP. The package construction is as shown in Figure 9. Table 13 provides the package thermal resistance from case-to-ambient under various airflow conditions, and the maximum ambient air temperature that can be applied to the device without an external heat sink. The thermal resistance value reflects all thermal paths including through the leads in an environment where the leads are exposed.

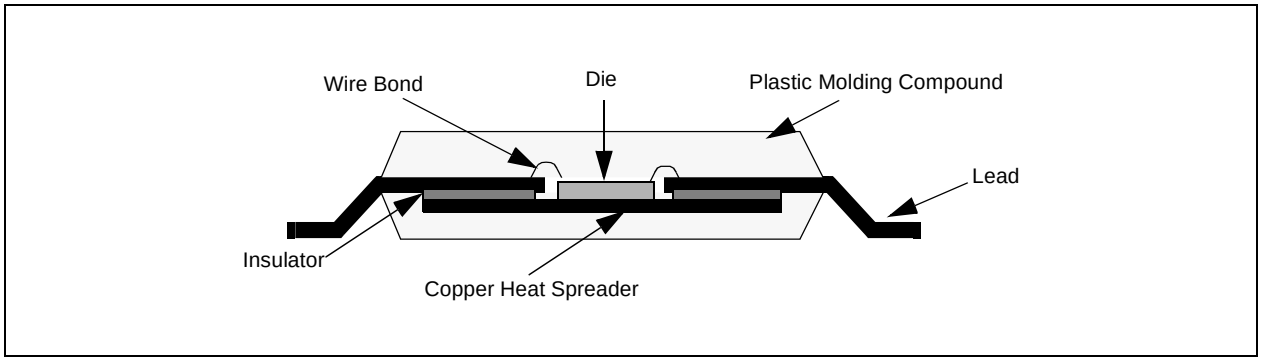


Figure 9. Package Cross Section

Table 13. Thermal Resistance

Symbol	Parameter	Value (°C/W)	$T_{A(MAX)}$ (°C)
θ_{JC}	Thermal resistance from junction-to-case	4.6	
θ_{CA}	Thermal resistance from case-to-ambient with no airflow, including conduction through the leads.	28.4	50.9
θ_{CA100}	Thermal resistance from case-to-ambient with 100 LFPM airflow	22.7	57.8
θ_{CA200}	Thermal resistance from case-to-ambient with 200 LFPM airflow	19.9	61.1
θ_{CA400}	Thermal resistance from case-to-ambient with 400 LFPM airflow	16.2	65.6
θ_{CA600}	Thermal resistance from case-to-ambient with 600 LFPM airflow	13.9	68.3

NOTE: *Max ambient temperature = max case temperature - (max power dissipation • $\theta_{CAAIRFLOW}$).*

ORDERING INFORMATION

VSC830 2.7Gb/s Asynchronous Dual 2x2 Crosspoint Switch

Part Number	Description
VSC830QZ	44-Pin PQFP, 10mm x 10mm x 2mm Body Temperature Range: 0°C ambient to +85°C case
VSC830QZ-01	44-Pin PQFP, 10mm x 10mm x 2mm Body Temperature Range: –40°C ambient to +85°C case

CORPORATE HEADQUARTERS
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VITESSE

VSC830
Data Sheet

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FEATURES

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- 2.7Gb/s NRZ Data Bandwidth, 2.7GHz Signal Bandwidth
- PECL/TTL-Compatible Control Inputs
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- Single 3.3V Supply, 1W Typical Dissipation
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- Compact 44-Pin PQFP, 10mm x 10mm Package

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The crosspoint function is based on a multiplexer tree architecture. Each 2x2 switch can be considered as a pair of 2:1 multiplexers that share the same inputs. The signal path through each switch is fully differential and delay matched. The signal path is unregistered, so there are no restrictions on the phase, frequency, or signal pattern at each input. Unused outputs can be independently powered off, thereby eliminating power on unused sections (see "Termination Schemes" on page 5). The switch control inputs can be configured to be compatible with PECL or TTL levels. The high-speed input and output levels are nominally PECL compatible and capable of interfacing with a wide range of termination schemes.

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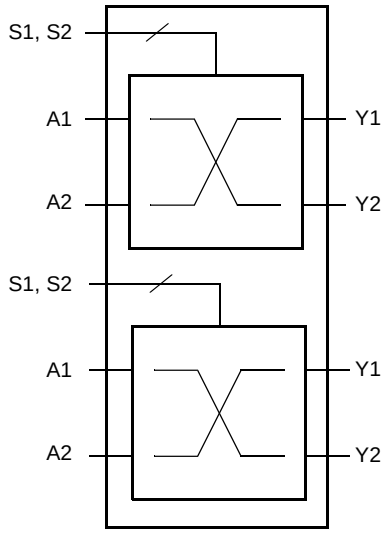
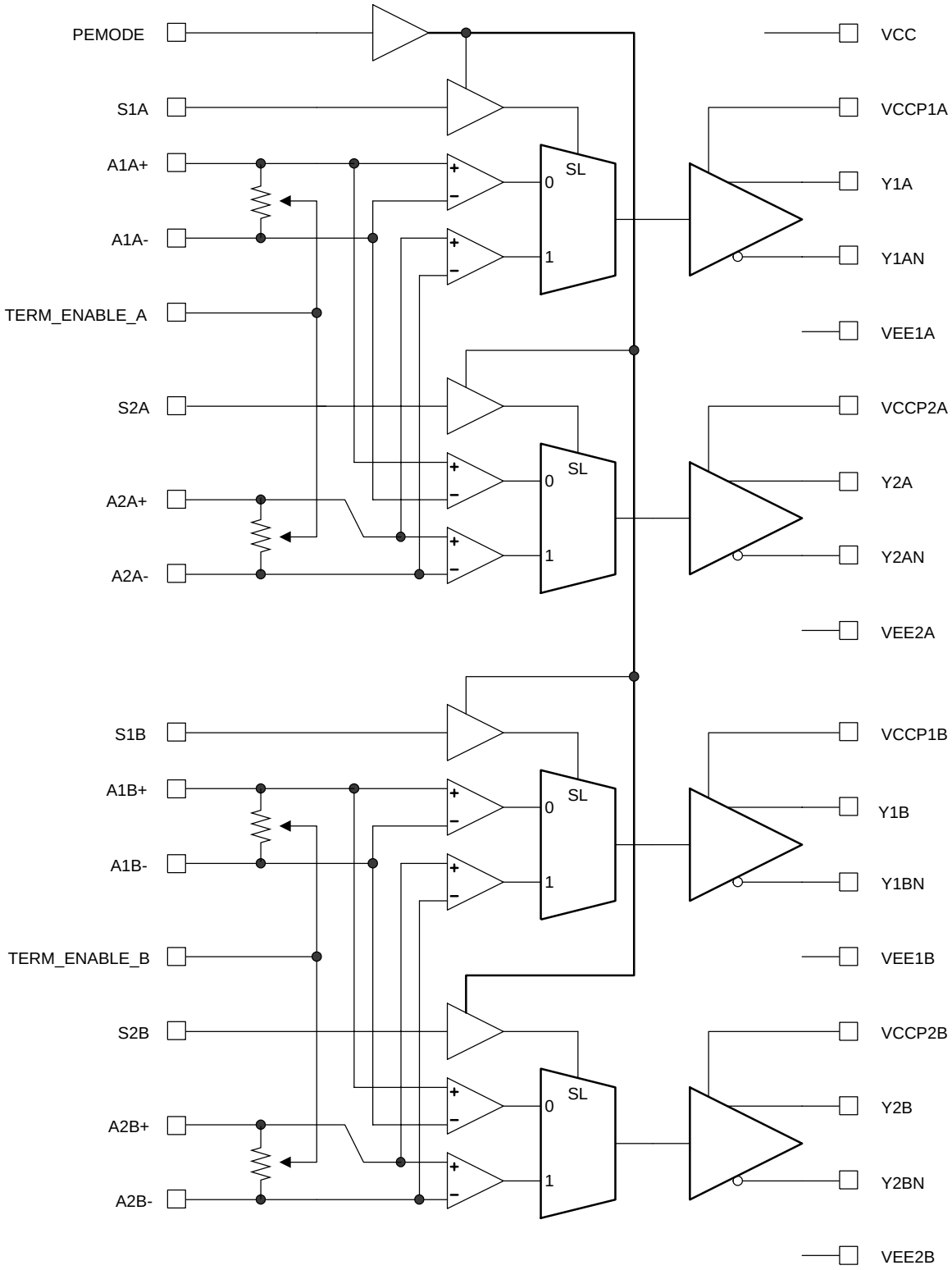


VSC830 Functional Block Diagram



FUNCTIONAL DESCRIPTION

Select

As shown in Figure 1, each output can be treated as a 2:1 multiplexer, with the A1 and A2 inputs common to both multiplexers. The select input S1 independently controls the state of the multiplexer that drives output Y1, and select input S2 independently controls the output of Y2. Table 1 specifies the function of the select inputs.

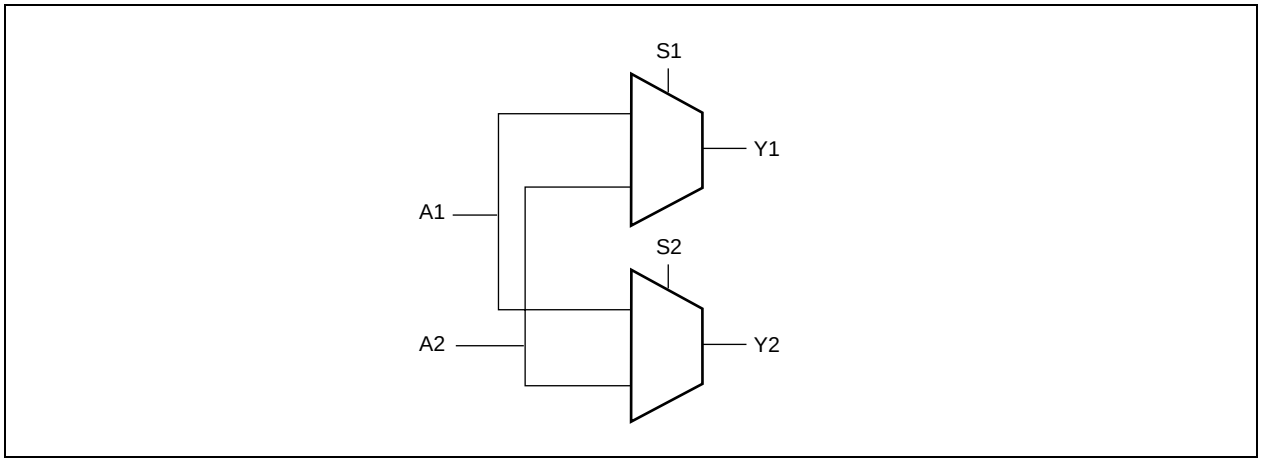


Figure 1. Select Functional Block Diagram

Table 1. Select Function

S1	S2	Y1	Y2
0	0	A1	A1
1	0	A2	A1
0	1	A1	A2
1	1	A2	A2

MODE

The interface level of the select pins, S1 and S2, can be programmed to either TTL or PECL levels by shorting the MODE pin to either V_{CC} or V_{EE}. Note that the MODE pin must be tied to either V_{CC} or V_{EE}. The function of MODE is specified in Table 2.

Table 2. MODE Function

MODE	S1, S2
V_{EE}	TTL
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Power-Down

Power to each output stage is provided through V_{CC}, V_{CCP}, and V_{EE}. V_{CC} is common to all outputs. To power off unused outputs, tie the respective V_{EE} and V_{CCP} pin to V_{CC}, as shown in Figure 2. Minimum power configuration requires output channel 1A active, so power must be applied to V_{CCP}1A and V_{EE}1A at all times.

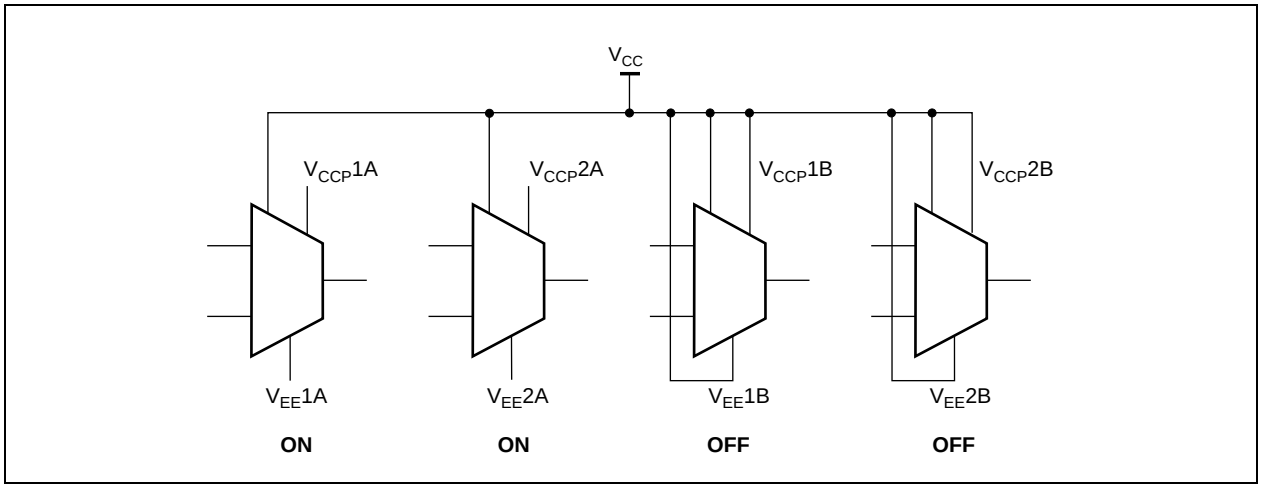


Figure 2. Power-Down Mode Example

Programmable Input Termination

Across each differential input (from the + input to the - input) of the VSC830 is a switched 100Ω termination resistor. Using the TERM_ENABLE pin, the termination can be optionally disabled. To enable the input termination, connect the respective TERM_ENABLE pin to V_{CC}. To disable the internal termination, connect TERM_ENABLE to V_{EE}. If unconnected, the TERM_ENABLE pin will self-bias to V_{EE} and disable the internal termination. Independent termination controls are provided for the A and B switches.

Termination Schemes

Signal Terminations

The high-speed inputs (A1A±, A1B±, A2A± and A2B±) on the VSC830 are internally terminated with a programmable 100Ω termination between the true and complement input. The input termination can be disabled by connecting the TERM_ENABLE pin to VEE. High impedance internal biasing resistors provide the correct bias voltage at the inputs for AC-coupled applications as shown in Figure 3.

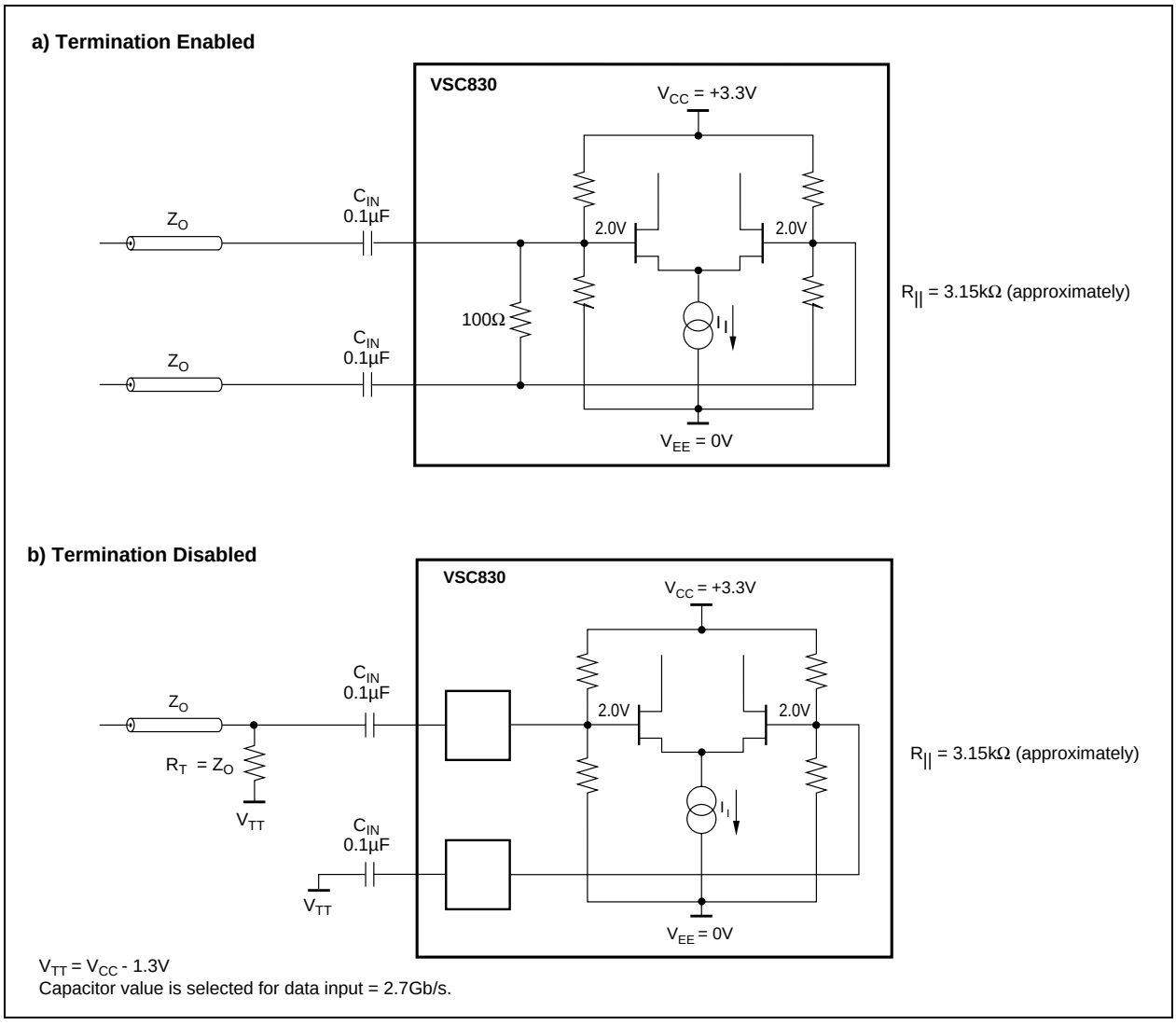


Figure 3. High-Speed Input Termination

The high-speed outputs (Y1A±, Y1B±, Y2A± and Y2B±) each consist of a differential pair designed to drive a 50Ω transmission line. The transmission line should be terminated with a 100Ω resistor at the receiver of the downstream device between the true and complement outputs. No connection to a termination voltage is required. The output driver is source terminated to 50Ω on-chip, providing a snubbing of any reflections. Output power can be cut by tying V_{EE} to V_{CC}. In single-ended mode, the unused output must be terminated with 50Ω. Examples of output terminations are shown in Figure 4 on page 6.

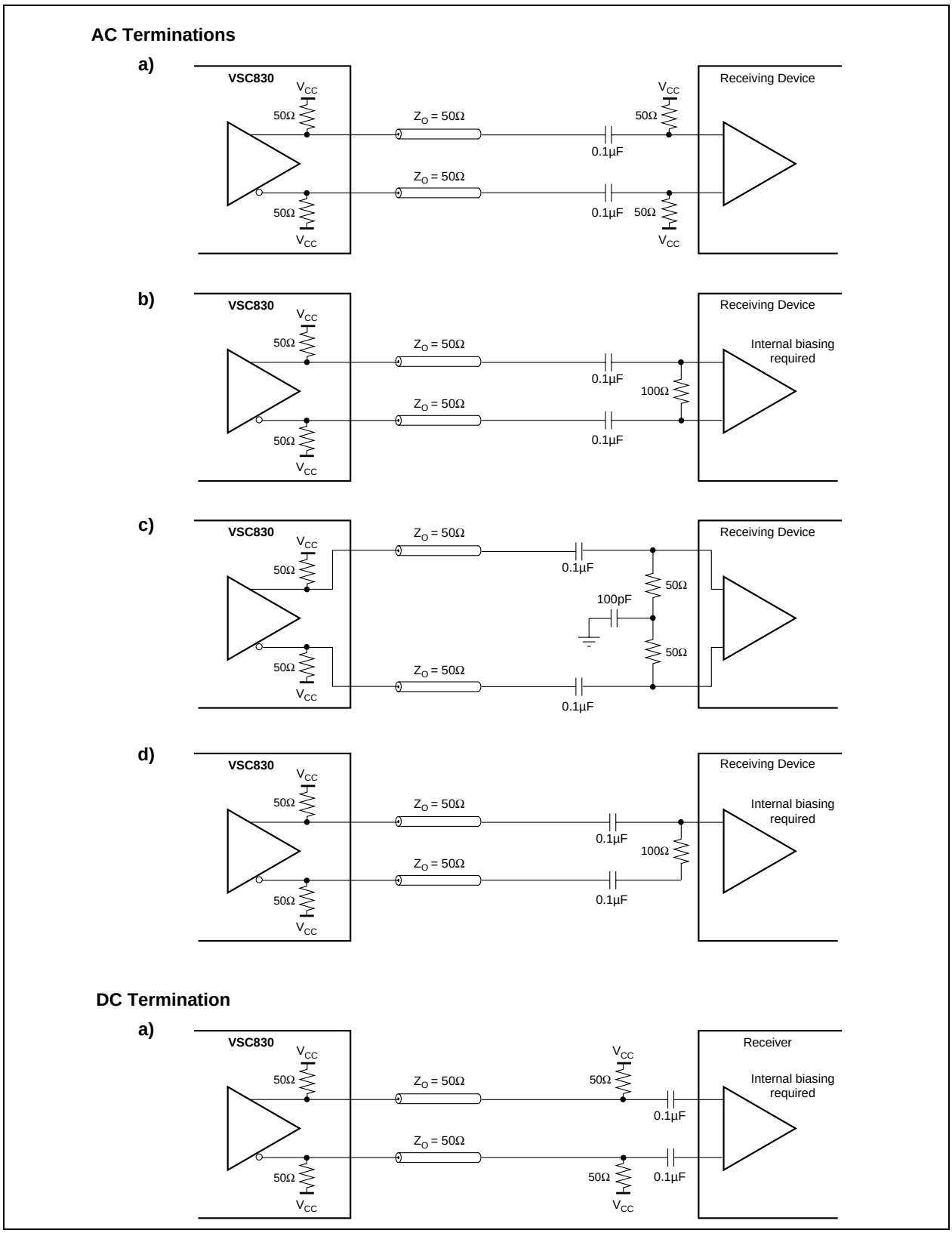


Figure 4. Termination Examples of High-Speed Outputs (Y1A±, Y1B±, Y2A±, Y2B±)

LAYOUT CONSIDERATIONS

Power Supply

The VSC830 is a single supply part, requiring only a 3.3V supply. The location and hook-up of the bypass capacitors is critical to providing the VSC830 with a clean 3.3V power supply. V_{CC} that are adjacent can share a 0.027µF capacitor connected to V_{EE}.

Normally the four channel specific V_{CC} pins (V_{CC}P1A, V_{CC}P1B, V_{CC}P2A, V_{CC}P2B) are connected to one common V_{CC} plane. In the same way the four channel specific V_{EE} pins are connected to the common V_{EE} plane. A suggested decoupling schematic for this configuration is shown in Figure 4d. However, a slightly higher signal integrity can be achieved if these pins are treated as different power supplies. In this case, V_{CC}P1A should then be decoupled to V_{EE}1A, etc, as shown in Figure 4b.

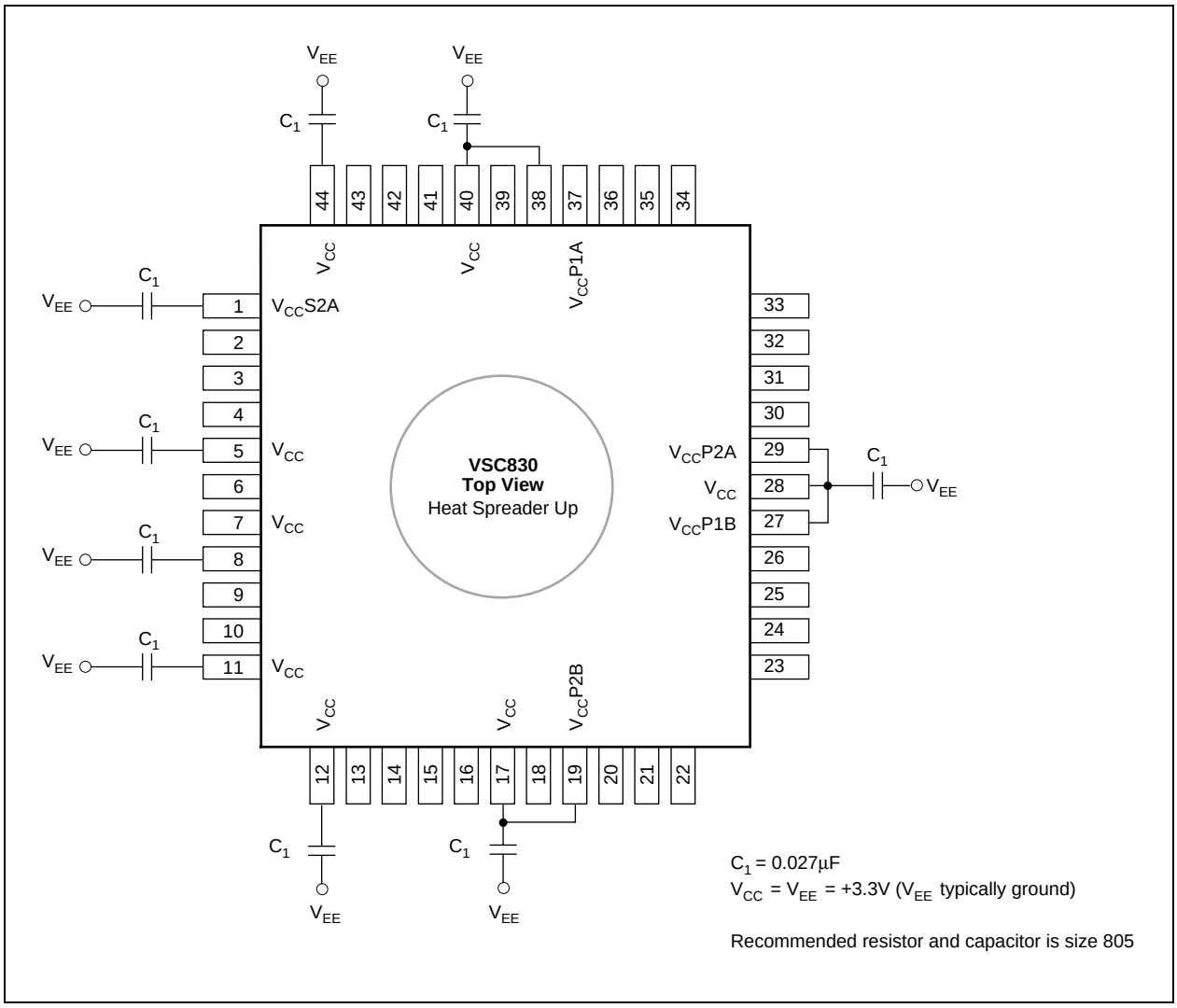


Figure 5. Decoupling Example: Common V_{CC} and V_{EE} Planes

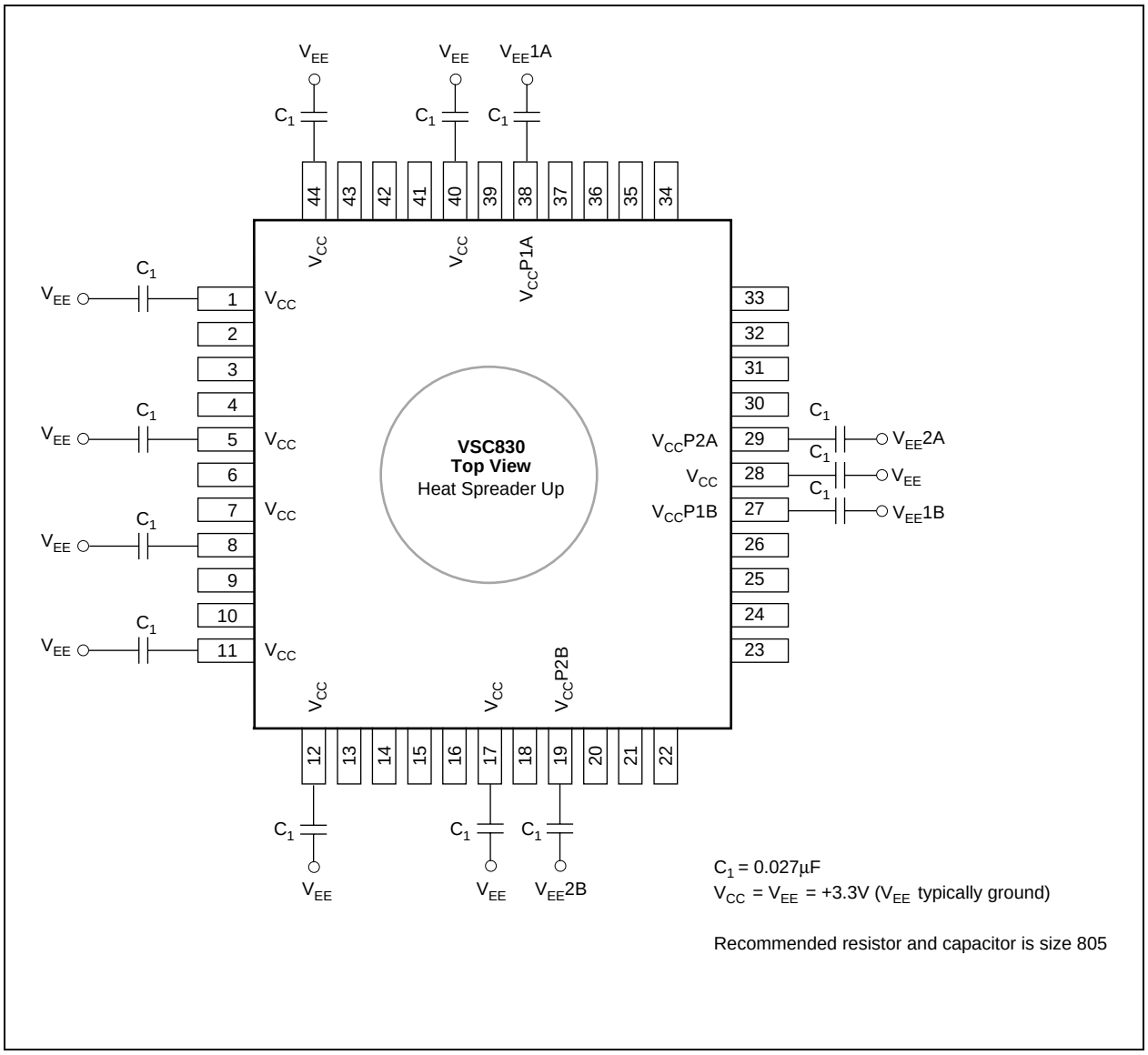


Figure 6. Decoupling Example: Separate V_{CC} and V_{EE} Planes

High-Speed Serial Inputs/Outputs

The high-speed serial signals contain digital data at fundamental frequencies up to 2.488GHz clock rate. Given that, in order to preserve the edges of such data sequences, it is necessary to have excellent frequency and phase response up to at least the 3rd harmonic, if not the 7th harmonic. Improved signal quality will result should the reader follow the general design rules below:

1. Keep traces as short as possible. Initial component placement should be very carefully considered.
2. The impedance of the traces must match that of the terminations, connectors and cable(s) in order to reduce reflections and impedance mismatches. Reflections can create standing waves that will increase the signal jitter.
3. Differential transmission line impedance must be maintained at 100Ω.
4. When routing differential pairs, keep the lengths identical for both traces. Differences in trace length translate directly into signal skew and can add to the signal jitter. Remember also that the differential impedance is affected by the separation between the traces.
5. Keep differential pair traces on the same side of the PCB to minimize impedance discontinuity, such as the one caused when using printed-circuit board vias.
6. Eliminate or reduce stubs.
7. Use rounded corners rather than 45° or 90° corners.
8. Keep signal traces far from other signals which might capacitively couple noise into the signals. This includes the other trace of a differential pair or the traces of the parallel PECL or TTL interface.
9. Do not cut up the power or ground planes in an effort to steer current paths. This usually produces more noise, not less.

SPECIFICATIONS

DC Characteristics

Over recommended operating cnditions unless stated otherwise.

Table 3. Power Supply

Symbol	Parameter	Min	Typ	Max	Units	Condition
I_{CC}	Total $V_{CC(P)}$ supply current			350	mA	
P_D	Power dissipation per output (Y1A±, Y2A±, Y1B±, Y2B±)			300	mW	
P_T	Total chip power (all outputs powered on)			1.2	W	

NOTE: *Specified with outputs terminated, 100Ω between true and complement, V_{CC} = 3.45V.*

Table 4. Select Input Levels, TTL

Symbol	Parameter	Min	Typ	Max	Units	Condition
V_{IH}	Input HIGH voltage	2.0			V	
V_{IL}	Input LOW voltage			0.8	V	
I_{IH}	Input HIGH current			500	µA	V_{IN} = 2.4V
I_{IL}	Input LOW current			–500	µA	V_{IN} = 0.5V

Table 5. Select Input Levels, PECL

Symbol	Parameter	Min	Typ	Max	Units	Condition
V_{IH}	Input HIGH voltage	V_{CC} – 1.0			V	
V_{IL}	Input LOW voltage			V_{CC} – 1.6	V	
I_{IH}	Input HIGH current			500	µA	V_{IN} = 2.5V
I_{IL}	Input LOW current			–500	µA	V_{IN} = 1.5V

Table 6. Control Inputs

Symbol	Parameter	Min	Typ	Max	Units	Condition
R_{PEMODE}	PEMODE pin impedance		3100		Ω	

Table 7. A Input Levels, Differential PECL

Symbol	Parameter	Min	Typ	Max	Units	Condition
V_{ID}	Input differential voltage(1)	200		1000	mV	
V_{ICM}	Input common-mode voltage	V_{CC} – 1.7		V_{CC} – 0.9	V	

1. *Peak-to-peak swing of each side of the differential input.*

Table 8. Y Output Levels, Differential PECL

Symbol	Parameter	Min	Typ	Max	Units	Condition
V_{OD1}	Output differential voltage (data)(1)	400	700	1000	mV	
V_{OD2}	Output differential voltage (clock)(2)	400	550	850	mV	
V_{OCM}	Output common-mode voltage	V_{CC} – 1.6		V_{CC} – 1.0	V	

1. *Peak-to-peak swing of each side of the differential output with 2^{23}-1 PRBS data.*
2. *Peak-to-peak swing of each side of the differential output using alternating 1, 0 pattern.*

AC Characteristics

Table 9. AC Timing

Symbol	Parameter	Min	Typ	Max	Units	Condition
F_{RATE}	Signal path data rate			2.7	Gb/s	
F_{BW}	Signal path bandwidth (-3dB)			2.7	GHz	
T_{SKW}	Channel-to-channel delay skew		50		ps	
T_{CON}	Switch configuration setup time(1)			1	ns	
t_R, t_F	High-speed output rise/fall times(2)			150	ps	20% to 80%
t_{Jp-p}	Signal path added jitter, peak-to-peak(1)			40	ps	

1. *Tested on a sample basis only with 2^{23}-1 PRBS data, input signal rise/fall time <150ps. Value stated in table is added to measurement system jitter.*
2. *Input signal rise/fall time <150ps, measured using alternating 1, 0 pattern.*

Table 10. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{CC}, V_{CCP}	Power supply voltage	3.135	3.3	3.465	V	
T	Operating temperature range(1) **VSC830** **VSC830-01**	 0 –40		 +85 +85	 °C °C	

1. *Lower limit of specification is ambient temperature and upper limit is case temperature.*

Table 11. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Condition
V_{CC}	Power supply voltage, potential to ground	–0.5	+4.0	V	
	DC input voltage (TTL, ECL inputs)	-0.5	V_{CC} +0.5	V	
	Output current		50	mA	
T_C	Case temperature under bias	–55	+125	°C	
T_S	Storage temperature	–65	+150	°C	
V_{ESD}	ESD (human body model)		1500	V	

Stresses listed under “Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliabiility of the device.

PACKAGE INFORMATION

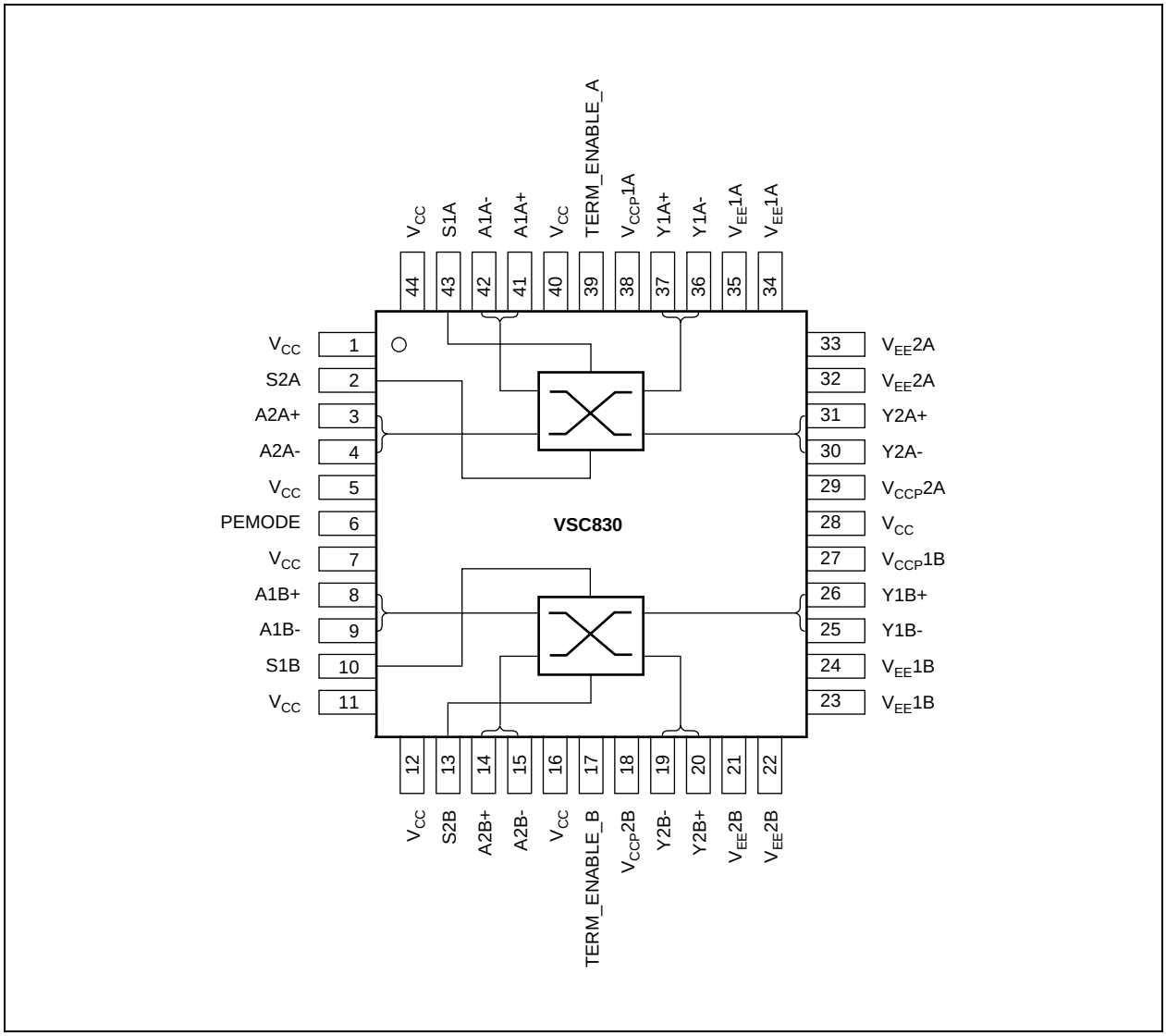


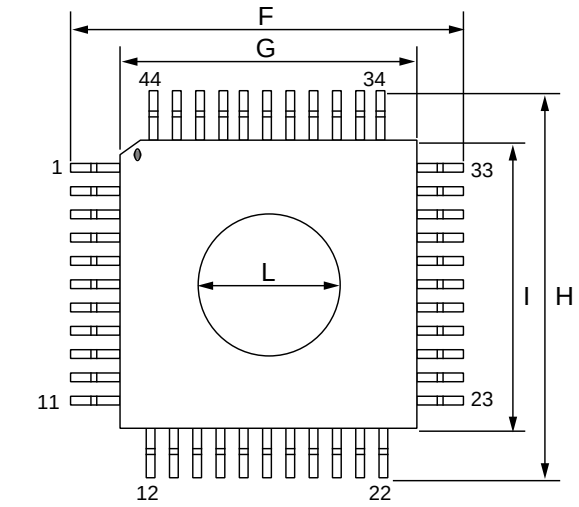
Figure 7. Pin DIagram for 44-Pin PQFP (QZ)

Table 12. Pin Identification for 44-Pin PQFP (QZ)

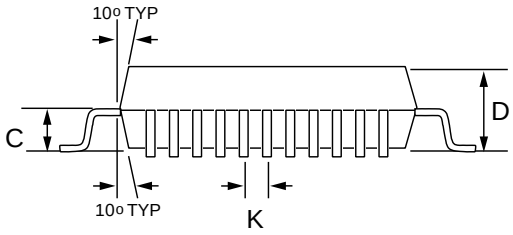
Pin Number	Signal	I/O	Type	Description
1	V_{CC}		Pwr	Power Supply, 3.3V
2	S2A	I	PECL, TTL	Channel 2A Input Selector
3	A2A+	I	PECL	Channel 2A Signal Input, True.
4	A2A–	I	PECL	Channel 2A Signal Input, Complement
5	V_{CC}		Pwr	Power Supply, 3.3V
6	PEMODE		Control	
7	V_{CC}		Pwr	Power Supply, 3.3V
8	A1B+	I	PECL	Channel 1B Signal Input, True.
9	A1B–	I	PECL	Channel 1B Signal Input, Complement.
10	S1B	I	PECL, TTL	Channel 1B Input Selector
11	V_{CC}		Pwr	Power Supply, 3.3V
12	V_{CC}		Pwr	Power Supply, 3.3V
13	S2B	I	PECL, TTL	Channel 2B Input Selector
14	A2B+	I	PECL	Channel 2B Signal Input, True.
15	A2B–	I	PECL	Channel 2B Signal Input, Complement.
16	V_{CC}		Pwr	Power Supply, 3.3V
17	TERM_ENABLE_B	I	Control	Input Termination Enable for B Switch. Normally LOW (V_{EE}). Connect to V_{CC} to enable internal 100Ω termination between AxA± inputs.
18	V_{CCP}2B		Pwr	Output driver power supply for channel 2B.
19	Y2B–	O	PECL	Channel 2B Output, Complement
20	Y2B+	O	PECL	Channel 2B Output, True
21	V_{EE}2B		Pwr	Ground for Channel 2B
22	V_{EE}2B		Pwr	Ground for Channel 2B
23	V_{EE}1B		Pwr	Ground for Channel 1B
24	V_{EE}1B		Pwr	Ground for Channel 1B
25	Y1B–	O	PECL	Channel 1B Output, Complement
26	Y1B+	O	PECL	Channel 1B Output, True
27	V_{CCP}1B		Pwr	Output Driver Power Supply for Channel 1B
28	V_{CC}		Pwr	Power Supply, 3.3V
29	V_{CCP}2A		Pwr	Output Driver Power Supply for Channel 2A
30	Y2A–	O	PECL	Channel 2A Output, Complement
31	Y2A+	O	PECL	Channel 2A Output, True
32	V_{EE}2A		Pwr	Ground for Channel 2A
33	V_{EE}2A		Pwr	Ground for Channel 2A
34	V_{EE}1A		Pwr	Ground for Channel 1A
35	V_{EE}1A		Pwr	Ground for Channel 1A

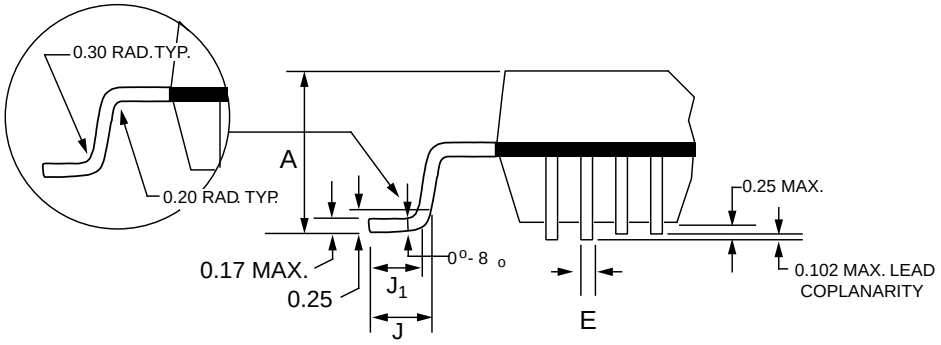
Table 12. Pin Identification for 44-Pin PQFP (QZ) (continued)

Pin Number	Signal	I/O	Type	Description
36	Y1A–	O	PECL	Channel 1A Output, Complement
37	Y1A+	O	PECL	Channel 1A Output, True
38	V_{CCP}1A		Pwr	Output Driver Power Supply for Channel 1A
39	TERM_ENABLE_A	I	Control	Input Termination Enable for A Switch. Normally LOW (V_{EE}). Connect to V_{CC} to enable internal 100Ω termination between AxA± inputs.
40	V_{CC}		Pwr	Power Supply, 3.3V
41	A1A+	I	PECL	Channel 1A Signal Input, True
42	A1A–	I	PECL	Channel 1A Signal Input, Complement
43	S1A	I	PECL, TTL	Channel 1A Input Selector
44	V_{CC}		Pwr	Power Supply, 3.3V



Item	mm	Tolerance
A	2.45	MAX
D	2.00	+0.10 / –0.05
E	0.35	±0.05
F	13.20	±0.25
G	10.00	±0.10
H	13.20	±0.25
I	10.00	±0.10
J	0.88	+0.15 / –0.10
J1	0.80	+0.15 / –0.10
K	0.80	BASIC
L	3.56	±0.50 DIA.





NOTES:
Drawing not to scale.
Heat spreader up.
All units in mm unless otherwise noted.

Figure 8. Package Drawing for 44-Pin PQFP (QZ)

Thermal Considerations

The VSC830 is package in a standard plastic quad flatpack (PQFP) with an embedded, but unexposed thermal slug. This package adheres to industry-standard EIAJ footprints for 10mm x 10mm body, 44-pin PQFP. The package construction is as shown in Figure 9. Table 13 provides the package thermal resistance from case-to-ambient under various airflow conditions, and the maximum ambient air temperature that can be applied to the device without an external heat sink. The thermal resistance value reflects all thermal paths including through the leads in an environment where the leads are exposed.

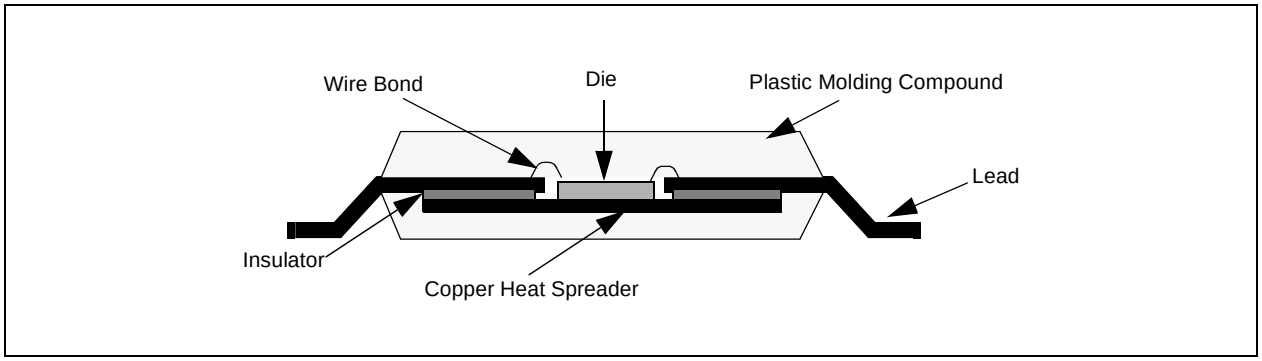


Figure 9. Package Cross Section

Table 13. Thermal Resistance

Symbol	Parameter	Value (°C/W)	$T_{A(MAX)}$ (°C)
θ_{JC}	Thermal resistance from junction-to-case	4.6	
θ_{CA}	Thermal resistance from case-to-ambient with no airflow, including conduction through the leads.	28.4	50.9
θ_{CA100}	Thermal resistance from case-to-ambient with 100 LFPM airflow	22.7	57.8
θ_{CA200}	Thermal resistance from case-to-ambient with 200 LFPM airflow	19.9	61.1
θ_{CA400}	Thermal resistance from case-to-ambient with 400 LFPM airflow	16.2	65.6
θ_{CA600}	Thermal resistance from case-to-ambient with 600 LFPM airflow	13.9	68.3

NOTE: *Max ambient temperature = max case temperature - (max power dissipation • $\theta_{CAAIRFLOW}$).*

ORDERING INFORMATION

VSC830 2.7Gb/s Asynchronous Dual 2x2 Crosspoint Switch

Part Number	Description
VSC830QZ	44-Pin PQFP, 10mm x 10mm x 2mm Body Temperature Range: 0°C ambient to +85°C case
VSC830QZ-01	44-Pin PQFP, 10mm x 10mm x 2mm Body Temperature Range: –40°C ambient to +85°C case

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