MICRON TECHNOLOGY, INC.

MT18LD(T)472(X)(S)
4 MEG x 72 DRAM MODULE

DRAM MODULE

4 MEG x 72

32 MEGABYTE, ECC, 3.3V, OPTIONAL SELF REFRESH, FAST PAGE OR EDO PAGE MODE

FEATURES

- JEDEC- and industry-standard ECC pinout in a 168-pin, dual-in-line memory module (DIMM)
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Low power, 18mW standby; 3,240mW active, typical
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN; optional Extended and SELF REFRESH
- All inputs are buffered except $\overline{RAS}$
- 2,048-cycle refresh distributed across 32ms or 2,048-cycle Extended Refresh distributed across 128ms
- FAST PAGE MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- 5V tolerant I/Os (5.5V maximum V_{IH} level)

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
- Components
  - SOJ — D
  - TSOP — DT
- Packages
  - 168-pin DIMM (gold) — G
- Access Cycle
  - FAST PAGE MODE — Blank
  - EDO PAGE MODE — X
- Refresh
  - Standard/32ms — Blank
  - SELF REFRESH/128ms — S

KEY TIMING PARAMETERS

EDO option

SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{CAS}
-6	110ns	60ns	25ns	35ns	20ns	10ns
-7	130ns	70ns	30ns	40ns	25ns	12ns

FPM option

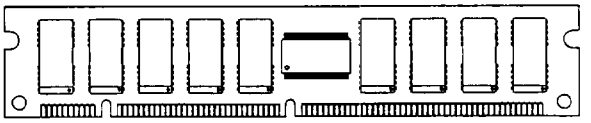
SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{RP}
-6	110ns	60ns	35ns	35ns	20ns	40ns
-7	130ns	70ns	40ns	40ns	25ns	50ns

PIN ASSIGNMENT (Front View)

168-Pin DIMM

(DE-15) SOJ version

(DE-16) TSOP version



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	$\overline{OE2}$	86	DQ36	128	RFU
3	DQ1	45	$\overline{RAS2}$	87	DQ37	129	NC
4	DQ2	46	$\overline{CAS4}$	88	DQ38	130	NC
5	DQ3	47	RFU	89	DQ39	131	RFU
6	Vcc	48	$\overline{WE2}$	90	Vcc	132	$\overline{PDE}$
7	DQ4	49	Vcc	91	DQ40	133	Vcc
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	Vcc	101	DQ49	143	Vcc
18	Vcc	60	DQ24	102	Vcc	144	DQ60
19	DQ14	61	RFU	103	DQ50	145	RFU
20	DQ15	62	RFU	104	DQ51	146	RFU
21	DQ16	63	RFU	105	DQ52	147	RFU
22	DQ17	64	RFU	106	DQ53	148	RFU
23	Vss	65	DQ25	107	Vss	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	Vcc	68	Vss	110	Vcc	152	Vss
27	$\overline{WE0}$	69	DQ28	111	RFU	153	DQ64
28	$\overline{CAS0}$	70	DQ29	112	NC	154	DQ65
29	RFU	71	DQ30	113	RFU	155	DQ66
30	$\overline{RAS0}$	72	DQ31	114	NC	156	DQ67
31	$\overline{OE0}$	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ32	116	Vss	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	RFU	83	ID0	125	RFU	167	ID1
42	RFU	84	Vcc	126	B0	168	Vcc

MTCTS040

VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT18LDT472G-xx	4 Meg x 72 ECC, FPM, TSOP
MT18LDT472G-xx X	4 Meg x 72 ECC, EDO, TSOP
MT18LDT472G-xx S	4 Meg x 72 ECC, FPM, TSOP, S*
MT18LDT472G-xx XS	4 Meg x 72 ECC, EDO, TSOP, S*
MT18LD472G-xx	4 Meg x 72 ECC, FPM, SOJ
MT18LD472G-xx X	4 Meg x 72 ECC, EDO, SOJ
MT18LD472G-xx S	4 Meg x 72 ECC, FPM, SOJ, S*
MT18LD472G-xx XS	4 Meg x 72 ECC, EDO, SOJ, S*

S = SELF REFRESH

GENERAL DESCRIPTION

The MT18LD(T)472(X)(S) is a randomly accessed 32MB solid-state memory organized in a x72 configuration. It is specially processed to operate from 3.0V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0/B0-A10) at a time. Two copies of address 0 (A0 and B0) are defined to allow maximum performance for 4-byte applications which interleave between two 4-byte banks. A0 is common to the DRAMs used for DQ0-DQ35, while B0 is common to the DRAMs used for DQ36-DQ71. $\overline{RAS}$ is used to latch the first 11 bits and $\overline{CAS}$ the latter 11 bits.

READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. EARLY WRITE occurs when $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, and the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after $\overline{CAS}$ goes back HIGH. EDO provides for $\overline{CAS}$ precharge time (^tCP) to occur without the output data going invalid. This elimination of $\overline{CAS}$ output control provides for pipeline READs.

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{CAS}$. EDO-PAGE-MODE DRAMs operate similar to FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after $\overline{CAS}$ goes HIGH during READs, provided $\overline{RAS}$ and $\overline{OE}$ are held LOW. If $\overline{OE}$ is pulsed while $\overline{RAS}$ and $\overline{CAS}$ are LOW, data will toggle from valid data to High-Z and back to the same valid data. If $\overline{OE}$ is toggled or pulsed after $\overline{CAS}$ goes HIGH while $\overline{RAS}$ remains LOW, data will transition to and remain High-Z.

If the DQ outputs are wire OR'd, $\overline{OE}$ must be used to disable idle banks of DRAMs. Alternatively, pulsing $\overline{WE}$ to the idle banks during $\overline{CAS}$ HIGH time will also High-Z the outputs. Independent of $\overline{OE}$ control, the outputs will disable after ^tOFF, which is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last (reference the MT4LC4M4E8(S) DRAM data sheet for additional information on EDO functionality).

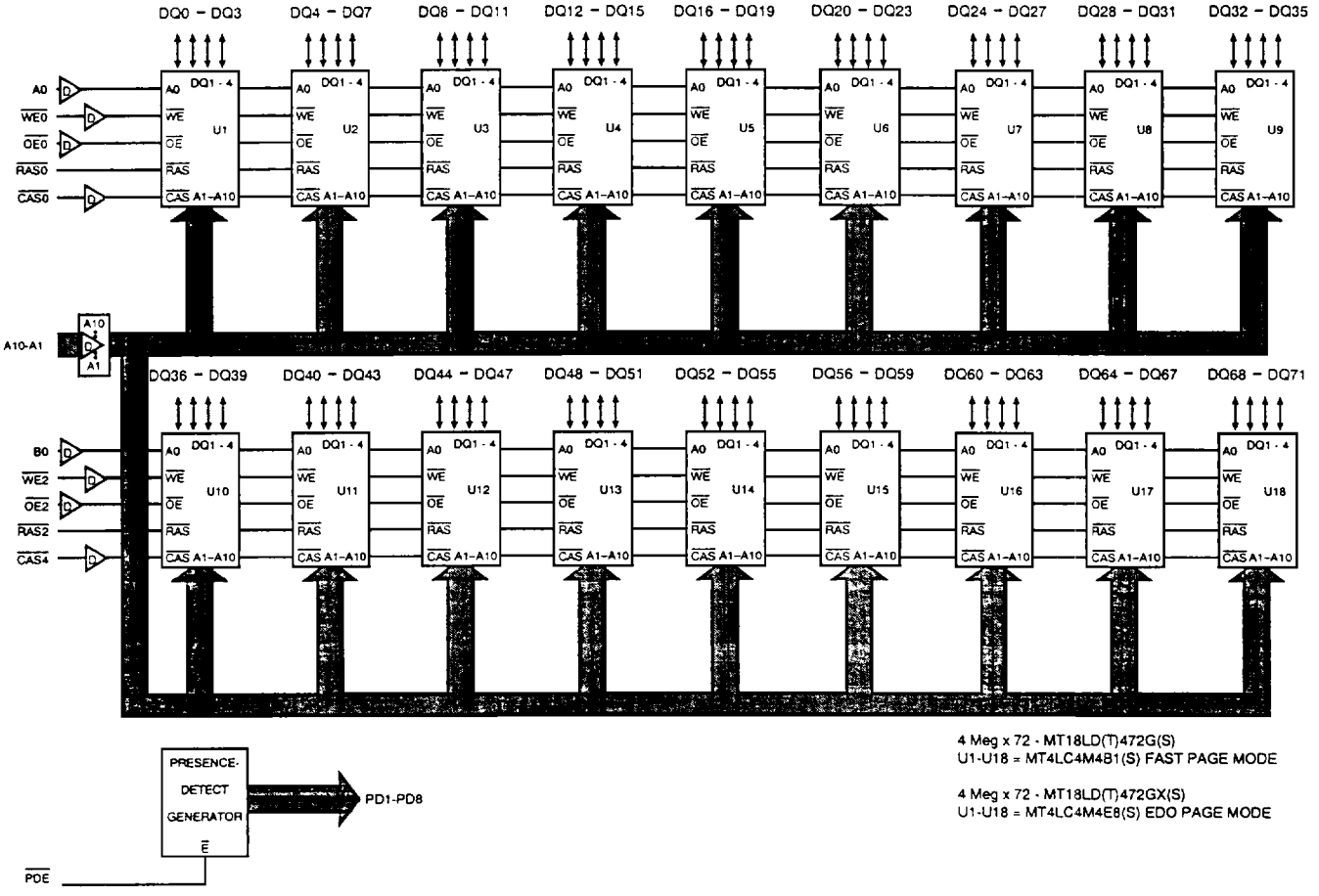
REFRESH

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Correct memory cell data is preserved by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR or HIDDEN) so that all combinations of $\overline{RAS}$ addresses (A0/B0-A9/A10) are executed at least every ^tREF, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

An additional SELF REFRESH mode is also available. The "S" version allows the user the option of a fully static low power data retention mode, or a dynamic refresh mode at the extended refresh period. The module's SELF REFRESH mode is initiated by executing a CBR REFRESH cycle and holding $\overline{RAS}$ LOW for the specified ^tRASS. Additionally, the "S" version allows for an extended refresh rate of 62.5µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or extended refresh mode.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for the time minimum of an operation cycle, typically ^tRPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR REFRESH sequence, a burst refresh is not required upon exiting SELF REFRESH mode. However, if the DRAM controller utilizes $\overline{RAS}$ ONLY or burst refresh sequence, all 2,048 rows must be refreshed within 300µs prior to the resumption of normal operation.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. All inputs with the exception of $\overline{RAS}$ are redriven.
2. D = line buffers.

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	$\overline{RAS0}$, $\overline{RAS2}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to clock-in the 11 row-address bits. Two $\overline{RAS}$ inputs allow for one x72 bank or two x36 banks.
28, 46	$\overline{CAS0}$, $\overline{CAS4}$	Buffered Input	Column-Address Strobe: $\overline{CAS}$ is used to clock-in the 11 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles.
27, 48	$\overline{WE0}$, $\overline{WE2}$	Buffered Input	Write Enable: $\overline{WE}$ is the READ/WRITE control for the DQ pins. $\overline{WE0}$ controls DQ0-DQ35. $\overline{WE2}$ controls DQ36-DQ71. If $\overline{WE}$ is LOW prior to $\overline{CAS}$ going LOW, the access is an EARLY WRITE cycle. If $\overline{WE}$ is HIGH while $\overline{CAS}$ is LOW, the access is a READ cycle, provided $\overline{OE}$ is also LOW. If WE goes LOW after $\overline{CAS}$ goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	$\overline{OE0}$, $\overline{OE2}$	Buffered Input	Output Enable: $\overline{OE}$ is the input/output control for the DQ pins. $\overline{OE0}$ controls DQ0-DQ35. $\overline{OE2}$ controls DQ36-DQ71. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-121, 126	A0-A10, B0	Buffered Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$. A0 is common to the DRAMs used for DQ0-DQ35 while B0 is common to the DRAMs used for DQ36-DQ71
2-5, 7-11, 13-17, 19-22, 52-53, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-106, 136-137, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ71	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ71 act as inputs to the addressed DRAM location. For READ access cycles, DQ0-DQ71 act as outputs for the addressed DRAM location.
79-82, 163-166	PD1-PD8	Buffered Output	Presence-Detect: These pins are read by the host system and tell the system the DIMM's personality. They will be either driven to V_{OH} (1) or they will be driven to V_{OL} (0).
29, 41-42, 47, 61-64, 111, 113, 115, 125, 128, 131, 145-148	RFU	—	RFU: These pins should be left unconnected (reserved for future use).
6, 18, 26, 40, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	Vcc	Supply	Power Supply: +3.3V ± 0.3V

PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1, 12, 23, 32, 43, 54, 68, 78, 85, 96, 107, 116, 127, 138, 152, 162	Vss	Supply	Ground
83, 167	ID0, ID1	Output	ID bits: ID0 = DIMM type. ID1 = Refresh Mode. These pins will be either left floating (NC) or they will be grounded (Vss).
132	$\overline{PDE}$	Input	Presence-Detect Enable: $\overline{PDE}$ is the READ control for the buffered presence-detect pins.
24-25, 39, 50-51, 108-109, 112, 114, 122-123, 129, 130, 134-135, 150, 161	NC	—	No connect

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	$\overline{PDE}$	ADDRESSES t_R	ADDRESSES t_C	DATA-IN/OUT DQ0-71
Standby		H	H→X	X	X	X	X	X	High-Z
READ		L	L	H	L	X	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	X	ROW	COL	Data-Out, Data-In
EDO/FAST-PAGE-	1st Cycle	L	H→L	H	L	X	ROW	COL	Data-Out
MODE READ	2nd Cycle	L	H→L	H	L	X	n/a	COL	Data-Out
EDO/FAST-PAGE-	1st Cycle	L	H→L	L	X	X	ROW	COL	Data-In
MODE EARLY-WRITE	2nd Cycle	L	H→L	L	X	X	n/a	COL	Data-In
EDO/FAST-PAGE-	1st Cycle	L	H→L	H→L	L→H	X	ROW	COL	Data-Out, Data-In
MODE READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	X	n/a	COL	Data-Out, Data-In
$\overline{RAS}$-ONLY REFRESH		H	X	X	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L	X	ROW	COL	Data-Out
REFRESH	WRITE	L→H→L	L	L	X	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	X	High-Z
SELF REFRESH (S version)		H→L	L	H	X	X	X	X	High-Z
READ PRESENCE-DETECTS		X	X	X	X	L	X	X	Not Affected

PRESENCE-DETECT TRUTH TABLE

CHARACTERISTICS					PRESENCE-DETECT PIN (PDx)							
Module Density	Module Organization	Row/Column Addresses	ID0	ID1	1	2	3	4	5	6	7	8
0MB	No module installed	X			1	1	1	1				
2MB	256K x 64/72	9/9			0	0	0	0				
4MB	512K x 64/72	9/9			1	0	0	0				
4MB	512K x 64/72/80	10/9			0	1	0	0				
8MB	1 Meg x 64/72/80	10/9			1	1	0	0				
8MB	1 Meg x 64/72/80	10/10			0	0	1	0				
16MB	2 Meg x 64/72/80	10/10			1	0	1	0				
16MB	2 Meg x 64/72/80	11/10			1	0	0	1				
32MB	4 Meg x 64/72/80	11/10			0	1	0	1				
• 32MB	4 Meg x 64/72/80	12*/11*			1	1	0	1				
64MB	8 Meg x 64/72/80	12/10			0	0	1	0				
Page Mode		Fast Page Mode							0			
		EDO Page Mode							1			
Access Timing		80ns								1	0	
		70ns								0	1	
		60ns								1	1	
		50ns								0	0	
Refresh Control		Standard		Vss								
		Self		NC								
Data Width, Parity		x64, No Parity	Vss									1
		x72, Parity	NC									1
		x72, ECC	Vss									0
		x80, ECC	NC									0

NOTE: Vss = ground; 0 = V_{OL}; 1 = V_{OH}.

* This addressing includes a redundant address to allow mixing of 12/10 and 11/11 DRAMs with the same presence-detect setting. The MT18_D(T)472 uses 11/11 DRAMs.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (Vcc = +3.3V ±0.3V)

PARAMETER/CONDITION		SYM	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		VIH	2.0	5.5	V	
Input Low (Logic 0) Voltage, all inputs		VIL	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ 5.5V (All other pins not under test = 0V) for each package input	$\overline{CAS0}$, $\overline{CAS4}$ A0-A10, B0, $\overline{PDE}$ $\overline{WE0}$, 2, $\overline{OE0}$, 2	II1	-2	2	µA	
	$\overline{RAS0}$, $\overline{RAS2}$	II2	-18	18	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V) for each package input	DQ0-DQ71, PD1-PD8	IOZ	-10	10	µA	
OUTPUT LEVELS Output High Voltage (IOUT = -2mA)		VOH	2.4		V	
Output Low Voltage (IOUT = 2mA)		VOL		0.4	V	

			MAX			
PARAMETER/CONDITION	SYMBOL	SIZE	-6	-7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	ICC1	32MB	32	32	mA	28
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	ICC2	32MB	9	9	mA	28
	ICC2 (S only)	32MB	2.7	2.7		
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: tRC = tRC [MIN])	ICC3	32MB	2,160	1,980	mA	3, 4, 28,32
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, Address Cycling: tPC = tPC [MIN])	ICC4	32MB	1,620	1,440	mA	3, 4, 28,32
OPERATING CURRENT: EDO PAGE MODE (X version only) Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, Address Cycling: tPC = tPC [MIN])	ICC5 (X only)	32MB	1,980	1,800	mA	3, 4, 28,32
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = VIH: tRC = tRC [MIN])	ICC6	32MB	2,160	1,980	mA	3, 28, 32
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: tRC = tRC [MIN])	ICC7	32MB	2,160	1,980	mA	3, 5, 28
REFRESH CURRENT: Extended (S version only) Average power supply current; $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = tRAS (MIN); $\overline{WE}$= Vcc -0.2V; A0/B0-A10, $\overline{OE}$ and DIN = Vcc -0.2V or 0.2V (DIN may be left open); tRC = 62.5µs	ICC8 (S only)	32MB	5.4	5.4	mA	3, 5, 31
REFRESH CURRENT: SELF (S version only) Average power supply current; CBR cycling with $\overline{RAS}$ ≥ tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc -0.2V; A0/B0-A10, $\overline{OE}$ and DIN = Vcc -0.2V or 0.2V (DIN may be left open)	ICC9 (S only)	32MB	5.4	5.4	mA	5, 36

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Pin Relative to Vss ..... -1V to +4.6V
Voltage on Inputs or I/O Pins
Relative to Vss ..... -1V to +5.5V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 18W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A10, B0, $\overline{PDE}$	C_{I1}		9	pF	2
Input Capacitance: $\overline{WE0}$, $\overline{WE2}$, $\overline{OE0}$, $\overline{OE2}$, $\overline{CAS0}$, $\overline{CAS4}$	C_{I2}		9	pF	2
Input Capacitance: $\overline{RAS0}$, $\overline{RAS2}$	C_{I3}		70	pF	2
Input/Output Capacitance: DQ0-DQ71	C_{IO}		10	pF	2
Output Capacitance: PD1-PD8	C_O		9	pF	2

FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		35		40	ns	25
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	48		53		ns	24
Column-address setup time	^tASC	2		2		ns	23
Row-address setup time	^tASR	5		5		ns	25
Column-address to $\overline{WE}$ delay time	^tAWD	57		67		ns	23, 30
Access time from $\overline{CAS}$	^tCAC		20		25	ns	15, 25
Column-address hold time	^tCAH	15		20		ns	25
$\overline{CAS}$ pulse width	^tCAS	15	10,000	20	10,000	ns	
$\overline{RAS}$ LOW to "don't care" during SELF REFRESH	^tCHD	15		15		ns	36
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	8		8		ns	5, 24
$\overline{CAS}$ to output in Low-Z	^tCLZ	5		5		ns	23, 33
$\overline{CAS}$ precharge time	^tCP	10		10		ns	16
Access time from $\overline{CAS}$ precharge	^tCPA		40		45	ns	25
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	15		15		ns	25
$\overline{CAS}$ hold time	^tCSH	58		68		ns	24
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	12		12		ns	5, 23
$\overline{CAS}$ to $\overline{WE}$ delay time	^tCWD	42		47		ns	23, 30
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in hold time	^tDH	15		20		ns	25, 29
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	-2		-2		ns	24, 29
Output disable	^tOD		15		20	ns	
Output enable	^tOE		15		20	ns	
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^tOEH	13		18		ns	24
Output buffer turn-off delay	^tOFF	5	20	5	25	ns	20,27,38

FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	tORD	0		0		ns	20
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		ns	
$\overline{PDE}$ to valid presence-detect data	tPD		10		10	ns	35
$\overline{PDE}$ inactive to presence-detects inactive	tPDOFF	2		2		ns	34
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	87		97		ns	23
Access time from $\overline{RAS}$	tRAC		60		70	ns	14
$\overline{RAS}$ to column-address delay time	tRAD	13	25	13	30	ns	18, 26
Row-address hold time	tRAH	8		8		ns	24
Column-address to $\overline{RAS}$ lead time	tRAL	35		40		ns	25
$\overline{RAS}$ pulse width	tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH	tRASS	100		100		µs	36

EDO PAGE MODE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	tAA		35		40	ns	25
Column-address setup to $\overline{CAS}$ precharge during writes	tACH	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	tAR	43		53		ns	24
Column-address setup time	tASC	2		2		ns	23
Row-address setup time	tASR	5		5		ns	25
Column-address to $\overline{WE}$ delay time	tAWD	57		67		ns	23, 30
Access time from $\overline{CAS}$	tCAC		20		25	ns	15, 25
Column-address hold time	tCAH	15		17		ns	25
$\overline{CAS}$ pulse width	tCAS	10	10,000	12	10,000	ns	
$\overline{RAS}$ LOW to "don't care" during SELF REFRESH	tCHD	15		15		ns	36
$\overline{CAS}$ hold time (CBR REFRESH)	tCHR	8		10		ns	5, 24
$\overline{CAS}$ to output in Low-Z	tCLZ	2		2		ns	23
Data output hold after $\overline{CAS}$ LOW	tCOH	7		7		ns	23
$\overline{CAS}$ precharge time	tCP	10		10		ns	16
Access time from $\overline{CAS}$ precharge	tCPA		40		45	ns	25, 37
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	10		10		ns	25
$\overline{CAS}$ hold time	tCSH	48		53		ns	24
$\overline{CAS}$ setup time (CBR REFRESH)	tCSR	7		7		ns	5, 23
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	37		42		ns	23, 30
Write command to $\overline{CAS}$ lead time	tCWL	15		15		ns	
Data-in hold time	tDH	15		17		ns	25, 29
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		ns	
Data-in setup time	tDS	-2		-2		ns	24, 29
Output disable	tOD	0	15	0	15	ns	
Output enable	tOE		15		15	ns	
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	8		10		ns	24
$\overline{OE}$ HIGH hold time from $\overline{CAS}$ HIGH	tOEHC	10		10		ns	
$\overline{OE}$ HIGH pulse width	tOEP	10		10		ns	
$\overline{OE}$ LOW to $\overline{CAS}$ HIGH setup time	tOES	5		5		ns	
Output buffer turn-off delay	tOFF	5	20	5	20	ns	20,27,38
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	tORD	0		0		ns	20
EDO-PAGE-MODE READ or WRITE cycle time	tPC	25		30		ns	
$\overline{PDE}$ to valid presence-detect data	tPD		10		10	ns	35
$\overline{PDE}$ inactive to presence-detects inactive	tPDOFF	2		2		ns	34
EDO-PAGE-MODE READ-WRITE cycle time	tPRWC	77		87		ns	23
Access time from $\overline{RAS}$	tRAC		60		70	ns	14
$\overline{RAS}$ to column-address delay time	tRAD	10	25	10	30	ns	18, 26
Row-address hold time	tRAH	8		8		ns	24
Column-address to $\overline{RAS}$ lead time	tRAL	35		40		ns	25
$\overline{RAS}$ pulse width	tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (EDO PAGE MODE)	tRASP	60	125,000	70	125,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH	tRASS	100		100		µs	36
Random READ or WRITE cycle time	tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	12	40	12	45	ns	17, 26

EDO PAGE MODE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Read command hold time (referenced to $\overline{CAS}$)	tRCH	2		2		ns	19, 23
Read command setup time	tRCS	2		2		ns	23
Refresh period (2,048 cycles)	tREF		32		32	ms	
Refresh period (2,048 cycles) S version	tREF		128		128	ms	
$\overline{RAS}$ precharge time	tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH	tRPS	110		130		ns	36
Read command hold time (referenced to $\overline{RAS}$)	tRRH	0		0		ns	19
$\overline{RAS}$ hold time	tRSH	15		17		ns	25
READ WRITE cycle time	tRWC	155		182		ns	25
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	82		92		ns	23, 30
Write command to $\overline{RAS}$ lead time	tRWL	20		20		ns	25
Transition time (rise or fall)	tT	2	50	2	50	ns	
Write command hold time	tWCH	15		17		ns	25
Write command hold time (referenced to $\overline{RAS}$)	tWCR	43		53		ns	24
$\overline{WE}$ command setup time	tWCS	2		2		ns	23
Output disable delay from $\overline{WE}$ ($\overline{CAS}$ HIGH)	tWHZ	2	18	2	20	ns	27
Write command pulse width	tWP	10		12		ns	
$\overline{WE}$ pulse width for output disable when $\overline{CAS}$ HIGH	tWPZ	10		12		ns	
$\overline{WE}$ hold time (CBR REFRESH)	tWRH	8		8		ns	22, 24
$\overline{WE}$ setup time (CBR REFRESH)	tWRP	12		12		ns	22, 23

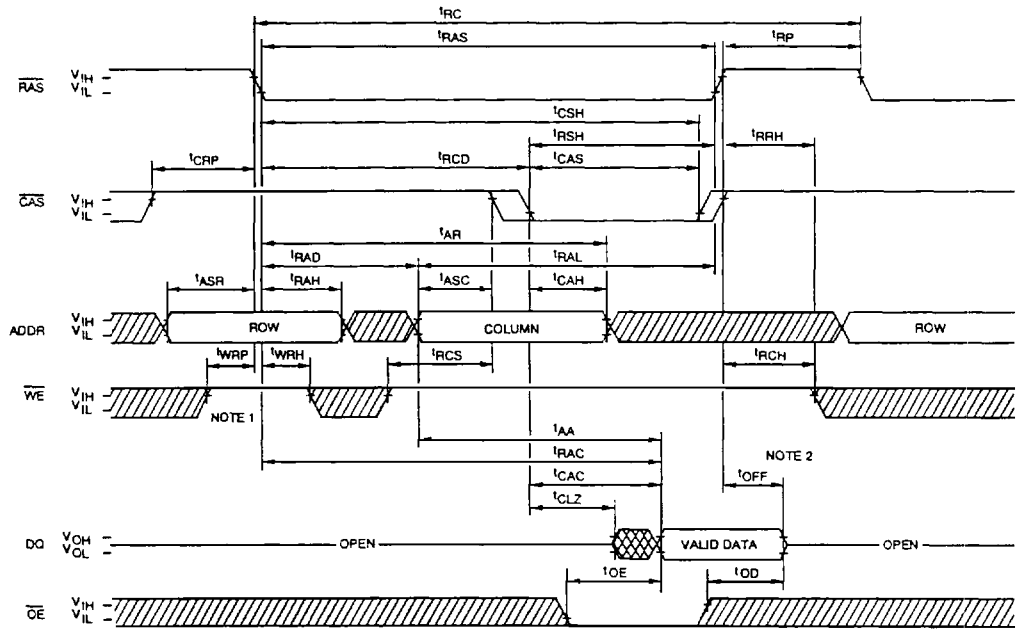
NOTES

1. All voltages referenced to Vss.
2. This parameter is sampled. Vcc = +3.3V ±0.3V; f = 1 MHz.
3. Icc is dependent on cycle rates.
4. Icc is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns for FPM and 2.5ns for EDO.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CP.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
22. ^{t}WTS and ^{t}WTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverse of ^{t}WRP and ^{t}WRH in the CBR REFRESH cycle.
23. A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
24. A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
25. A +5ns timing skew from the DRAM to the module resulted from the addition of line drivers.
26. A -2ns (MIN) and a -5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
27. A +2ns (MIN) and a +5ns (MAX) timing skew from the DRAM to the module resulted from the addition of line drivers.
28. The maximum current ratings are based with the memory operating or being refreshed in the x72 mode. The stated maximums may be reduced by approximately one-half when used in the x36 mode.
29. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
30. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
31. Refresh current increases if ^{t}RAS is extended beyond its minimum specification.
32. Column-address changed once each cycle.

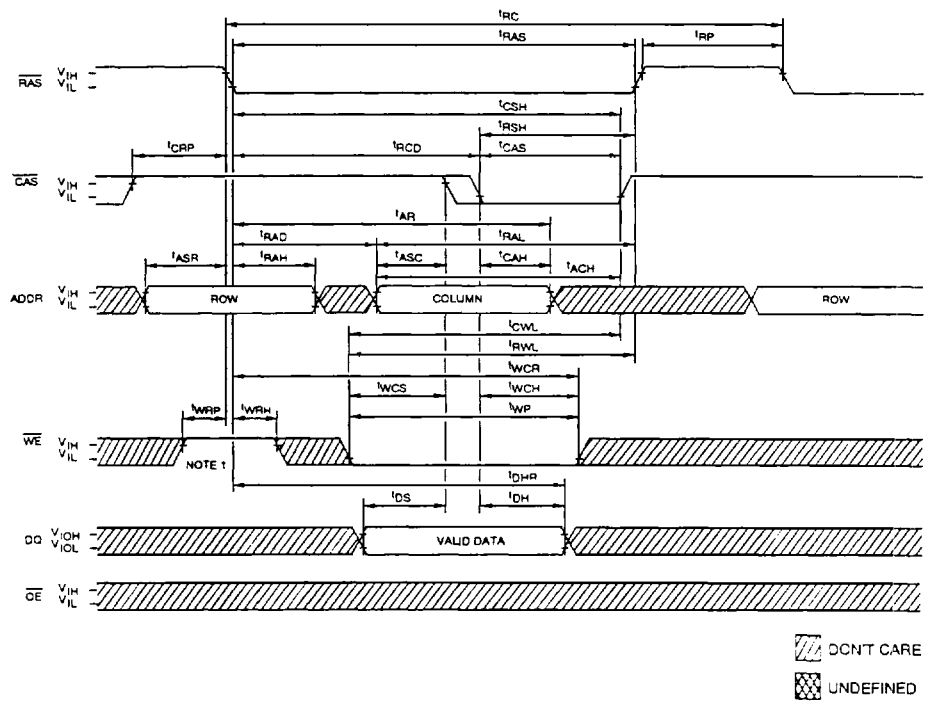
NOTES (continued)

33. The 3ns minimum parameter guaranteed by design.
34. ^{t}PDOFF MAX is determined by the pull-up resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent DIMM position.
35. Measured with the specified current load and 100pf.
36. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.
37. ^{t}CAC (MIN), ^{t}CPA (MIN) and ^{t}AA (MIN) are for reference only to help aid the user as to when to expect the earliest data to be accessed. Only ^{t}CAC (MAX), ^{t}CPA (MAX) and ^{t}AA (MAX) are guaranteed.
38. For FAST PAGE MODE option, ^{t}OFF is determined by the first $\overline{RAS}$ or $\overline{CAS}$ signal to transition HIGH. In comparison, ^{t}OFF on an EDO option is determined by the latter of the $\overline{RAS}$ and $\overline{CAS}$ signal to transition HIGH.
39. Applies to both EDO and FAST PAGE MODEs.

READ CYCLE [39]

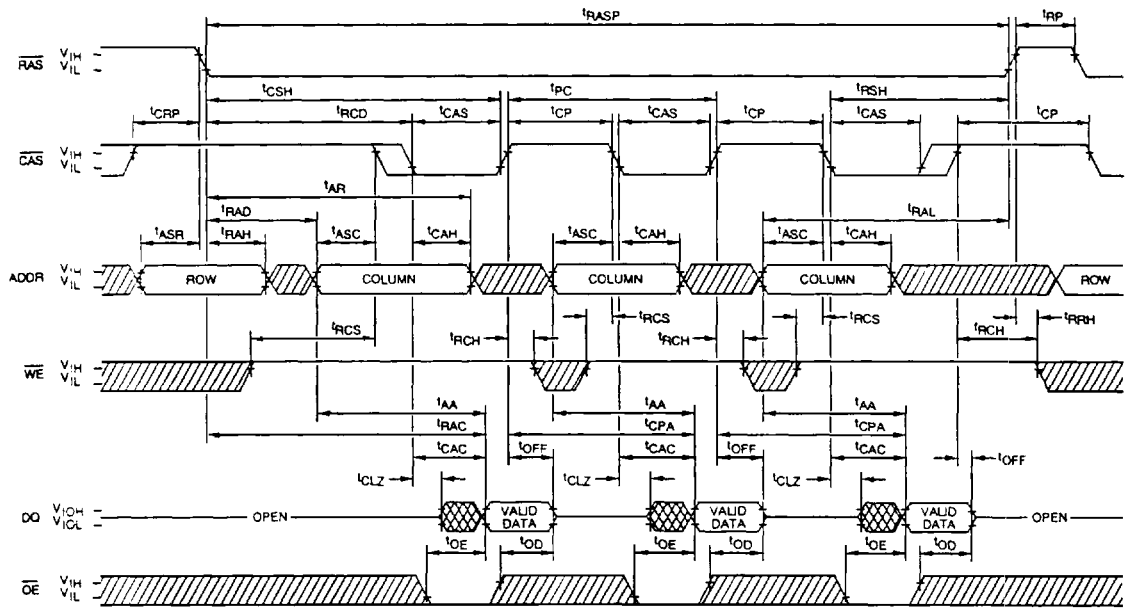


EARLY WRITE CYCLE [39]

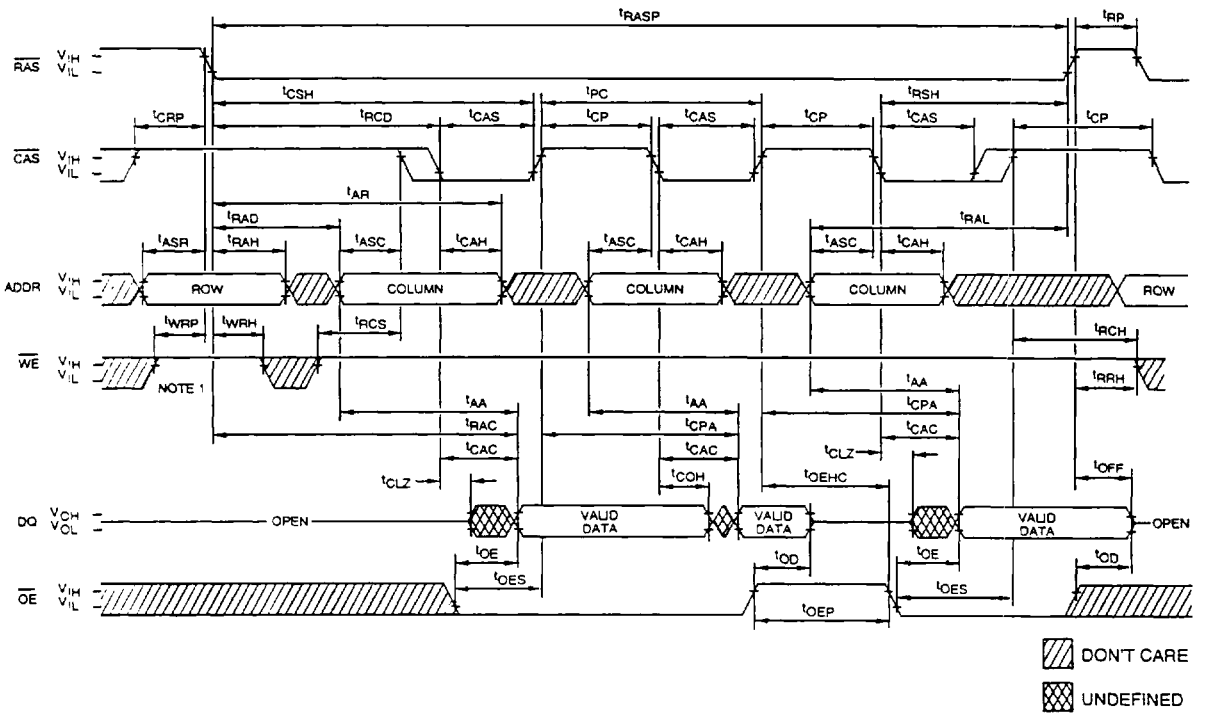


NOTE:
1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. tOFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

FAST-PAGE-MODE READ CYCLE

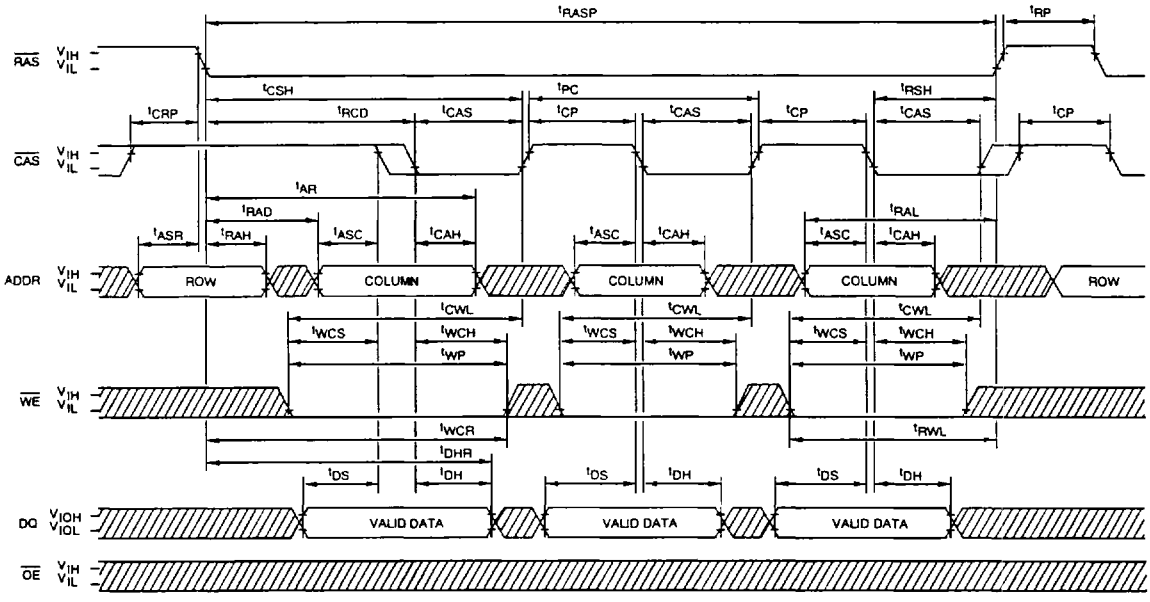


EDO-PAGE-MODE READ CYCLE

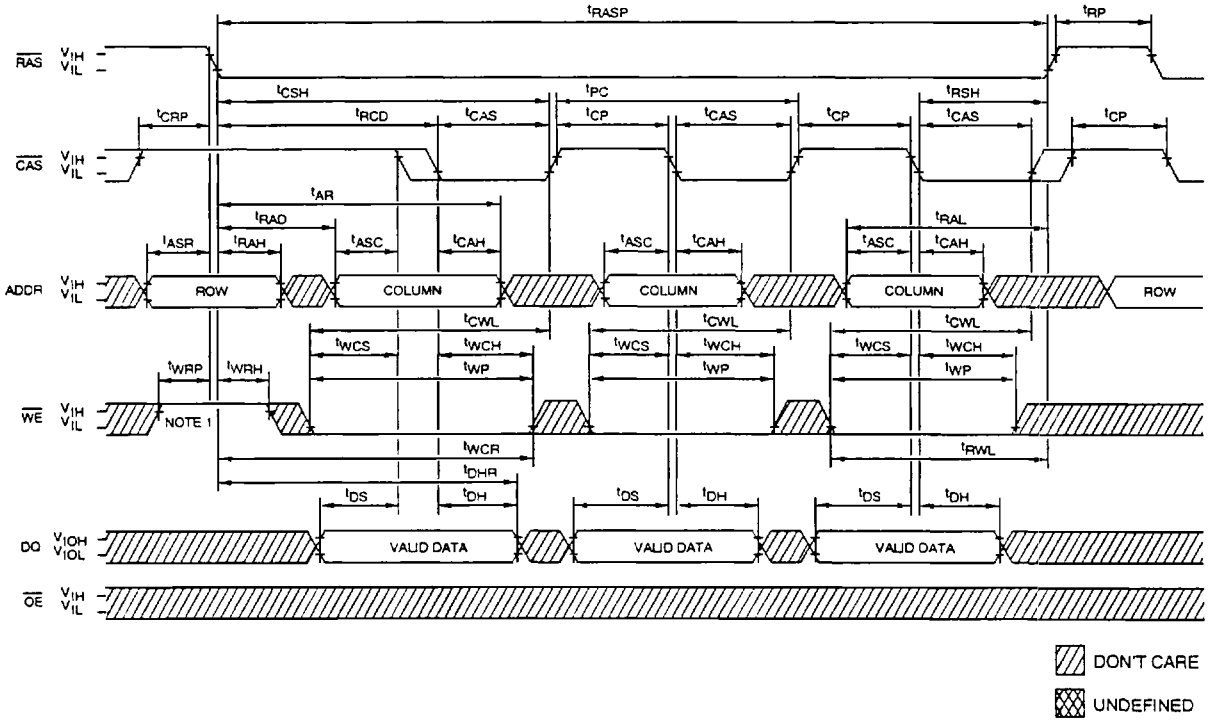


NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

FAST-PAGE-MODE EARLY-WRITE CYCLE



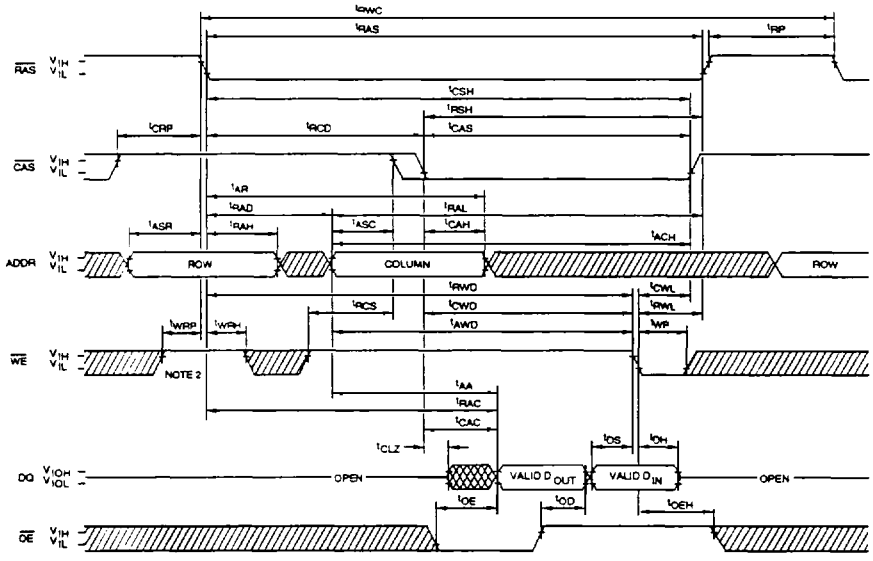
EDO-PAGE-MODE EARLY-WRITE CYCLE



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

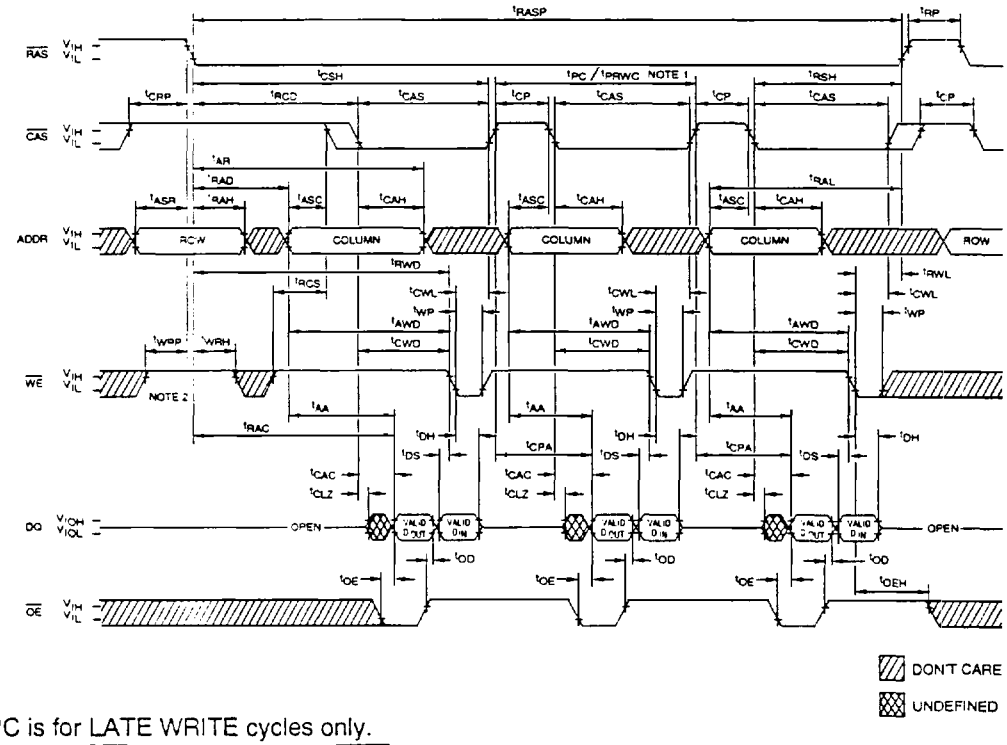
READ WRITE CYCLE [39]

(LATE WRITE and READ-MODIFY-WRITE cycles)



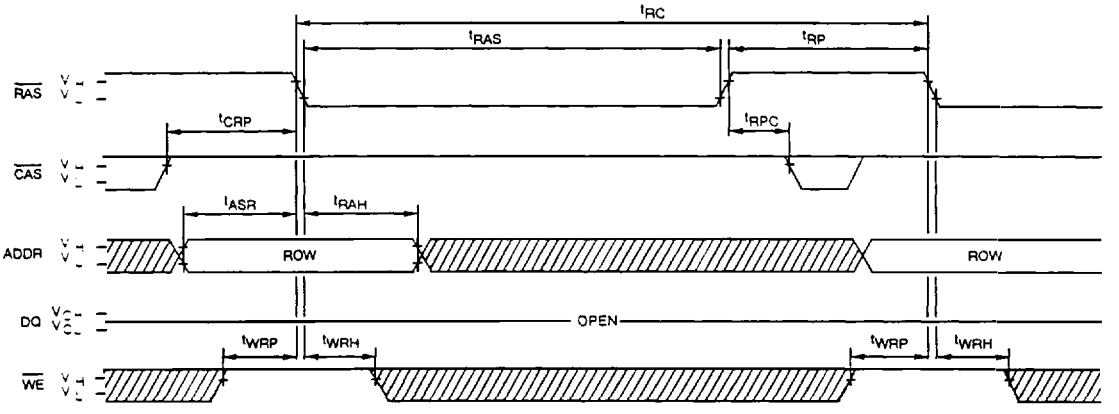
EDO/FAST PAGE MODE-PAGE-MODE READ-WRITE CYCLE [39]

(LATE WRITE and READ-MODIFY-WRITE cycles)

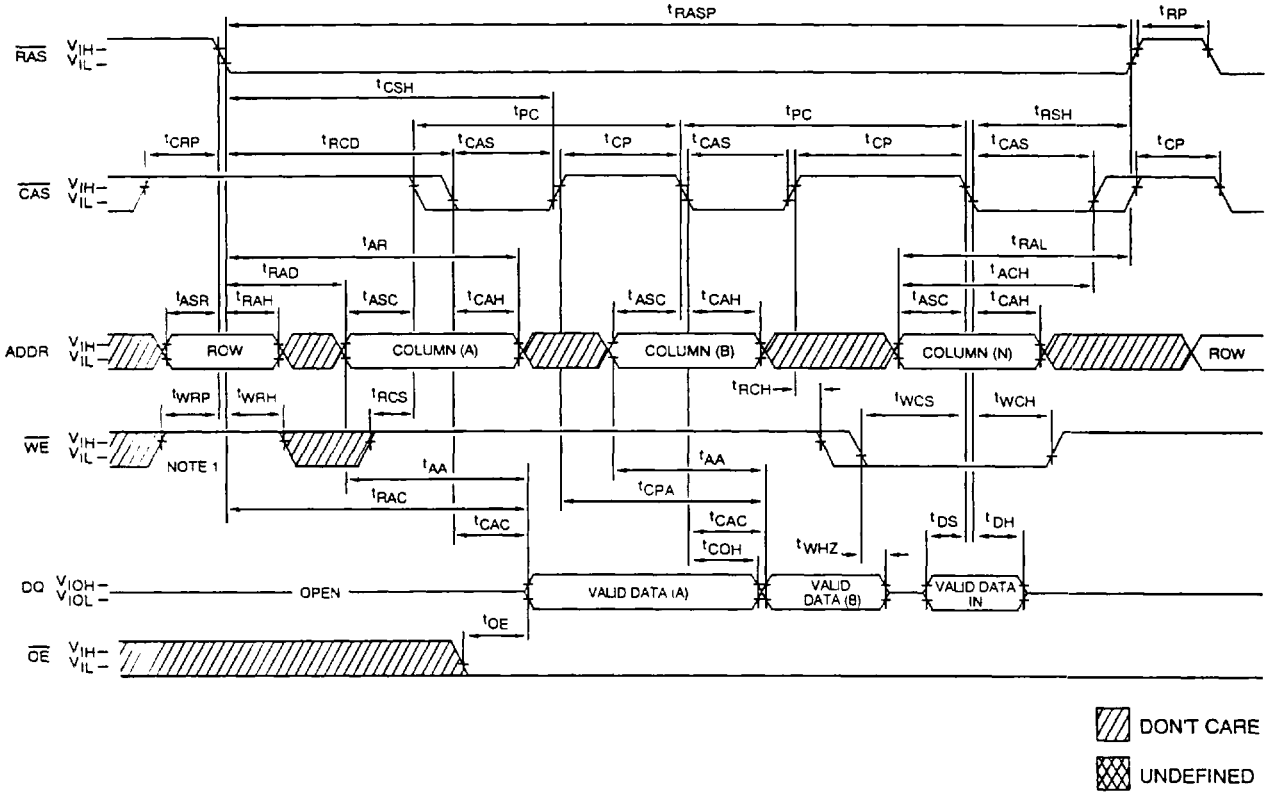


NOTE:
1. tPC is for LATE WRITE cycles only.
2. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

RAS-ONLY REFRESH CYCLE [39]
(WE = DON'T CARE)

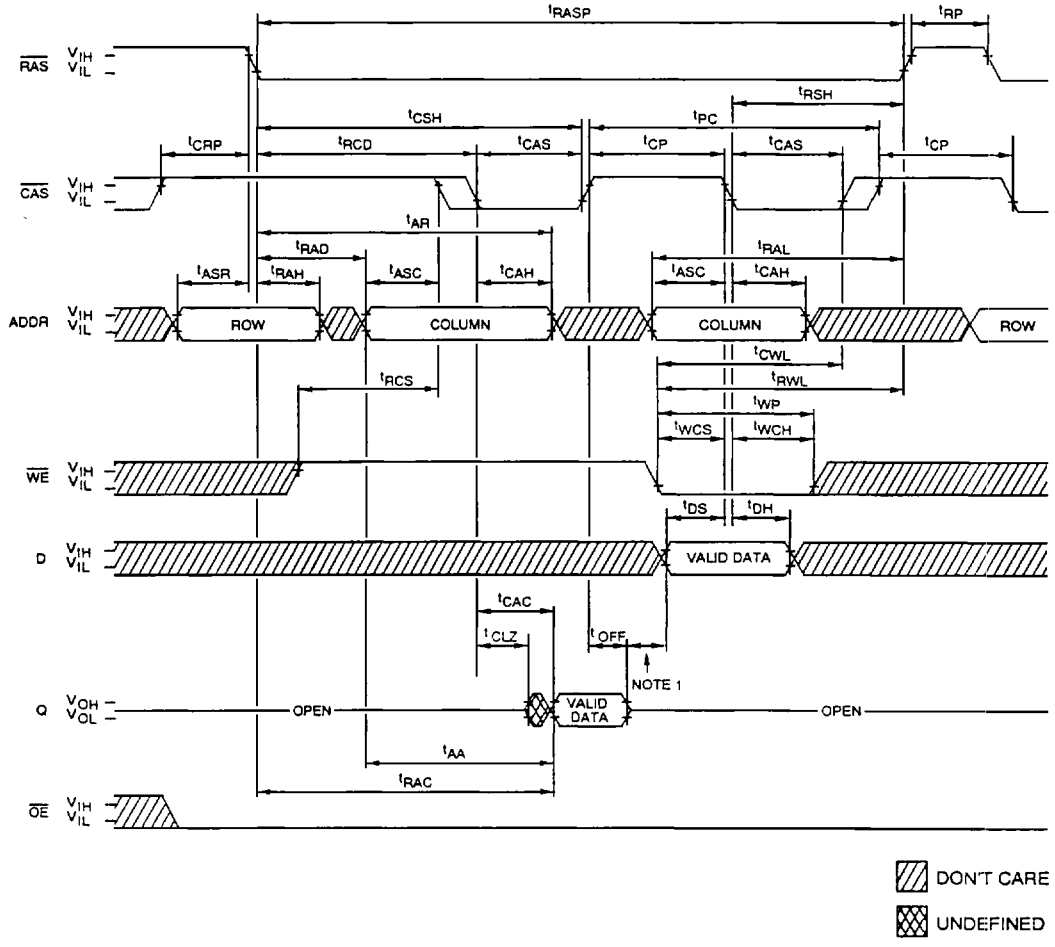


EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Although WE is a "don't care" at RAS time during an access cycle (READ or WRITE), the system designer should implement WE HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

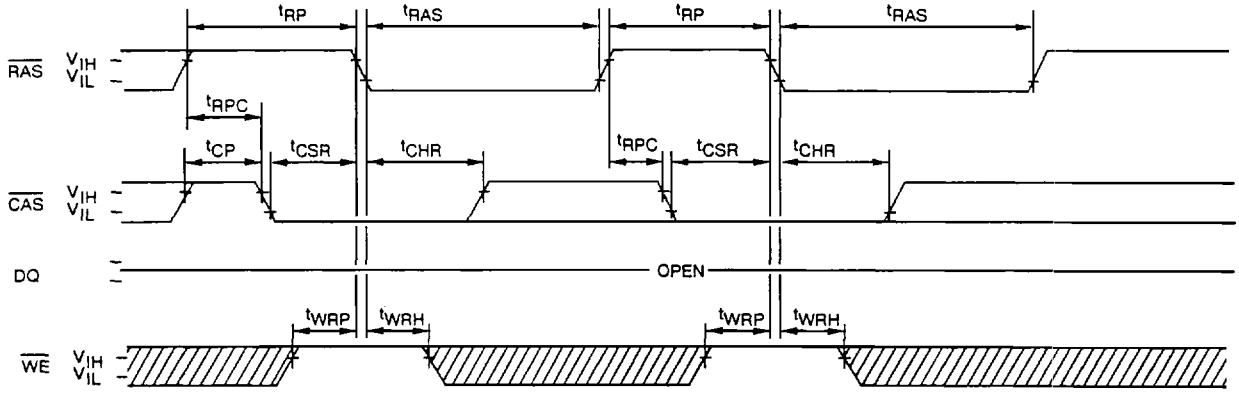
FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate.

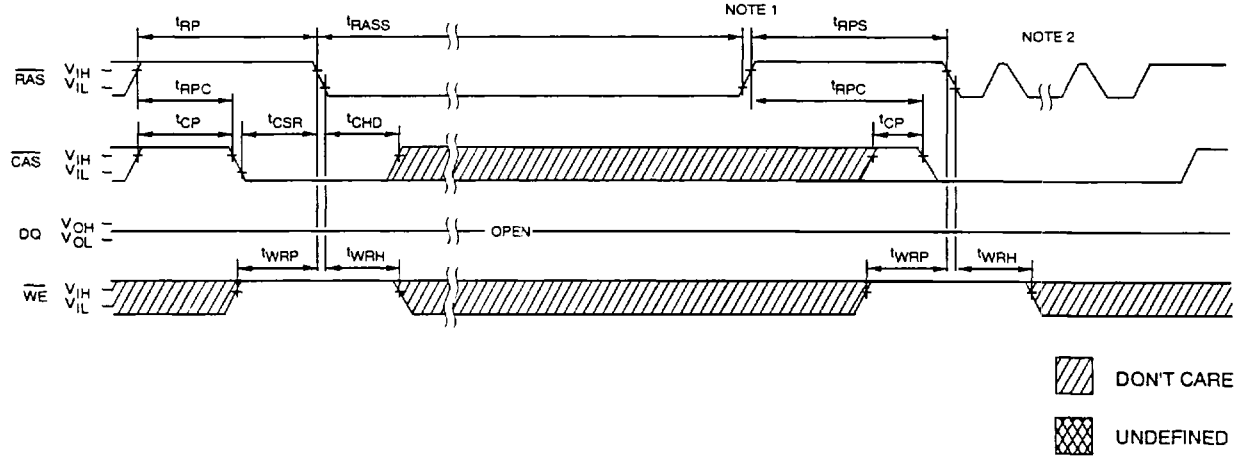
CBR REFRESH CYCLE [39]

(Addresses, $\overline{OE}$ = DON'T CARE)



SELF REFRESH CYCLE [39]

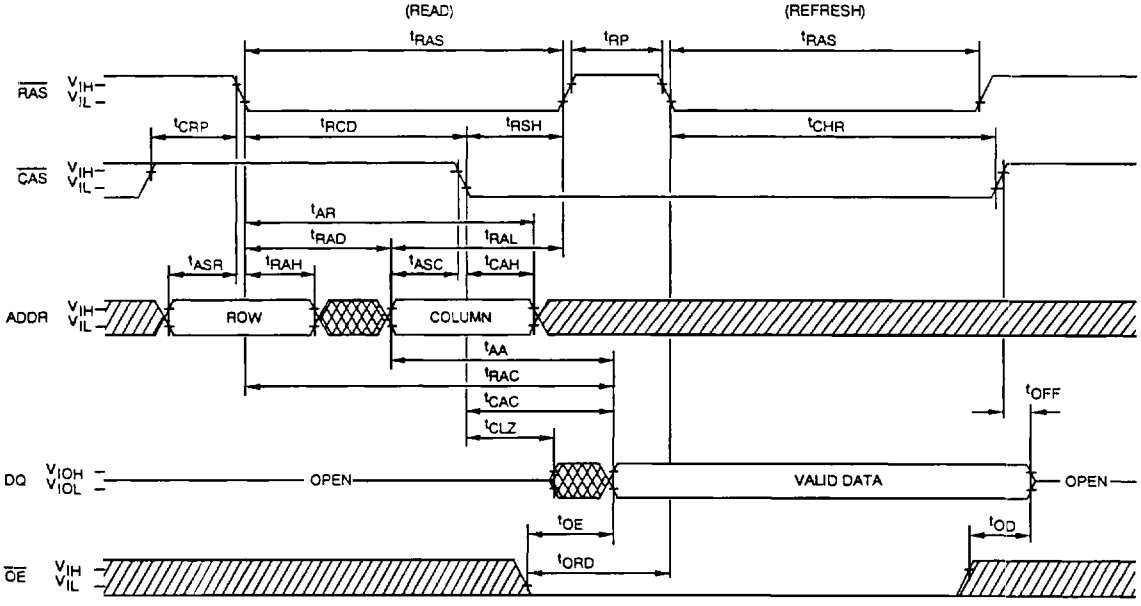
(Addresses and $\overline{OE}$ = DON'T CARE)



NOTE: 1. Once tRASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

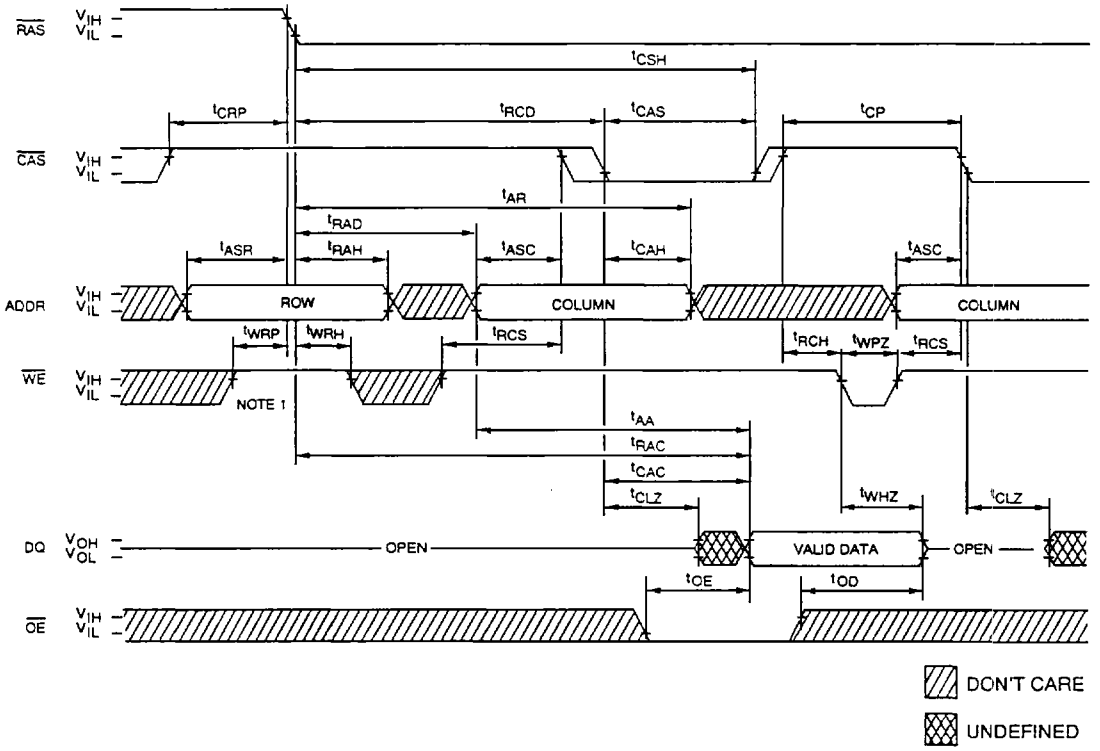
HIDDEN REFRESH CYCLE [21, 39]

($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



PRESENCE DETECT READ CYCLE [39]

EDO READ CYCLE
(with $\overline{WE}$-controlled disable)



NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.