National Semiconductor

ADVANCED INFORMATION

# 54F/74F256
# Dual 4-Bit Addressable Latch

## General Description

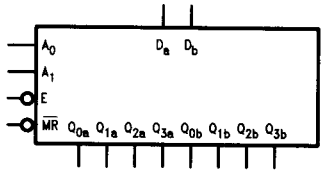
The 'F256 dual addressable latch has four distinct modes of operation which are selectable by controlling the Clear and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode ($\overline{MR}$ = $\overline{E}$ = LOW), addressed outputs will follow the level of the D inputs with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the Address and Data inputs.

## Features

- Combines dual demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common clear input
- Useful as dual 1-of-4 active HIGH decoder

## Logic Symbols

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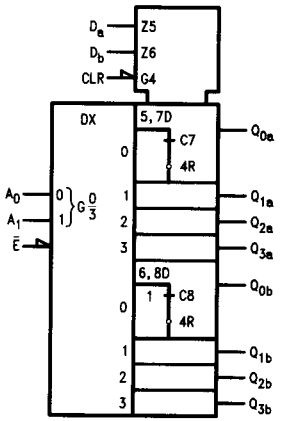
**IEEE/IEC**

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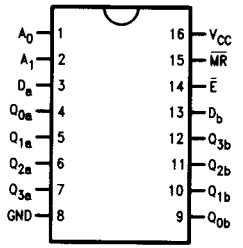
## Connection Diagrams

**Pin Assignment for DIP, SOIC and Flatpak**

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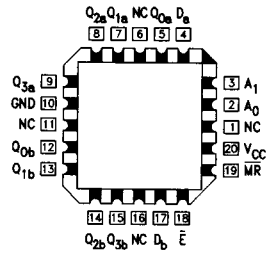
**Pin Assignment for LCC and PCC**

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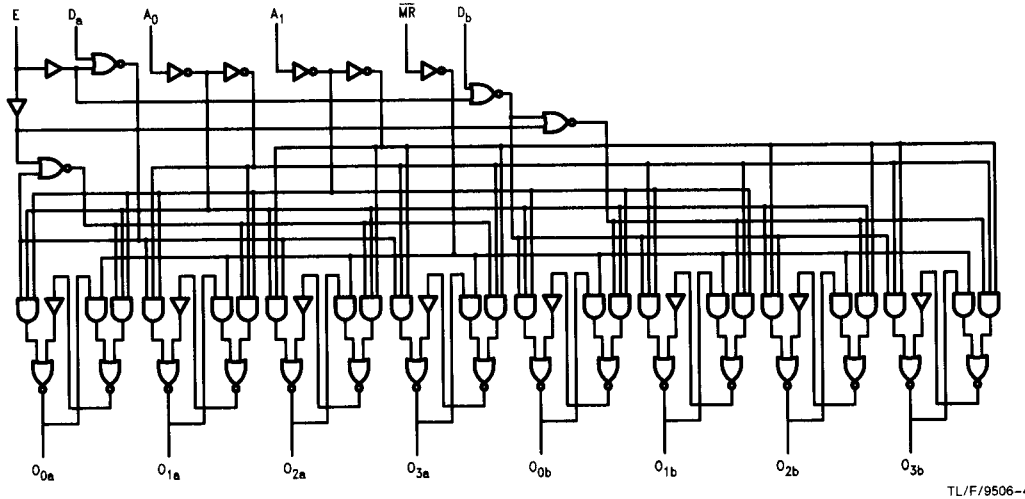
**Mode Select-Function Table**

| Operating Mode | Inputs | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{MR}$ | $\overline{E}$ | D | $A_0$ | $A_1$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| Master Reset | L | H | X | X | X | L | L | L | L |
| Demultiplex (Active HIGH Decoder when D = H) | L | L | d | L | L | Q = d | L | L | L |
| | L | L | d | H | L | L | Q = d | L | L |
| | L | L | d | L | H | L | L | Q = d | L |
| | L | L | d | H | H | L | L | L | Q = d |
| Store (Do Nothing) | H | H | X | X | X | $q_0$ | $q_1$ | $q_2$ | $q_3$ |
| Addressable Latch | H | L | d | L | L | Q = d | $q_1$ | $q_2$ | $q_3$ |
| | H | L | d | H | L | $q_0$ | Q = d | $q_2$ | $q_3$ |
| | H | L | d | L | H | $q_0$ | $q_1$ | Q = d | $q_3$ |
| | H | L | d | H | H | $q_0$ | $q_1$ | $q_2$ | Q = d |

H = HIGH Voltage Level Steady State
L = LOW Voltage Level Steady State
X = Immaterial
d = HIGH or LOW Data one setup time prior to the LOW-to-HIGH Enable transition
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

## Logic Diagram

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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.