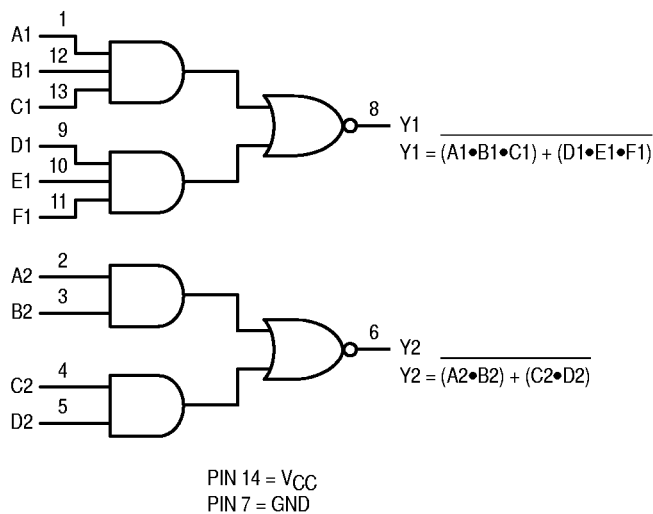


## 2-Wide, 2-Input/2-Wide, 3-Input AND-NOR Gates High-Performance Silicon-Gate CMOS

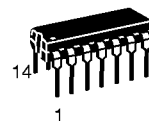
The MC74HC51 is identical in pinout to the LS51. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 42 FETs or 10.5 Equivalent Gates

### LOGIC DIAGRAM



## MC74HC51



**N SUFFIX**  
PLASTIC PACKAGE  
CASE 646-06



**D SUFFIX**  
SOIC PACKAGE  
CASE 751A-03

### ORDERING INFORMATION

MC74HCXXN Plastic  
MC74HCXXD SOIC

### PIN ASSIGNMENT

|     |   |    |     |
|-----|---|----|-----|
| A1  | 1 | 14 | VCC |
| A2  | 2 | 13 | C1  |
| B2  | 3 | 12 | B1  |
| C2  | 4 | 11 | F1  |
| D2  | 5 | 10 | E1  |
| Y2  | 6 | 9  | D1  |
| GND | 7 | 8  | Y1  |

### FUNCTION TABLES

| Inputs                 |    |    |    |    |    | Output |
|------------------------|----|----|----|----|----|--------|
| A1                     | B1 | C1 | D1 | E1 | F1 | Y1     |
| H                      | H  | H  | X  | X  | X  | L      |
| X                      | X  | X  | H  | H  | H  | L      |
| All other combinations |    |    |    |    |    | H      |

| Inputs                 |    |    |    | Output |
|------------------------|----|----|----|--------|
| A2                     | B2 | C2 | D2 | Y2     |
| H                      | H  | X  | X  | L      |
| X                      | X  | H  | H  | L      |
| All other combinations |    |    |    | H      |



**MAXIMUM RATINGS\***

| Symbol           | Parameter  | Value                          | Unit |
|------------------|--|--------------------------------|------|
| V <sub>CC</sub>  | DC Supply Voltage (Referenced to GND)  | - 0.5 to + 7.0                 | V    |
| V <sub>in</sub>  | DC Input Voltage (Referenced to GND)   | - 1.5 to V <sub>CC</sub> + 1.5 | V    |
| V <sub>out</sub> | DC Output Voltage (Referenced to GND)  | - 0.5 to V <sub>CC</sub> + 0.5 | V    |
| I <sub>in</sub>  | DC Input Current, per Pin  | ± 20                           | mA   |
| I <sub>out</sub> | DC Output Current, per Pin   | ± 25                           | mA   |
| I <sub>CC</sub>  | DC Supply Current, V <sub>CC</sub> and GND Pins                                  | ± 50                           | mA   |
| P <sub>D</sub>   | Power Dissipation in Still Air<br>Plastic DIP†<br>SOIC Package†                  | 750<br>500                     | mW   |
| T <sub>stg</sub> | Storage Temperature  | - 65 to + 150                  | °C   |
| T <sub>L</sub>   | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package) | 260                            | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.  
 † Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C  
 SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**RECOMMENDED OPERATING CONDITIONS**

| Symbol                             | Parameter  | Min   | Max             | Unit               |    |
|------------------------------------|--|---|-----------------|--------------------|----|
| V <sub>CC</sub>                    | DC Supply Voltage (Referenced to GND)                | 2.0   | 6.0             | V                  |    |
| V <sub>in</sub> , V <sub>out</sub> | DC Input Voltage, Output Voltage (Referenced to GND) | 0   | V <sub>CC</sub> | V                  |    |
| T <sub>A</sub>                     | Operating Temperature, All Package Types             | - 55  | + 125           | °C                 |    |
| t <sub>r</sub> , t <sub>f</sub>    | Input Rise and Fall Time<br>(Figure 1)               | V <sub>CC</sub> = 2.0 V<br>V <sub>CC</sub> = 4.5 V<br>V <sub>CC</sub> = 6.0 V | 0<br>0<br>0     | 1000<br>500<br>400 | ns |

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

| Symbol          | Parameter                                      | Test Conditions   | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|-----------------|--|---|----------------------|------------------|--------|---------|------|
|                 |  |   |                      | - 55 to 25°C     | ≤ 85°C | ≤ 125°C |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage               | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA  | 2.0                  | 1.5              | 1.5    | 1.5     | V    |
|                 |  |   | 4.5                  | 3.15             | 3.15   | 3.15    |      |
|                 |  |   | 6.0                  | 4.2              | 4.2    | 4.2     |      |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage                | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA  | 2.0                  | 0.3              | 0.3    | 0.3     | V    |
|                 |  |   | 4.5                  | 0.9              | 0.9    | 0.9     |      |
|                 |  |   | 6.0                  | 1.2              | 1.2    | 1.2     |      |
| V <sub>OH</sub> | Minimum High-Level Output Voltage              | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA | 2.0                  | 1.9              | 1.9    | 1.9     | V    |
|                 |  |   | 4.5                  | 4.4              | 4.4    | 4.4     |      |
|                 |  |   | 6.0                  | 5.9              | 5.9    | 5.9     |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage               | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA | 2.0                  | 0.1              | 0.1    | 0.1     | V    |
|                 |  |   | 4.5                  | 0.1              | 0.1    | 0.1     |      |
|                 |  |   | 6.0                  | 0.1              | 0.1    | 0.1     |      |
| I <sub>in</sub> | Maximum Input Leakage Current                  | V <sub>in</sub> = V <sub>CC</sub> or GND  | 2.0                  | ± 0.1            | ± 1.0  | ± 1.0   | μA   |
|                 |  |   | 4.5                  |                  |        |         |      |
|                 |  |   | 6.0                  |                  |        |         |      |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 μA                 | 2.0                  | 2                | 20     | 40      | μA   |
|                 |  |   | 4.5                  |                  |        |         |      |
|                 |  |   | 6.0                  |                  |        |         |      |

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

**AC ELECTRICAL CHARACTERISTICS** ( $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6 \text{ ns}$ )

| Symbol                   | Parameter   | $V_{CC}$<br>V     | Guaranteed Limit |                         |                          | Unit |
|--------------------------|---|-------------------|------------------|-------------------------|--------------------------|------|
|                          |   |                   | - 55 to<br>25°C  | $\leq 85^\circ\text{C}$ | $\leq 125^\circ\text{C}$ |      |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Maximum Propagation Delay, Any Input to Output Y<br>(Figures 1 and 2) | 2.0<br>4.5<br>6.0 | 125<br>25<br>21  | 155<br>31<br>26         | 190<br>38<br>32          | ns   |
| $t_{TLH}$ ,<br>$t_{THL}$ | Maximum Output Transition Time, Any Output<br>(Figures 1 and 2)       | 2.0<br>4.5<br>6.0 | 75<br>15<br>13   | 95<br>19<br>16          | 110<br>22<br>19          | ns   |
| $C_{in}$                 | Maximum Input Capacitance   | —                 | 10               | 10                      | 10                       | pF   |

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

| $C_{PD}$ | Power Dissipation Capacitance (Per Section)* | Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$ | pF |
|----------|--|--|----|
|          |  | 23                                       |    |

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

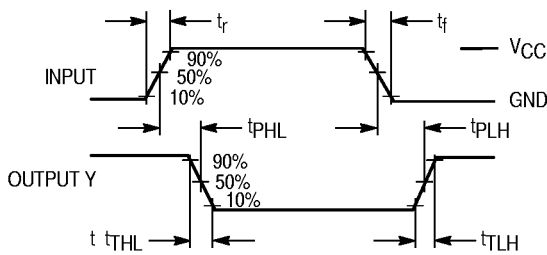
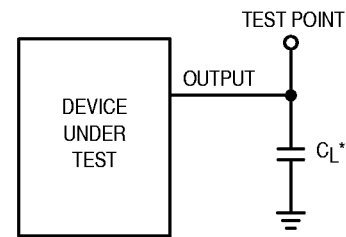


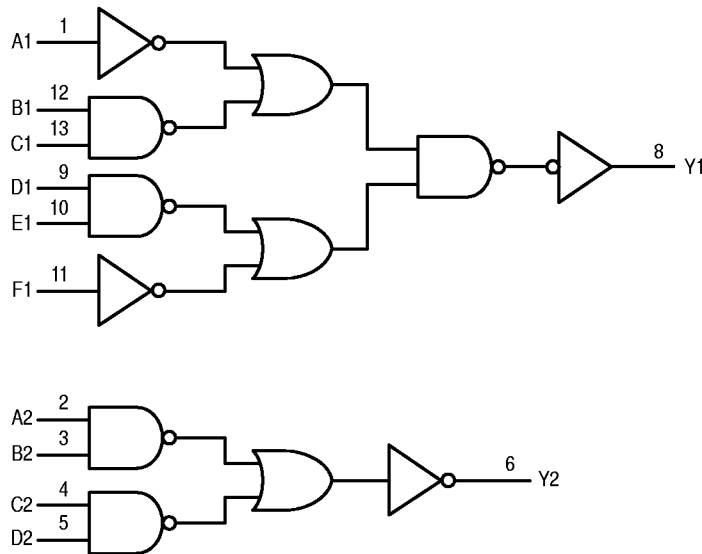
Figure 1. Switching Waveforms



\* Includes all probe and jig capacitance

Figure 2. Test Circuit

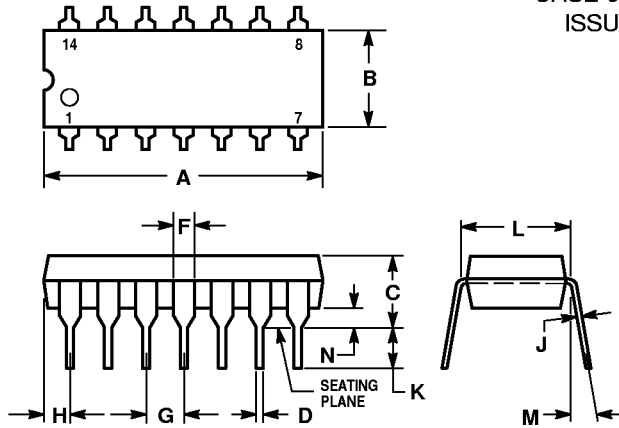
**EXPANDED LOGIC DIAGRAM**



PIN 14 =  $V_{CC}$   
PIN 7 = GND

OUTLINE DIMENSIONS

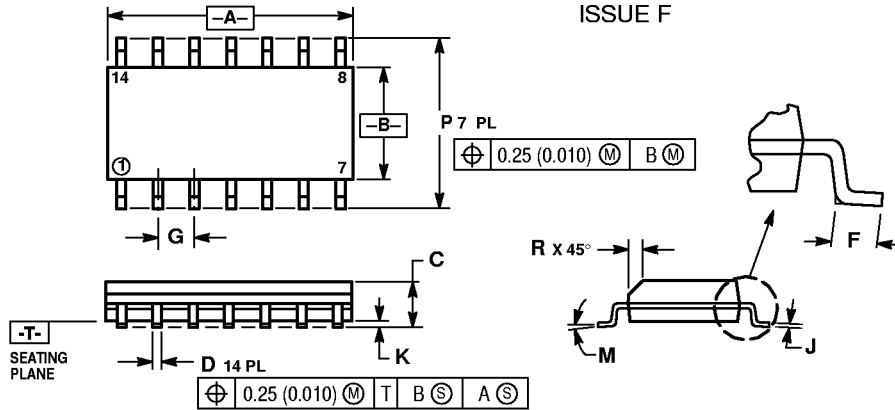
**N SUFFIX**  
**PLASTIC DIP PACKAGE**  
 CASE 646-06  
 ISSUE L



- NOTES:
- LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  - DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  - DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  - ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.715     | 0.770 | 18.16       | 19.56 |
| B   | 0.240     | 0.260 | 6.10        | 6.60  |
| C   | 0.145     | 0.185 | 3.69        | 4.69  |
| D   | 0.015     | 0.021 | 0.38        | 0.53  |
| F   | 0.040     | 0.070 | 1.02        | 1.78  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.052     | 0.095 | 1.32        | 2.41  |
| J   | 0.008     | 0.015 | 0.20        | 0.38  |
| K   | 0.115     | 0.135 | 2.92        | 3.43  |
| L   | 0.300 BSC |       | 7.62 BSC    |       |
| M   | 0°        | 10°   | 0°          | 10°   |
| N   | 0.015     | 0.039 | 0.39        | 1.01  |

**D SUFFIX**  
**PLASTIC SOIC PACKAGE**  
 CASE 751A-03  
 ISSUE F



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: MILLIMETER.
  - DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  - MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  - DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 8.55        | 8.75 | 0.337     | 0.344 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.054     | 0.068 |
| D   | 0.35        | 0.49 | 0.014     | 0.019 |
| F   | 0.40        | 1.25 | 0.016     | 0.049 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| J   | 0.19        | 0.25 | 0.008     | 0.009 |
| K   | 0.10        | 0.25 | 0.004     | 0.009 |
| M   | 0°          | 7°   | 0°        | 7°    |
| P   | 5.80        | 6.20 | 0.228     | 0.244 |
| R   | 0.25        | 0.50 | 0.010     | 0.019 |

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