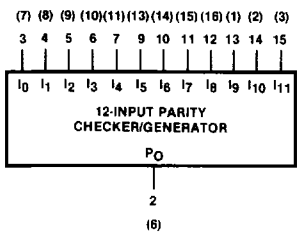
F10160 • F10560
12-BIT PARITY CHECKER/GENERATOR

DESCRIPTION — The F10160 and F10560 are 12-Input Parity Generators. The output will be HIGH when an odd number of inputs are HIGH; typical delay is 4 ns. For applications requiring fewer than 12 inputs, unused inputs may be left open, since internal input resistors hold unconnected inputs LOW.

PIN NAMES

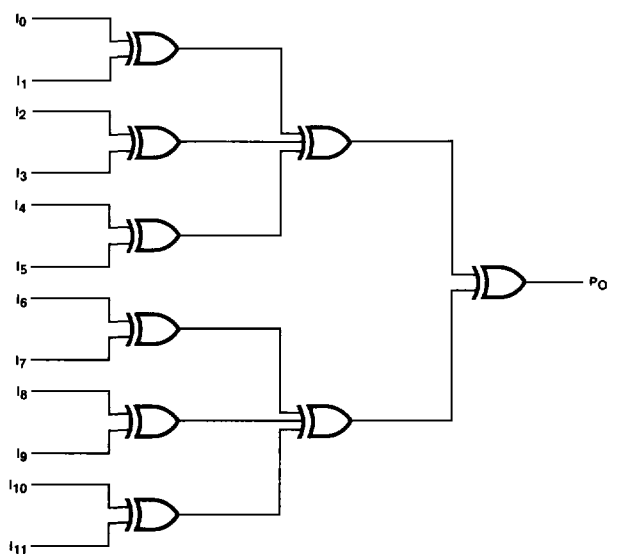
I_n	Inputs
P_O	Parity Odd

LOGIC SYMBOL

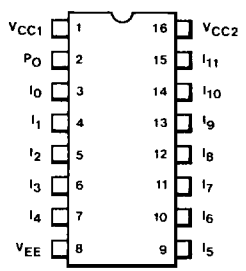


V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



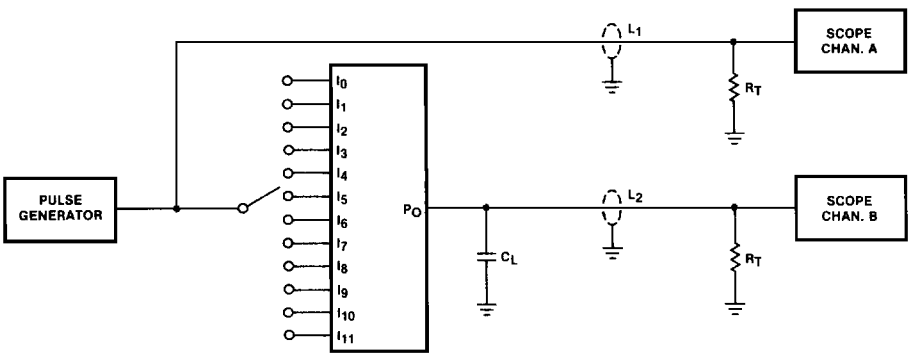
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH (All Inputs)			220	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−59	−46		mA	25°C	Inputs and Outputs Open

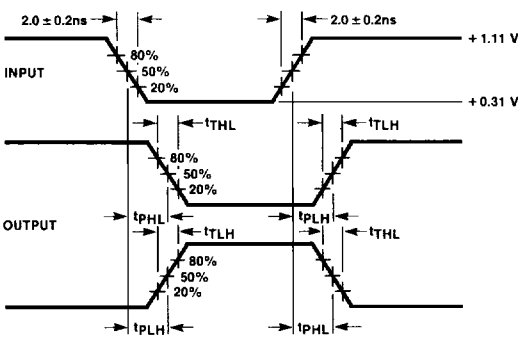
SWITCHING CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay, LOW to HIGH, HIGH to LOW	2.0	4.0	7.5	ns	See Figure 1
t_{TLH}, t_{THL}	Output Transition Time LOW to HIGH, HIGH to LOW (20% to 80%) (80% to 20%)	1.5	2.0	3.3	ns	

SWITCHING CIRCUIT AND WAVEFORM



L_1 and L_2 = equal length 50 Ω impedance lines
$R_T = 50$ Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF



Jig set-up with no circuit under test
$V_{CC1} = V_{CC2} = +2.0$ V
$V_{EE} = -3.2$ V

Fig. 1.