

FMB MB9A110A Series

32-bit ARM™ Cortex™-M3 based Microcontroller
MB9AF111LA/MA/NA, MB9AF112LA/MA/NA,
MB9AF114LA/MA/NA, MB9AF115MA/NA, MB9AF116MA/NA

Data Sheet (Full Production)





FM3 MB9A110A Series

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■ DESCRIPTION

The MB9A110A Series are highly integrated 32-bit microcontrollers that target for high-performance and cost-sensitive embedded control applications.

The MB9A110A Series are based on the ARM Cortex-M3 Processor with on-chip Flash memory and SRAM, and have peripheral functions such as Motor Control Timers, ADCs and Communication Interfaces (UART, CSIO, I²C, LIN).

The products which are described in this data sheet are placed into TYPE1 product categories in "FM3 Family PERIPHERAL MANUAL".

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ARM™

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This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion Inc. deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur.

■ FEATURES

- 32-bit ARM Cortex-M3 Core
 - Processor version: r2p1
 - Up to 40MHz Frequency Operation
 - Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
 - 24-bit System timer (Sys Tick): System timer for OS task management

- On-chip Memories

[Flash memory]

- Up to 512 Kbytes
- Read cycle: 0wait-cycle
- Security function for code protection

[SRAM]

This Series contains a total of up to 32Kbyte on-chip SRAM memories. This is composed of two independent SRAM (SRAM0, SRAM1). SRAM0 is connected to I-code bus or D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

- SRAM0: Up to 16 Kbyte
- SRAM1: Up to 16 Kbyte

- External Bus Interface*

- Supports SRAM, NOR Flash device
- Up to 8 chip selects
- 8/16-bit Data width
- Up to 25-bit Address bit
- Supports Address/Data multiplex
- Supports external RDY function.

* : MB9AF111LA, F112LA and F114LA do not support External Bus Interface.

- Multi-function Serial Interface (Max 8channels)

- 4 channels with 16-byte FIFO (ch.4 to ch.7), 4 channels without FIFO (ch.0 to ch.3)
- Operation mode is selectable from the followings for each channel.
 - UART
 - CSIO
 - LIN
 - I²C

[UART]

- Full duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control : Automatically control the transmission/reception by CTS/RTS (only ch.4)*
- Various error detection functions available (parity errors, framing errors, and overrun errors)
 - * : MB9AF111LA, F112LA and F114LA do not support Hardware Flow control

[CSIO]

- Full duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detection function available

[LIN]

- LIN protocol Rev.2.1 supported
- Full duplex double buffer
- Master/Slave mode supported
- LIN break field generation (can be changed 13 to 16-bit length)
- LIN break delimiter generation (can be changed 1 to 4-bit length)
- Various error detection functions available (parity errors, framing errors, and overrun errors)

[I²C]

Standard mode (Max 100kbps) / High-speed mode (Max 400kbps) supported

- DMA Controller (8channels)

The DMA Controller has an independent bus from the CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: byte/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

- A/D Converter (Max 16channels)

[12-bit A/D Converter]

- Successive Approximation type
- Built-in 3units*
- Conversion time: 1.0μs @ 5V
- Priority conversion available (priority at 2levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16steps, for Priority conversion: 4steps)
 - * : MB9AF111LA, F112LA and F114LA build in 2 unites.

- **Base Timer (Max 8channels)**

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16/32-bit reload timer
- 16/32-bit PWC timer

- **General-Purpose I/O Port**

This series can use its pins as General-Purpose I/O ports when they are not used for an external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated to.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 83 high-speed General-Purpose I/O Ports@100pin Package
- Some ports are 5V tolerant I/O (MB9AF115MA/NA, MB9AF116MA/NA only)
See "■ PIN DESCRIPTION" to confirm the corresponding pins.

- **Multi-function Timer (Max 2units)**

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3ch/unit
- Input capture × 4ch/unit
- Output compare × 6ch/unit
- A/D activating compare × 3ch/unit
- Waveform generator × 3ch/unit
- 16-bit PPG timer × 3ch/unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

- **Quadrature Position/Revolution Counter (QPRC) (Max 2units)**

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use as the up/down counter.

- The detection edge of three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

- **Dual Timer (Two 32/16-bit Down Counters)**

The Dual Timer consists of two programmable 32/16-bit down counters.

Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

- **Watch Counter**

The Watch counter is used for wake up from Low-Power Consumption mode.

- Interval timer: up to 64s (Max)@ Sub Clock : 32.768kHz

- **External Interrupt Controller Unit**

- Up to 16 external interrupt input pins
- Include one non-maskable interrupt (NMI input pin)

- **Watch dog Timer (2channels)**

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

The "Hardware" watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, "the Hardware" watchdog is active in any low-power consumption mode except STOP.

- **CRC (Cyclic Redundancy Check) Accelerator**

The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

- **Clock and Reset**

[Clocks]

Selectable from five clock sources (2 ext. osc, 2 built-in CR osc, and main PLL).

- Main Clock : 4MHz to 48MHz
- Sub Clock : 32.768kHz
- Built-in high-speed CR Clock : 4MHz
- Built-in low-speed CR Clock : 100kHz
- Main PLL Clock

[Resets]

Reset requests from INITX pins, Power-on reset, Software reset, watchdog timers reset, low-voltage detector reset and clock super visor reset.

- **Clock Super Visor (CSV)**

Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

- If external OSC clock failure (clock stop) is detected, reset is asserted.
- If external OSC frequency anomaly is detected, interrupt or reset is asserted.

- **Low-Voltage Detector (LVD)**

This Series includes 2-stages monitoring of voltage on the VCC. When the voltage falls below the voltage has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

- **Low-Power Consumption Mode**

Three Low-Power Consumption modes supported.

- SLEEP
- TIMER
- STOP

- **Debug**

- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM).*
- Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer.*

* : MB9AF111LA/MA, F112LA/MA, F114LA/MA, F115MA and F116MA support only SWJ-DP.

- **Power Supply**

Wide range voltage: $VCC = 2.7V$ to $5.5V$

■ PRODUCT LINEUP

● Memory size

| Product name | MB9AF111LA/MA/NA | MB9AF112LA/MA/NA | MB9AF114LA/MA/NA |
|---------------|------------------|------------------|------------------|
| On-chip Flash | 64Kbytes | 128Kbytes | 256Kbytes |
| On-chip SRAM | 16Kbytes | 16Kbytes | 32Kbytes |

| Product name | MB9AF115MA/NA | MB9AF116MA/NA |
|---------------|---------------|---------------|
| On-chip Flash | 384Kbytes | 512Kbytes |
| On-chip SRAM | 32Kbytes | 32Kbytes |

● Function

| Product name | | MB9AF111LA MB9AF112LA MB9AF114LA | MB9AF111MA MB9AF112MA MB9AF114MA MB9AF115MA MB9AF116MA | MB9AF111NA MB9AF112NA MB9AF114NA MB9AF115NA MB9AF116NA |
|---|------------------------|---|--|---|
| Pin count | | 64 | 80 | 100 |
| CPU | | Cortex-M3 | | |
| Freq. | | 40MHz | | |
| Supply voltage range | | 2.7V to 5.5V | | |
| DMAC | | 8ch. | | |
| External Bus Interface | | - | Addr:21-bit (Max) Data:8-bit CS:4 (Max) Support: SRAM, NOR Flash | Addr:25-bit (Max) Data:8/16-bit CS:8 (Max) Support: SRAM, NOR Flash |
| Multi-function Serial Interface (UART/CSIO/LIN/I ² C) | | 8ch. (Max) ch.4 to ch.7: FIFO (16steps × 9-bit) ch.0 to ch.3: No FIFO | | |
| Base Timer (PWC/Reload timer/PWM/PPG) | | 8ch. (Max) | | |
| MF-Timer | A/D activation compare | 3ch. | 1 unit | 2 units (Max) |
| | Input capture | 4ch. | | |
| | Free-run timer | 3ch. | | |
| | Output compare | 6ch. | | |
| | Waveform generator | 3ch. | | |
| | PPG | 3ch. | | |
| QPRC | | 2ch. (Max) | | |
| Dual Timer | | 1 unit | | |
| Watch Counter | | 1 unit | | |
| CRC Accelerator | | Yes | | |
| Watchdog timer | | 1ch. (SW) + 1ch. (HW) | | |
| External Interrupts | | 8pins (Max) + NMI × 1 | 11pins (Max) + NMI × 1 | 16pins (Max) + NMI × 1 |
| I/O ports | | 51pins (Max) | 66pins (Max) | 83pins (Max) |
| 12-bit A/D converter | | 9ch. (2 units) | 12ch. (3 units) | 16ch. (3 units) |
| CSV (Clock Super Visor) | | Yes | | |
| LVD (Low-Voltage Detector) | | 2ch. | | |
| Built-in CR | High-speed | 4MHz (± 2%) | | |
| | Low-speed | 100kHz (Typ) | | |
| Debug Function | | SWJ-DP | | SWJ-DP/ETM |

Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.

It is necessary to use the port relocate function of the I/O port according to your function use.

■ PACKAGES

| Package \ Product name | MB9AF111LA MB9AF112LA MB9AF114LA | MB9AF111MA MB9AF112MA MB9AF114MA MB9AF115MA MB9AF116MA | MB9AF111NA MB9AF112NA MB9AF114NA MB9AF115NA MB9AF116NA |
|--------------------------------------|--|--|--|
| LQFP: FPT-64P-M24/M38 (0.5mm pitch) | ○ | - | - |
| LQFP: FPT-64P-M23/M39 (0.65mm pitch) | ○ | - | - |
| QFN: LCC-64P-M24 (0.5mm pitch) | ○ | - | - |
| LQFP: FPT-80P-M21/M37 (0.5mm pitch) | - | ○ | - |
| LQFP: FPT-100P-M20/M23 (0.5mm pitch) | - | - | ○ |
| QFP: FPT-100P-M06 (0.65mm pitch) | - | - | ○ |
| BGA: BGA-112P-M04 (0.8mm pitch) | - | - | ○* |

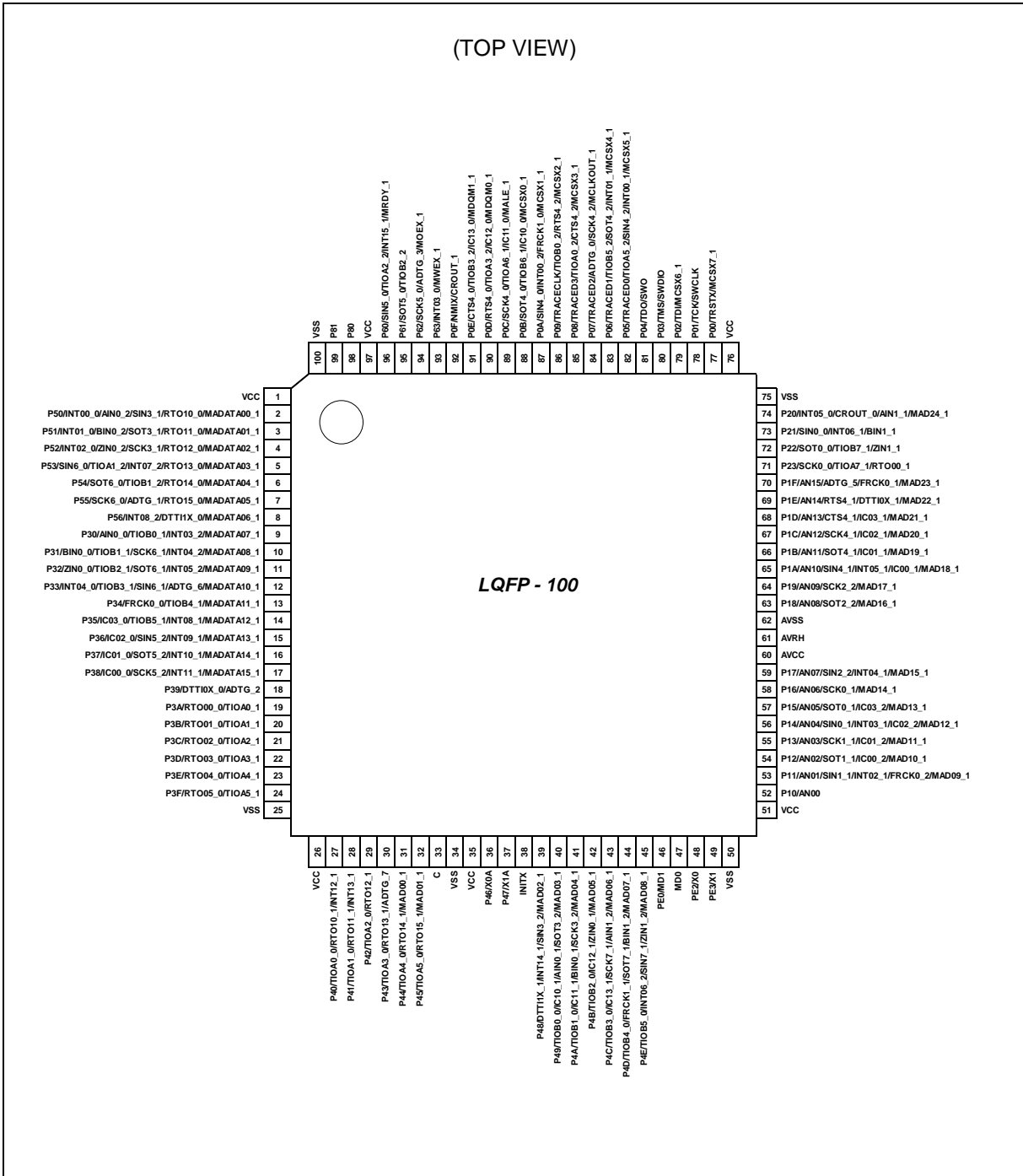
○ : Supported

* : MB9AF115NA and MB9AF116NA are in the planning stage.

Note : Refer to "■PACKAGE DIMENSIONS" for detailed information on each package.

■ PIN ASSIGNMENT

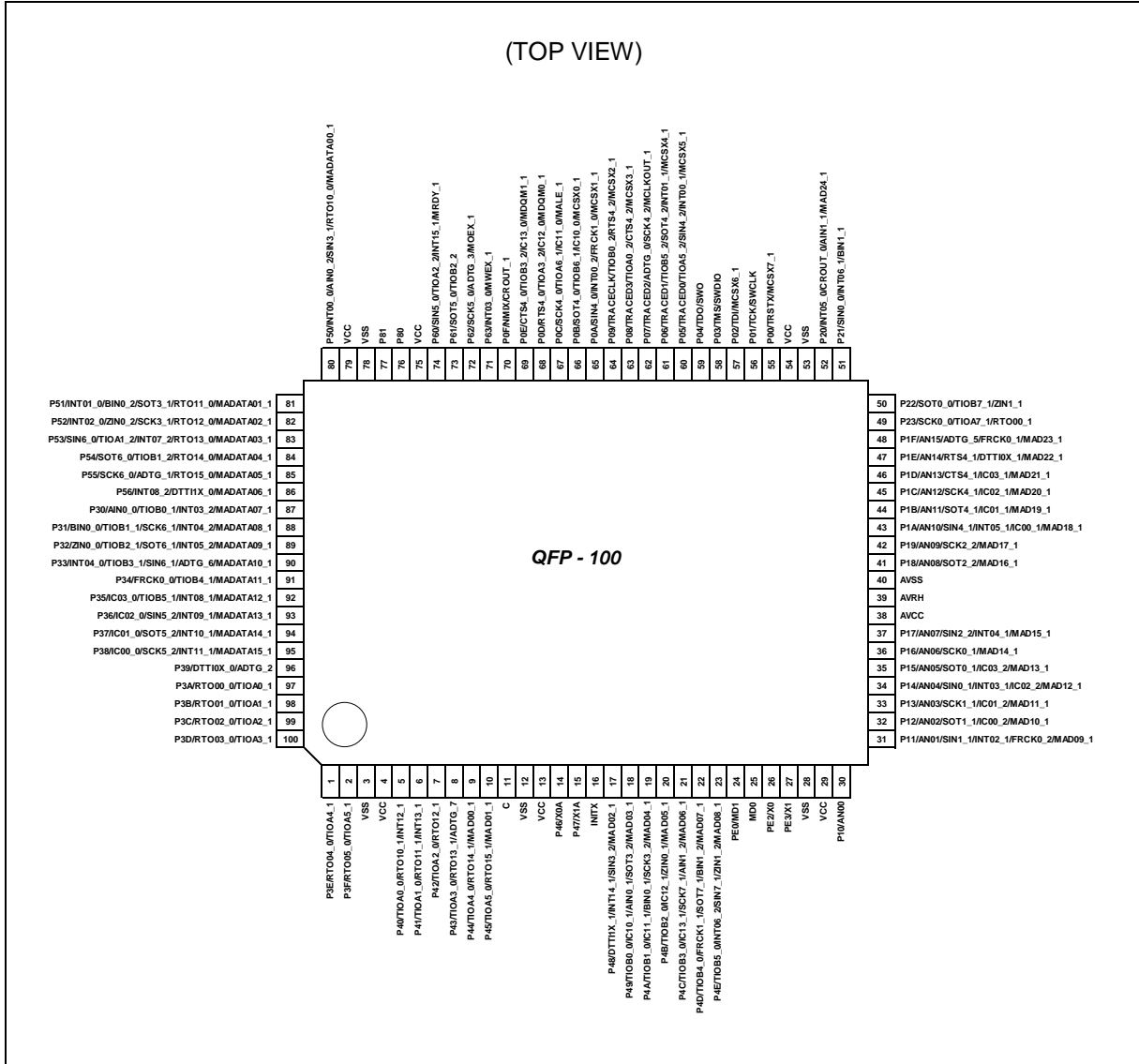
● FPT-100P-M20/M23



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

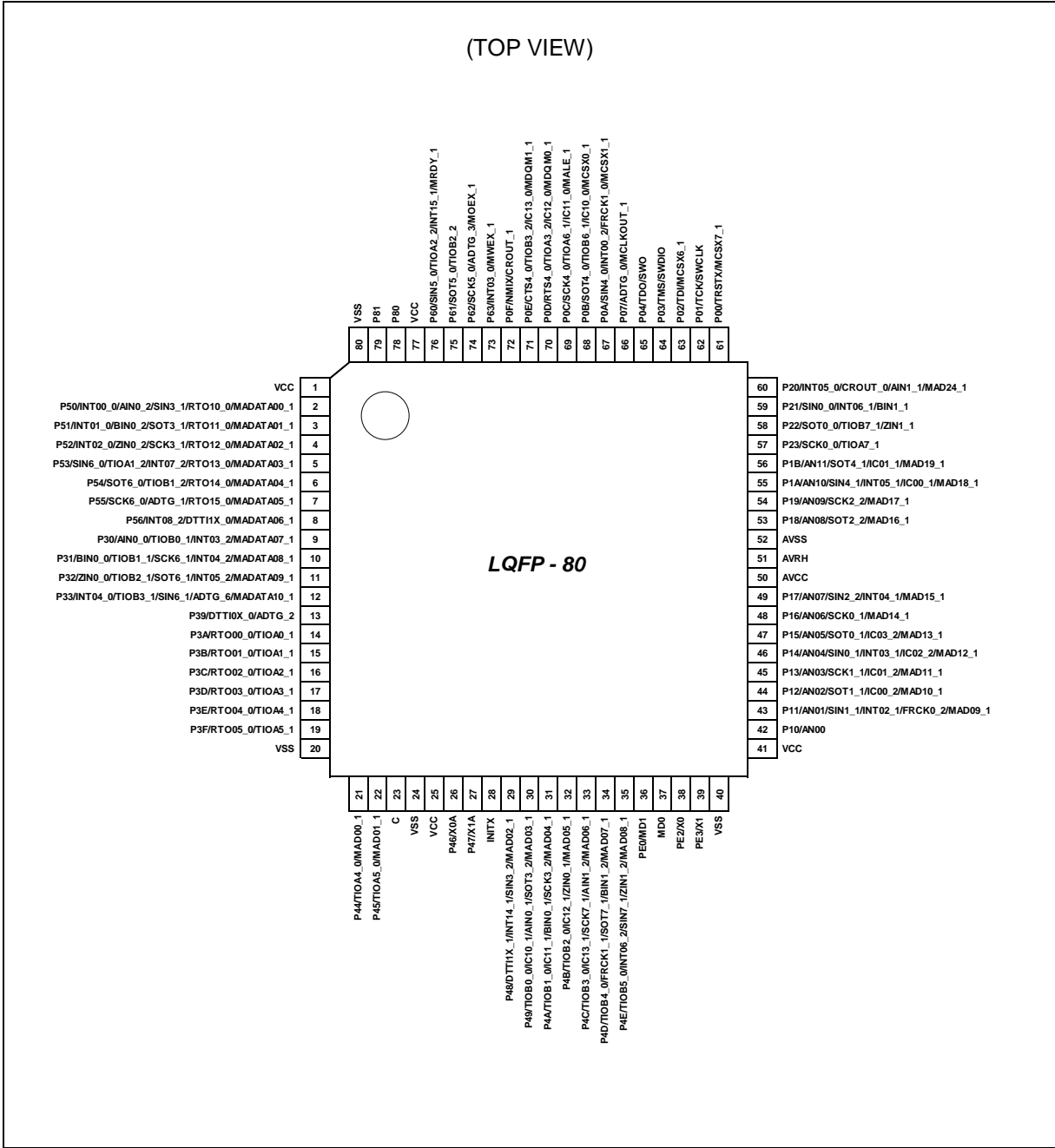
● FPT-100P-M06



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

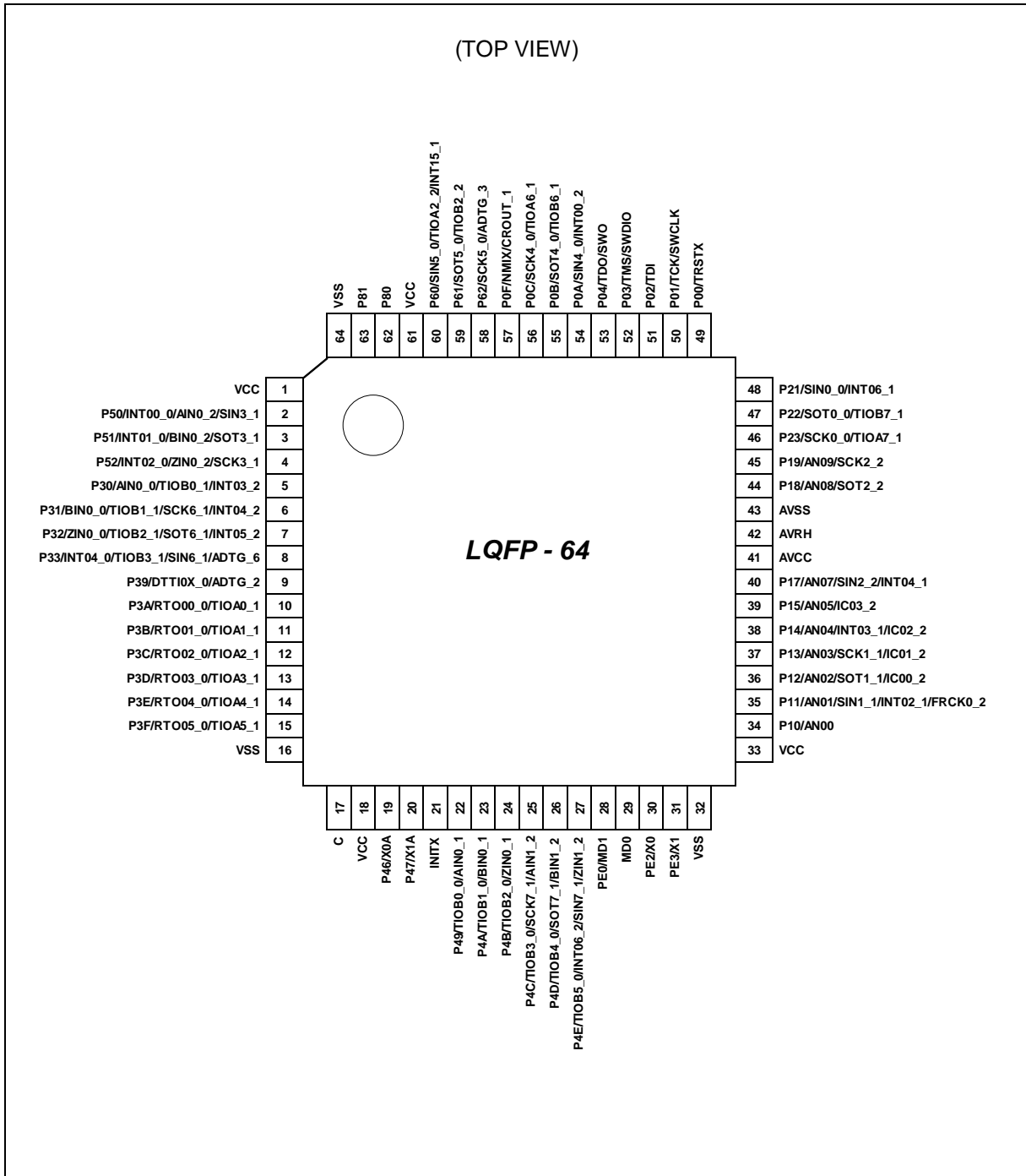
● FPT-80P-M21/FPT-80P-M37



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

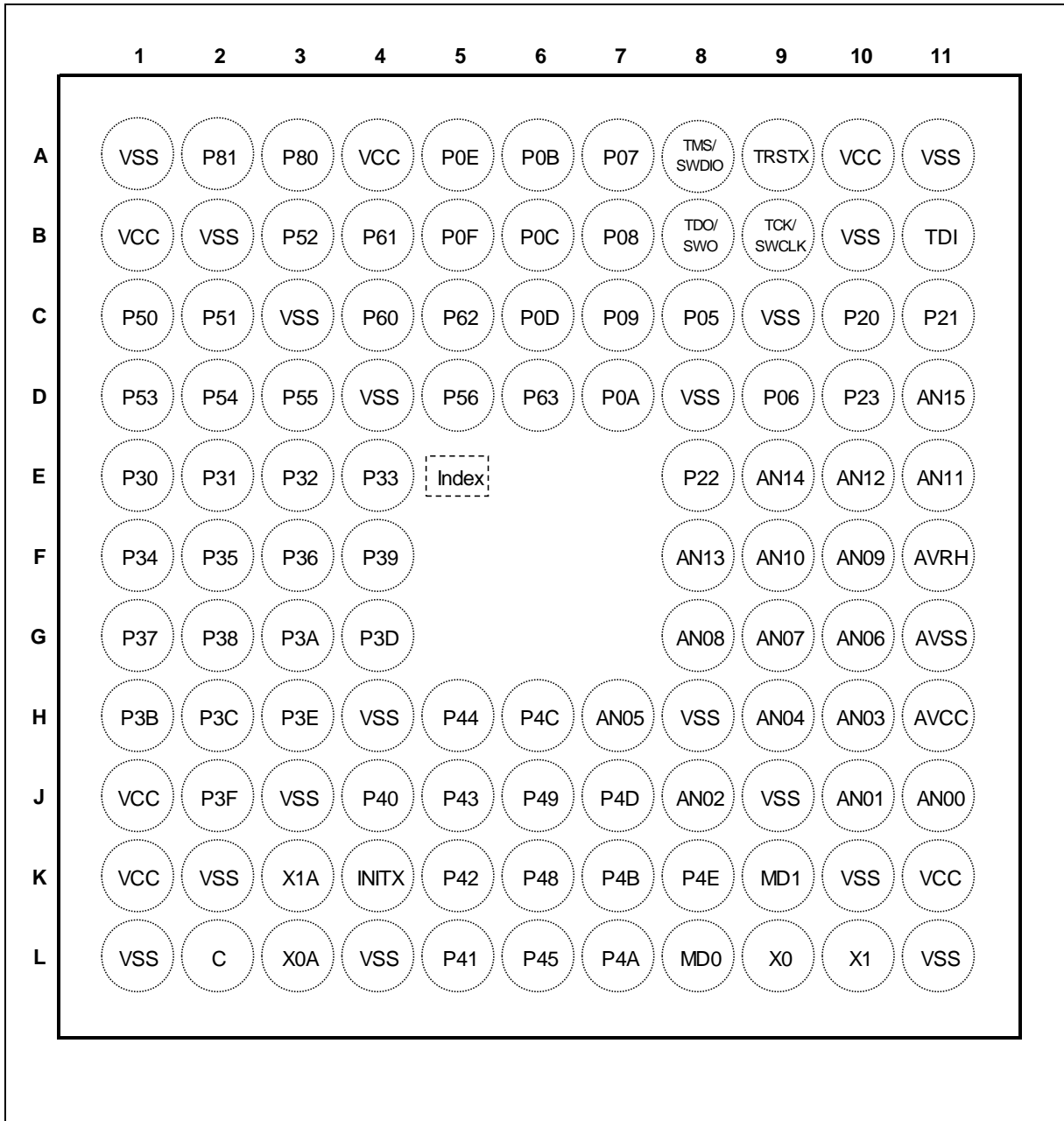
● FPT-64P-M23/M24/M38/M39



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

● BGA-112P-M04



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

■ PIN DESCRIPTION

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin

| Pin No | | | | | Pin name | I/O circuit type | Pin state type |
|----------|---------|---------|---------|-------------------|----------------------|------------------|----------------|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 | | | |
| 1 | 79 | B1 | 1 | 1 | VCC | - | |
| 2 | 80 | C1 | 2 | 2 | P50 | E | H |
| | | | | | INT00_0 | | |
| | | | | | AIN0_2 | | |
| | | | | - | SIN3_1 | | |
| | | | | | RTO10_0 (PPG10_0) | | |
| | | | | | MADATA00_1 | | |
| 3 | 81 | C2 | 3 | 3 | P51 | E | H |
| | | | | | INT01_0 | | |
| | | | | | BIN0_2 | | |
| | | | | - | SOT3_1 (SDA3_1) | | |
| | | | | | RTO11_0 (PPG10_0) | | |
| | | | | | MADATA01_1 | | |
| 4 | 82 | B3 | 4 | 4 | P52 | E | H |
| | | | | | INT02_0 | | |
| | | | | | ZIN0_2 | | |
| | | | | - | SCK3_1 (SCL3_1) | | |
| | | | | | RTO12_0 (PPG12_0) | | |
| | | | | | MADATA02_1 | | |
| 5 | 83 | D1 | 5 | - | P53 | E | H |
| | | | | | SIN6_0 | | |
| | | | | | TIOA1_2 | | |
| | | | | | INT07_2 | | |
| | | | | | RTO13_0 (PPG12_0) | | |
| | | | | | MADATA03_1 | | |
| 6 | 84 | D2 | 6 | - | P54 | E | I |
| | | | | | SOT6_0 (SDA6_0) | | |
| | | | | | TIOB1_2 | | |
| | | | | | RTO14_0 (PPG14_0) | | |
| | | | | | MADATA04_1 | | |

| Pin No | | | | | Pin name | I/O circuit type | Pin state type |
|----------|---------|---------|---------|-------------------|----------------------|------------------|----------------|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 | | | |
| 7 | 85 | D3 | 7 | - | P55 | E | I |
| | | | | | SCK6_0 (SCL6_0) | | |
| | | | | | ADTG_1 | | |
| | | | | | RTO15_0 (PPG14_0) | | |
| | | | | | MADATA05_1 | | |
| 8 | 86 | D5 | 8 | - | P56 | E | H |
| | | | | | INT08_2 | | |
| | | | | | DTT11X_0 | | |
| | | | | | MADATA06_1 | | |
| 9 | 87 | E1 | 9 | 5 | P30 | E | H |
| | | | | | AIN0_0 | | |
| | | | | | TIOB0_1 | | |
| | | | | INT03_2 | | | |
| | | | | - | MADATA07_1 | | |
| 10 | 88 | E2 | 10 | 6 | P31 | E | H |
| | | | | | BIN0_0 | | |
| | | | | | TIOB1_1 | | |
| | | | | | SCK6_1 (SCL6_1) | | |
| | | | | INT04_2 | | | |
| | | | | - | MADATA08_1 | | |
| 11 | 89 | E3 | 11 | 7 | P32 | E | H |
| | | | | | ZIN0_0 | | |
| | | | | | TIOB2_1 | | |
| | | | | | SOT6_1 (SDA6_1) | | |
| | | | | INT05_2 | | | |
| | | | | - | MADATA09_1 | | |
| 12 | 90 | E4 | 12 | 8 | P33 | E | H |
| | | | | | INT04_0 | | |
| | | | | | TIOB3_1 | | |
| | | | | | SIN6_1 | | |
| | | | | ADTG_6 | | | |
| | | | | - | MADATA10_1 | | |
| 13 | 91 | F1 | - | - | P34 | E | I |
| | | | | | FRCK0_0 | | |
| | | | | | TIOB4_1 | | |
| | | | | | MADATA11_1 | | |

| Pin No | | | | | Pin name | I/O circuit type | Pin state type |
|----------|---------|---------|---------|-------------------|----------------------|------------------|----------------|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 | | | |
| 14 | 92 | F2 | - | - | P35 | E | H |
| | | | | | IC03_0 | | |
| | | | | | TIOB5_1 | | |
| | | | | | INT08_1 | | |
| | | | | | MADATA12_1 | | |
| 15 | 93 | F3 | - | - | P36 | E | H |
| | | | | | IC02_0 | | |
| | | | | | SIN5_2 | | |
| | | | | | INT09_1 | | |
| | | | | | MADATA13_1 | | |
| 16 | 94 | G1 | - | - | P37 | E | H |
| | | | | | IC01_0 | | |
| | | | | | SOT5_2 (SDA5_2) | | |
| | | | | | INT10_1 | | |
| | | | | | MADATA14_1 | | |
| 17 | 95 | G2 | - | - | P38 | E | H |
| | | | | | IC00_0 | | |
| | | | | | SCK5_2 (SCL5_2) | | |
| | | | | | INT11_1 | | |
| | | | | | MADATA15_1 | | |
| 18 | 96 | F4 | 13 | 9 | P39 | E | I |
| | | | | | DTTIOX_0 | | |
| | | | | | ADTG_2 | | |
| 19 | 97 | G3 | 14 | 10 | P3A | G | I |
| | | | | | RTO00_0 (PPG00_0) | | |
| | | | | | TIOA0_1 | | |
| 20 | 98 | H1 | 15 | 11 | P3B | G | I |
| | | | | | RTO01_0 (PPG00_0) | | |
| | | | | | TIOA1_1 | | |
| 21 | 99 | H2 | 16 | 12 | P3C | G | I |
| | | | | | RTO02_0 (PPG02_0) | | |
| | | | | | TIOA2_1 | | |
| 22 | 100 | G4 | 17 | 13 | P3D | G | I |
| | | | | | RTO03_0 (PPG02_0) | | |
| | | | | | TIOA3_1 | | |
| - | - | B2 | - | - | VSS | - | - |

| Pin No | | | | | Pin name | I/O circuit type | Pin state type |
|----------|---------|---------|---------|-------------------|----------------------|------------------|----------------|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 | | | |
| 23 | 1 | H3 | 18 | 14 | P3E | G | I |
| | | | | | RTO04_0 (PPG04_0) | | |
| | | | | | TIOA4_1 | | |
| 24 | 2 | J2 | 19 | 15 | P3F | G | I |
| | | | | | RTO05_0 (PPG04_0) | | |
| | | | | | TIOA5_1 | | |
| 25 | 3 | L1 | 20 | 16 | VSS | - | - |
| 26 | 4 | J1 | - | - | VCC | - | - |
| 27 | 5 | J4 | - | - | P40 | G | H |
| | | | | | TIOA0_0 | | |
| | | | | | RTO10_1 (PPG10_1) | | |
| | | | | | INT12_1 | | |
| 28 | 6 | L5 | - | - | P41 | G | H |
| | | | | | TIOA1_0 | | |
| | | | | | RTO11_1 (PPG10_1) | | |
| | | | | | INT13_1 | | |
| 29 | 7 | K5 | - | - | P42 | G | I |
| | | | | | TIOA2_0 | | |
| | | | | | RTO12_1 (PPG12_1) | | |
| 30 | 8 | J5 | - | - | P43 | G | I |
| | | | | | TIOA3_0 | | |
| | | | | | RTO13_1 (PPG12_1) | | |
| | | | | | ADTG_7 | | |
| 31 | 9 | H5 | 21 | - | P44 | G | I |
| | | | - | | TIOA4_0 | | |
| | | | | | MAD00_1 | | |
| | | | | | RTO14_1 (PPG14_1) | | |
| 32 | 10 | L6 | 22 | - | P45 | G | I |
| | | | - | | TIOA5_0 | | |
| | | | | | MAD01_1 | | |
| | | | | | RTO15_1 (PPG14_1) | | |
| - | - | K2 | - | - | VSS | - | - |
| - | - | J3 | - | - | VSS | - | - |
| - | - | H4 | - | - | VSS | - | - |

| Pin No | | | | | Pin name | I/O circuit type | Pin state type |
|----------|---------|---------|---------|-------------------|--------------------|------------------|----------------|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 | | | |
| 33 | 11 | L2 | 23 | 17 | C | - | |
| 34 | 12 | L4 | 24 | - | VSS | - | |
| 35 | 13 | K1 | 25 | 18 | VCC | - | |
| 36 | 14 | L3 | 26 | 19 | P46 | D | M |
| | | | | | X0A | | |
| 37 | 15 | K3 | 27 | 20 | P47 | D | N |
| | | | | | X1A | | |
| 38 | 16 | K4 | 28 | 21 | INITX | B | C |
| 39 | 17 | K6 | 29 | - | P48 | E | H |
| | | | | | DTT1X_1 | | |
| | | | | | INT14_1 | | |
| | | | | | SIN3_2 | | |
| | | | | | MAD02_1 | | |
| 40 | 18 | J6 | 30 | 22 | P49 | E | I |
| | | | | | TIOB0_0 | | |
| | | | | - | AIN0_1 | | |
| | | | | | IC10_1 | | |
| | | | | | SOT3_2 (SDA3_2) | | |
| | | | | | MAD03_1 | | |
| 41 | 19 | L7 | 31 | 23 | P4A | E | I |
| | | | | | TIOB1_0 | | |
| | | | | - | BIN0_1 | | |
| | | | | | IC11_1 | | |
| | | | | | SCK3_2 (SCL3_2) | | |
| | | | | | MAD04_1 | | |
| 42 | 20 | K7 | 32 | 24 | P4B | E | I |
| | | | | | TIOB2_0 | | |
| | | | | - | ZIN0_1 | | |
| | | | | | IC12_1 | | |
| | | | | | MAD05_1 | | |
| 43 | 21 | H6 | 33 | 25 | P4C | E / I* | I |
| | | | | | TIOB3_0 | | |
| | | | | | SCK7_1 (SCL7_1) | | |
| | | | | - | AIN1_2 | | |
| | | | | | IC13_1 | | |
| | | | | | MAD06_1 | | |

| Pin No | | | | | Pin name | I/O circuit type | Pin state type |
|----------|---------|---------|---------|-------------------|--------------------|------------------|----------------|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 | | | |
| 44 | 22 | J7 | 34 | 26 | P4D | E / I* | I |
| | | | | | TIOB4_0 | | |
| | | | | | SOT7_1 (SDA7_1) | | |
| | | | | - | BIN1_2 | | |
| | | | | | FRCK1_1 | | |
| | | | | | MAD07_1 | | |
| 45 | 23 | K8 | 35 | 27 | P4E | E / I* | I |
| | | | | | TIOB5_0 | | |
| | | | | | INT06_2 | | |
| | | | | | SIN7_1 | | |
| | | | | | ZIN1_2 | | |
| | | | | - | MAD08_1 | | |
| 46 | 24 | K9 | 36 | 28 | MD1 | C | P |
| | | | | | PE0 | | |
| 47 | 25 | L8 | 37 | 29 | MD0 | J | D |
| 48 | 26 | L9 | 38 | 30 | X0 | A | A |
| | | | | | PE2 | | |
| 49 | 27 | L10 | 39 | 31 | X1 | A | B |
| | | | | | PE3 | | |
| 50 | 28 | L11 | 40 | 32 | VSS | - | |
| 51 | 29 | K11 | 41 | 33 | VCC | - | |
| 52 | 30 | J11 | 42 | 34 | P10 | F | K |
| | | | | | AN00 | | |
| 53 | 31 | J10 | 43 | 35 | P11 | F | L |
| | | | | | AN01 | | |
| | | | | | SIN1_1 | | |
| | | | | | INT02_1 | | |
| | | | | | FRCK0_2 | | |
| | | | | - | MAD09_1 | | |
| 54 | 32 | J8 | 44 | 36 | P12 | F | K |
| | | | | | AN02 | | |
| | | | | | SOT1_1 (SDA1_1) | | |
| | | | | | IC00_2 | | |
| | | | | | - | | |
| | | | | - | - | | |
| - | - | J9 | - | - | VSS | - | |

| Pin No | | | | | Pin name | I/O circuit type | Pin state type |
|----------|---------|---------|---------|-------------------|--------------------|------------------|----------------|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 | | | |
| 55 | 33 | H10 | 45 | 37 | P13 | F | K |
| | | | | | AN03 | | |
| | | | | | SCK1_1 (SCL1_1) | | |
| | | | | IC01_2 | | | |
| | | | | - | MAD11_1 | | |
| 56 | 34 | H9 | 46 | 38 | P14 | F | L |
| | | | | | AN04 | | |
| | | | | | INT03_1 | | |
| | | | | | IC02_2 | | |
| | | | | - | SIN0_1 | | |
| | | | | - | MAD12_1 | | |
| 57 | 35 | H7 | 47 | 39 | P15 | F | K |
| | | | | | AN05 | | |
| | | | | | IC03_2 | | |
| | | | | - | SOT0_1 (SDA0_1) | | |
| | | | | - | MAD13_1 | | |
| 58 | 36 | G10 | 48 | - | P16 | F | K |
| | | | | | AN06 | | |
| | | | | | SCK0_1 (SCL0_1) | | |
| | | | | | MAD14_1 | | |
| 59 | 37 | G9 | 49 | 40 | P17 | F | L |
| | | | | | AN07 | | |
| | | | | | SIN2_2 | | |
| | | | | | INT04_1 | | |
| | | | | - | MAD15_1 | | |
| 60 | 38 | H11 | 50 | 41 | AVCC | - | |
| 61 | 39 | F11 | 51 | 42 | AVRH | - | |
| 62 | 40 | G11 | 52 | 43 | AVSS | - | |
| 63 | 41 | G8 | 53 | 44 | P18 | F | K |
| | | | | | AN08 | | |
| | | | | | SOT2_2 (SDA2_2) | | |
| | | | | - | MAD16_1 | | |
| 64 | 42 | F10 | 54 | 45 | P19 | F | K |
| | | | | | AN09 | | |
| | | | | | SCK2_2 (SCL2_2) | | |
| | | | | - | MAD17_1 | | |
| - | - | H8 | - | - | VSS | - | |

| Pin No | | | | | Pin name | I/O circuit type | Pin state type |
|----------|---------|---------|---------|-------------------|--------------------|------------------|----------------|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 | | | |
| 65 | 43 | F9 | 55 | - | P1A | F | L |
| | | | | | AN10 | | |
| | | | | | SIN4_1 | | |
| | | | | | INT05_1 | | |
| | | | | | IC00_1 | | |
| | | | | | MAD18_1 | | |
| 66 | 44 | E11 | 56 | - | P1B | F | K |
| | | | | | AN11 | | |
| | | | | | SOT4_1 (SDA4_1) | | |
| | | | | | IC01_1 | | |
| | | | | | MAD19_1 | | |
| 67 | 45 | E10 | - | - | P1C | F | K |
| | | | | | AN12 | | |
| | | | | | SCK4_1 (SCL4_1) | | |
| | | | | | IC02_1 | | |
| | | | | | MAD20_1 | | |
| 68 | 46 | F8 | - | - | P1D | F | K |
| | | | | | AN13 | | |
| | | | | | CTS4_1 | | |
| | | | | | IC03_1 | | |
| | | | | | MAD21_1 | | |
| 69 | 47 | E9 | - | - | P1E | F | K |
| | | | | | AN14 | | |
| | | | | | RTS4_1 | | |
| | | | | | DTTIOX_1 | | |
| | | | | | MAD22_1 | | |
| 70 | 48 | D11 | - | - | P1F | F | K |
| | | | | | AN15 | | |
| | | | | | ADTG_5 | | |
| | | | | | FRCK0_1 | | |
| | | | | | MAD23_1 | | |
| - | - | B10 | - | - | VSS | - | - |
| - | - | C9 | - | - | VSS | - | - |

| Pin No | | | | | Pin name | I/O circuit type | Pin state type |
|----------|---------|---------|---------|-------------------|----------------------|------------------|----------------|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 | | | |
| 71 | 49 | D10 | 57 | 46 | P23 | E | I |
| | | | | | SCK0_0 (SCL0_0) | | |
| | | | TIOA7_1 | | | | |
| | | | - | - | RTO00_1 (PPG00_1) | | |
| 72 | 50 | E8 | 58 | 47 | P22 | E | I |
| | | | | | SOT0_0 (SDA0_0) | | |
| | | | | TIOB7_1 | | | |
| | | | | - | ZIN1_1 | | |
| 73 | 51 | C11 | 59 | 48 | P21 | E | H |
| | | | | | SIN0_0 | | |
| | | | | INT06_1 | | | |
| | | | | - | BIN1_1 | | |
| 74 | 52 | C10 | 60 | | P20 | E | H |
| | | | | | INT05_0 | | |
| | | | | | CROUT_0 | | |
| | | | | | AIN1_1 | | |
| | | | | | MAD24_1 | | |
| 75 | 53 | A11 | - | - | VSS | - | |
| 76 | 54 | A10 | - | - | VCC | - | |
| 77 | 55 | A9 | 61 | 49 | P00 | E | E |
| | | | | | TRSTX | | |
| | | | | - | MCSX7_1 | | |
| 78 | 56 | B9 | 62 | 50 | P01 | E | E |
| | | | | | TCK | | |
| | | | | | SWCLK | | |
| 79 | 57 | B11 | 63 | 51 | P02 | E | E |
| | | | | | TDI | | |
| | | | | | - | | |
| 80 | 58 | A8 | 64 | 52 | P03 | E | E |
| | | | | | TMS | | |
| | | | | | SWDIO | | |
| 81 | 59 | B8 | 65 | 53 | P04 | E | E |
| | | | | | TDO | | |
| | | | | | SWO | | |
| 82 | 60 | C8 | | | P05 | E | F |
| | | | | | TRACED0 | | |
| | | | | | TIOA5_2 | | |
| | | | | | SIN4_2 | | |
| | | | | | INT00_1 | | |
| | | | | | MCSX5_1 | | |
| - | - | D8 | - | - | VSS | - | |

| Pin No | | | | | Pin name | I/O circuit type | Pin state type |
|----------|---------|---------|---------|-------------------|--------------------|------------------|--------------------|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 | | | |
| 83 | 61 | D9 | - | - | P06 | E | F |
| | | | | | TRACED1 | | |
| | | | | | TIOB5_2 | | |
| | | | | | SOT4_2 (SDA4_2) | | |
| | | | | | INT01_1 | | |
| | | | | | MCSX4_1 | | |
| 84 | 62 | A7 | 66 | - | P07 | E | G |
| | | | - | | ADTG_0 | | |
| | | | | | MCLKOUT_1 | | |
| | | | | | TRACED2 | | |
| | | | | | SCK4_2 (SCL4_2) | | |
| 85 | 63 | B7 | - | - | P08 | E | G |
| | | | | | TRACED3 | | |
| | | | | | TIOA0_2 | | |
| | | | | | CTS4_2 | | |
| | | | | | MCSX3_1 | | |
| 86 | 64 | C7 | - | - | P09 | E | G |
| | | | | | TRACECLK | | |
| | | | | | TIOB0_2 | | |
| | | | | | RTS4_2 | | |
| | | | | | MCSX2_1 | | |
| 87 | 65 | D7 | 67 | 54 | E / I* | H | |
| | | | | - | | | P0A |
| | | | | | | | SIN4_0 |
| | | | | | | | INT00_2 |
| | | | | | | | FRCK1_0 |
| MCSX1_1 | | | | | | | |
| 88 | 66 | A6 | 68 | 55 | E / I* | I | |
| | | | | - | | | P0B |
| | | | | | | | SOT4_0 (SDA4_0) |
| | | | | | | | TIOB6_1 |
| | | | | | | | IC10_0 |
| MCSX0_1 | | | | | | | |
| 89 | 67 | B6 | 69 | 56 | E / I* | I | |
| | | | | - | | | P0C |
| | | | | | | | SCK4_0 (SCL4_0) |
| | | | | | | | TIOA6_1 |
| | | | | | | | IC11_0 |
| MALE_1 | | | | | | | |
| - | - | D4 | - | - | VSS | - | |
| - | - | C3 | - | - | VSS | - | |

| Pin No | | | | | Pin name | I/O circuit type | Pin state type |
|----------|---------|---------|---------|-------------------|--------------------|------------------|----------------|
| LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 | | | |
| 90 | 68 | C6 | 70 | - | P0D | E | I |
| | | | | | RTS4_0 | | |
| | | | | | TIOA3_2 | | |
| | | | | | IC12_0 | | |
| | | | | | MDQM0_1 | | |
| 91 | 69 | A5 | 71 | - | P0E | E | I |
| | | | | | CTS4_0 | | |
| | | | | | TIOB3_2 | | |
| | | | | | IC13_0 | | |
| | | | | | MDQM1_1 | | |
| 92 | 70 | B5 | 72 | 57 | P0F | E | J |
| | | | | | NMIX | | |
| | | | | | CROUT_1 | | |
| 93 | 71 | D6 | 73 | - | P63 | E | H |
| | | | | | INT03_0 | | |
| | | | | | MWEX_1 | | |
| 94 | 72 | C5 | 74 | 58 | P62 | E | I |
| | | | | | SCK5_0 (SCL5_0) | | |
| | | | | ADTG_3 | | | |
| | | | | - | MOEX_1 | | |
| 95 | 73 | B4 | 75 | 59 | P61 | E | I |
| | | | | | SOT5_0 (SDA5_0) | | |
| | | | | | TIOB2_2 | | |
| 96 | 74 | C4 | 76 | 60 | P60 | E / I* | H |
| | | | | | SIN5_0 | | |
| | | | | | TIOA2_2 | | |
| | | | | INT15_1 | | | |
| | | | | - | MRDY_1 | | |
| 97 | 75 | A4 | 77 | 61 | VCC | - | |
| 98 | 76 | A3 | 78 | 62 | P80 | H | O |
| 99 | 77 | A2 | 79 | 63 | P81 | H | O |
| 100 | 78 | A1 | 80 | 64 | VSS | - | |

* : 5V tolerant I/O on MB9AF115MA/NA and MB9AF116MA/NA

■ SIGNAL DESCRIPTION

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

| Module | Pin name | Function | Pin No | | | | |
|--------------|----------|--|----------|---------|---------|---------|----------------|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 |
| ADC | ADTG_0 | A/D converter external trigger input pin | 84 | 62 | A7 | 66 | - |
| | ADTG_1 | | 7 | 85 | D3 | 7 | - |
| | ADTG_2 | | 18 | 96 | F4 | 13 | 9 |
| | ADTG_3 | | 94 | 72 | C5 | 74 | 58 |
| | ADTG_4 | | - | - | - | - | - |
| | ADTG_5 | | 70 | 48 | D11 | - | - |
| | ADTG_6 | | 12 | 90 | E4 | 12 | 8 |
| | ADTG_7 | | 30 | 8 | J5 | - | - |
| | ADTG_8 | | - | - | - | - | - |
| | AN00 | A/D converter analog input pin. ANxx describes ADC ch.xx. | 52 | 30 | J11 | 42 | 34 |
| | AN01 | | 53 | 31 | J10 | 43 | 35 |
| | AN02 | | 54 | 32 | J8 | 44 | 36 |
| | AN03 | | 55 | 33 | H10 | 45 | 37 |
| | AN04 | | 56 | 34 | H9 | 46 | 38 |
| | AN05 | | 57 | 35 | H7 | 47 | 39 |
| | AN06 | | 58 | 36 | G10 | 48 | - |
| | AN07 | | 59 | 37 | G9 | 49 | 40 |
| | AN08 | | 63 | 41 | G8 | 53 | 44 |
| | AN09 | | 64 | 42 | F10 | 54 | 45 |
| | AN10 | | 65 | 43 | F9 | 55 | - |
| AN11 | 66 | | 44 | E11 | 56 | - | |
| AN12 | 67 | | 45 | E10 | - | - | |
| AN13 | 68 | | 46 | F8 | - | - | |
| AN14 | 69 | | 47 | E9 | - | - | |
| AN15 | 70 | | 48 | D11 | - | - | |
| Base Timer 0 | TIOA0_0 | Base timer ch.0 TIOA pin | 27 | 5 | J4 | - | - |
| | TIOA0_1 | | 19 | 97 | G3 | 14 | 10 |
| | TIOA0_2 | | 85 | 63 | B7 | - | - |
| | TIOB0_0 | Base timer ch.0 TIOB pin | 40 | 18 | J6 | 30 | 22 |
| | TIOB0_1 | | 9 | 87 | E1 | 9 | 5 |
| | TIOB0_2 | | 86 | 64 | C7 | - | - |
| Base Timer 1 | TIOA1_0 | Base timer ch.1 TIOA pin | 28 | 6 | L5 | - | - |
| | TIOA1_1 | | 20 | 98 | H1 | 15 | 11 |
| | TIOA1_2 | | 5 | 83 | D1 | 5 | - |
| | TIOB1_0 | Base timer ch.1 TIOB pin | 41 | 19 | L7 | 31 | 23 |
| | TIOB1_1 | | 10 | 88 | E2 | 10 | 6 |
| | TIOB1_2 | | 6 | 84 | D2 | 6 | - |

| Module | Pin name | Function | Pin No | | | | |
|--------------|----------|--------------------------|----------|---------|---------|---------|----------------|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 |
| Base Timer 2 | TIOA2_0 | Base timer ch.2 TIOA pin | 29 | 7 | K5 | - | - |
| | TIOA2_1 | | 21 | 99 | H2 | 16 | 12 |
| | TIOA2_2 | | 96 | 74 | C4 | 76 | 60 |
| | TIOB2_0 | Base timer ch.2 TIOB pin | 42 | 20 | K7 | 32 | 24 |
| | TIOB2_1 | | 11 | 89 | E3 | 11 | 7 |
| | TIOB2_2 | | 95 | 73 | B4 | 75 | 59 |
| Base Timer 3 | TIOA3_0 | Base timer ch.3 TIOA pin | 30 | 8 | J5 | - | - |
| | TIOA3_1 | | 22 | 100 | G4 | 17 | 13 |
| | TIOA3_2 | | 90 | 68 | C6 | 70 | - |
| | TIOB3_0 | Base timer ch.3 TIOB pin | 43 | 21 | H6 | 33 | 25 |
| | TIOB3_1 | | 12 | 90 | E4 | 12 | 8 |
| | TIOB3_2 | | 91 | 69 | A5 | 71 | - |
| Base Timer 4 | TIOA4_0 | Base timer ch.4 TIOA pin | 31 | 9 | H5 | 21 | - |
| | TIOA4_1 | | 23 | 1 | H3 | 18 | 14 |
| | TIOA4_2 | | - | - | - | - | - |
| | TIOB4_0 | Base timer ch.4 TIOB pin | 44 | 22 | J7 | 34 | 26 |
| | TIOB4_1 | | 13 | 91 | F1 | - | - |
| | TIOB4_2 | | - | - | - | - | - |
| Base Timer 5 | TIOA5_0 | Base timer ch.5 TIOA pin | 32 | 10 | L6 | 22 | - |
| | TIOA5_1 | | 24 | 2 | J2 | 19 | 15 |
| | TIOA5_2 | | 82 | 60 | C8 | - | - |
| | TIOB5_0 | Base timer ch.5 TIOB pin | 45 | 23 | K8 | 35 | 27 |
| | TIOB5_1 | | 14 | 92 | F2 | - | - |
| | TIOB5_2 | | 83 | 61 | D9 | - | - |
| Base Timer 6 | TIOA6_1 | Base timer ch.6 TIOA pin | 89 | 67 | B6 | 69 | 56 |
| | TIOB6_1 | Base timer ch.6 TIOB pin | 88 | 66 | A6 | 68 | 55 |
| Base Timer 7 | TIOA7_0 | Base timer ch.7 TIOA pin | - | - | - | - | - |
| | TIOA7_1 | | 71 | 49 | D10 | 57 | 46 |
| | TIOA7_2 | | - | - | - | - | - |
| | TIOB7_0 | Base timer ch.7 TIOB pin | - | - | - | - | - |
| | TIOB7_1 | | 72 | 50 | E8 | 58 | 47 |
| | TIOB7_2 | | - | - | - | - | - |

| Module | Pin name | Function | Pin No | | | | |
|--------------|----------|---|----------|---------|---------|---------|----------------|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 |
| Debugger | SWCLK | Serial wire debug interface clock input | 78 | 56 | B9 | 62 | 50 |
| | SWDIO | Serial wire debug interface data input / output | 80 | 58 | A8 | 64 | 52 |
| | SWO | Serial wire viewer output | 81 | 59 | B8 | 65 | 53 |
| | TCK | J-TAG test clock input | 78 | 56 | B9 | 62 | 50 |
| | TDI | J-TAG test data input | 79 | 57 | B11 | 63 | 51 |
| | TDO | J-TAG debug data output | 81 | 59 | B8 | 65 | 53 |
| | TMS | J-TAG test mode state input/output | 80 | 58 | A8 | 64 | 52 |
| | TRACECLK | Trace CLK output of ETM | 86 | 64 | C7 | - | - |
| | TRACED0 | Trace data output of ETM | 82 | 60 | C8 | - | - |
| | TRACED1 | | 83 | 61 | D9 | - | - |
| | TRACED2 | | 84 | 62 | A7 | - | - |
| | TRACED3 | | 85 | 63 | B7 | - | - |
| | TRSTX | J-TAG test reset input | 77 | 55 | A9 | 61 | 49 |
| External Bus | MAD00_1 | External bus interface address bus | 31 | 9 | H5 | 21 | - |
| | MAD01_1 | | 32 | 10 | L6 | 22 | - |
| | MAD02_1 | | 39 | 17 | K6 | 29 | - |
| | MAD03_1 | | 40 | 18 | J6 | 30 | - |
| | MAD04_1 | | 41 | 19 | L7 | 31 | - |
| | MAD05_1 | | 42 | 20 | K7 | 32 | - |
| | MAD06_1 | | 43 | 21 | H6 | 33 | - |
| | MAD07_1 | | 44 | 22 | J7 | 34 | - |
| | MAD08_1 | | 45 | 23 | K8 | 35 | - |
| | MAD09_1 | | 53 | 31 | J10 | 43 | - |
| | MAD10_1 | | 54 | 32 | J8 | 44 | - |
| | MAD11_1 | | 55 | 33 | H10 | 45 | - |
| | MAD12_1 | | 56 | 34 | H9 | 46 | - |
| | MAD13_1 | | 57 | 35 | H7 | 47 | - |
| | MAD14_1 | | 58 | 36 | G10 | 48 | - |
| | MAD15_1 | | 59 | 37 | G9 | 49 | - |
| | MAD16_1 | | 63 | 41 | G8 | 53 | - |
| | MAD17_1 | | 64 | 42 | F10 | 54 | - |
| | MAD18_1 | | 65 | 43 | F9 | 55 | - |
| | MAD19_1 | | 66 | 44 | E11 | 56 | - |
| | MAD20_1 | | 67 | 45 | E10 | - | - |
| | MAD21_1 | | 68 | 46 | F8 | - | - |
| | MAD22_1 | | 69 | 47 | E9 | - | - |
| | MAD23_1 | | 70 | 48 | D11 | - | - |
| MAD24_1 | 74 | 52 | C10 | 60 | - | | |

| Module | Pin name | Function | Pin No | | | | |
|--------------|------------|---|---|---------|---------|---------|-------------------|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 |
| External Bus | MCSX0_1 | External bus interface chip select output pin | 88 | 66 | A6 | 68 | - |
| | MCSX1_1 | | 87 | 65 | D7 | 67 | - |
| | MCSX2_1 | | 86 | 64 | C7 | - | - |
| | MCSX3_1 | | 85 | 63 | B7 | - | - |
| | MCSX4_1 | | 83 | 61 | D9 | - | - |
| | MCSX5_1 | | 82 | 60 | C8 | - | - |
| | MCSX6_1 | | 79 | 57 | B11 | 63 | - |
| | MCSX7_1 | | 77 | 55 | A9 | 61 | - |
| | MDQM0_1 | External bus interface byte mask signal output | 90 | 68 | C6 | 70 | - |
| | MDQM1_1 | | 91 | 69 | A5 | 71 | - |
| | MOEX_1 | External bus interface read enable signal for SRAM | 94 | 72 | C5 | 74 | - |
| | MWEX_1 | External bus interface write enable signal for SRAM | 93 | 71 | D6 | 73 | - |
| | MADATA00_1 | External bus interface data bus | 2 | 80 | C1 | 2 | - |
| | MADATA01_1 | | 3 | 81 | C2 | 3 | - |
| | MADATA02_1 | | 4 | 82 | B3 | 4 | - |
| | MADATA03_1 | | 5 | 83 | D1 | 5 | - |
| | MADATA04_1 | | 6 | 84 | D2 | 6 | - |
| | MADATA05_1 | | 7 | 85 | D3 | 7 | - |
| | MADATA06_1 | | 8 | 86 | D5 | 8 | - |
| | MADATA07_1 | | 9 | 87 | E1 | 9 | - |
| | MADATA08_1 | | 10 | 88 | E2 | 10 | - |
| | MADATA09_1 | | 11 | 89 | E3 | 11 | - |
| | MADATA10_1 | | 12 | 90 | E4 | 12 | - |
| | MADATA11_1 | | 13 | 91 | F1 | - | - |
| | MADATA12_1 | | 14 | 92 | F2 | - | - |
| | MADATA13_1 | | 15 | 93 | F3 | - | - |
| | MADATA14_1 | | 16 | 94 | G1 | - | - |
| | MADATA15_1 | | 17 | 95 | G2 | - | - |
| | MALE_1 | | Address Latch enable signal for multiplex | 89 | 67 | B6 | 69 |
| | MRDY_1 | External RDY input signal | 96 | 74 | C4 | 76 | - |
| | MCLKOUT_1 | External bus clock output | 84 | 62 | A7 | 66 | - |

| Module | Pin name | Function | Pin No | | | | |
|--------------------|---|---|----------|---------|---------|---------|-------------------|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 |
| External Interrupt | INT00_0 | External interrupt request 00 input pin | 2 | 80 | C1 | 2 | 2 |
| | INT00_1 | | 82 | 60 | C8 | - | - |
| | INT00_2 | | 87 | 65 | D7 | 67 | 54 |
| | INT01_0 | External interrupt request 01 input pin | 3 | 81 | C2 | 3 | 3 |
| | INT01_1 | | 83 | 61 | D9 | - | - |
| | INT02_0 | External interrupt request 02 input pin | 4 | 82 | B3 | 4 | 4 |
| | INT02_1 | | 53 | 31 | J10 | 43 | 35 |
| | INT03_0 | External interrupt request 03 input pin | 93 | 71 | D6 | 73 | - |
| | INT03_1 | | 56 | 34 | H9 | 46 | 38 |
| | INT03_2 | | 9 | 87 | E1 | 9 | 5 |
| | INT04_0 | External interrupt request 04 input pin | 12 | 90 | E4 | 12 | 8 |
| | INT04_1 | | 59 | 37 | G9 | 49 | 40 |
| | INT04_2 | | 10 | 88 | E2 | 10 | 6 |
| | INT05_0 | External interrupt request 05 input pin | 74 | 52 | C10 | 60 | - |
| | INT05_1 | | 65 | 43 | F9 | 55 | - |
| | INT05_2 | | 11 | 89 | E3 | 11 | 7 |
| | INT06_1 | External interrupt request 06 input pin | 73 | 51 | C11 | 59 | 48 |
| | INT06_2 | | 45 | 23 | K8 | 35 | 27 |
| | INT07_2 | External interrupt request 07 input pin | 5 | 83 | D1 | 5 | - |
| | INT08_1 | External interrupt request 08 input pin | 14 | 92 | F2 | - | - |
| | INT08_2 | | 8 | 86 | D5 | 8 | - |
| | INT09_1 | External interrupt request 09 input pin | 15 | 93 | F3 | - | - |
| | INT10_1 | External interrupt request 10 input pin | 16 | 94 | G1 | - | - |
| INT11_1 | External interrupt request 11 input pin | 17 | 95 | G2 | - | - | |
| INT12_1 | External interrupt request 12 input pin | 27 | 5 | J4 | - | - | |
| INT13_1 | External interrupt request 13 input pin | 28 | 6 | L5 | - | - | |
| INT14_1 | External interrupt request 14 input pin | 39 | 17 | K6 | 29 | - | |
| INT15_1 | External interrupt request 15 input pin | 96 | 74 | C4 | 76 | 60 | |
| NMIX | Non-Maskable Interrupt input | 92 | 70 | B5 | 72 | 57 | |

| Module | Pin name | Function | Pin No | | | | |
|--------|----------------------------|----------------------------|----------|---------|---------|---------|-------------------|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 |
| GPIO | P00 | General-purpose I/O port 0 | 77 | 55 | A9 | 61 | 49 |
| | P01 | | 78 | 56 | B9 | 62 | 50 |
| | P02 | | 79 | 57 | B11 | 63 | 51 |
| | P03 | | 80 | 58 | A8 | 64 | 52 |
| | P04 | | 81 | 59 | B8 | 65 | 53 |
| | P05 | | 82 | 60 | C8 | - | - |
| | P06 | | 83 | 61 | D9 | - | - |
| | P07 | | 84 | 62 | A7 | 66 | - |
| | P08 | | 85 | 63 | B7 | - | - |
| | P09 | | 86 | 64 | C7 | - | - |
| | P0A | | 87 | 65 | D7 | 67 | 54 |
| | P0B | | 88 | 66 | A6 | 68 | 55 |
| | P0C | | 89 | 67 | B6 | 69 | 56 |
| | P0D | | 90 | 68 | C6 | 70 | - |
| | P0E | | 91 | 69 | A5 | 71 | - |
| | P0F | | 92 | 70 | B5 | 72 | 57 |
| | P10 | General-purpose I/O port 1 | 52 | 30 | J11 | 42 | 34 |
| | P11 | | 53 | 31 | J10 | 43 | 35 |
| | P12 | | 54 | 32 | J8 | 44 | 36 |
| | P13 | | 55 | 33 | H10 | 45 | 37 |
| | P14 | | 56 | 34 | H9 | 46 | 38 |
| | P15 | | 57 | 35 | H7 | 47 | 39 |
| | P16 | | 58 | 36 | G10 | 48 | - |
| | P17 | | 59 | 37 | G9 | 49 | 40 |
| | P18 | | 63 | 41 | G8 | 53 | 44 |
| | P19 | | 64 | 42 | F10 | 54 | 45 |
| | P1A | | 65 | 43 | F9 | 55 | - |
| | P1B | | 66 | 44 | E11 | 56 | - |
| | P1C | | 67 | 45 | E10 | - | - |
| | P1D | | 68 | 46 | F8 | - | - |
| P1E | 69 | 47 | E9 | - | - | | |
| P1F | 70 | 48 | D11 | - | - | | |
| P20 | General-purpose I/O port 2 | 74 | 52 | C10 | 60 | - | |
| P21 | | 73 | 51 | C11 | 59 | 48 | |
| P22 | | 72 | 50 | E8 | 58 | 47 | |
| P23 | | 71 | 49 | D10 | 57 | 46 | |

| Module | Pin name | Function | Pin No | | | | |
|--------|----------|----------------------------|----------------------------|---------|---------|---------|-------------------|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 |
| GPIO | P30 | General-purpose I/O port 3 | 9 | 87 | E1 | 9 | 5 |
| | P31 | | 10 | 88 | E2 | 10 | 6 |
| | P32 | | 11 | 89 | E3 | 11 | 7 |
| | P33 | | 12 | 90 | E4 | 12 | 8 |
| | P34 | | 13 | 91 | F1 | - | - |
| | P35 | | 14 | 92 | F2 | - | - |
| | P36 | | 15 | 93 | F3 | - | - |
| | P37 | | 16 | 94 | G1 | - | - |
| | P38 | | 17 | 95 | G2 | - | - |
| | P39 | | 18 | 96 | F4 | 13 | 9 |
| | P3A | | 19 | 97 | G3 | 14 | 10 |
| | P3B | | 20 | 98 | H1 | 15 | 11 |
| | P3C | | 21 | 99 | H2 | 16 | 12 |
| | P3D | | 22 | 100 | G4 | 17 | 13 |
| | P3E | | 23 | 1 | H3 | 18 | 14 |
| | P3F | | 24 | 2 | J2 | 19 | 15 |
| | P40 | | 27 | 5 | J4 | - | - |
| | P41 | | 28 | 6 | L5 | - | - |
| | P42 | | 29 | 7 | K5 | - | - |
| | P43 | | 30 | 8 | J5 | - | - |
| | P44 | | 31 | 9 | H5 | 21 | - |
| | P45 | | 32 | 10 | L6 | 22 | - |
| | P46 | | 36 | 14 | L3 | 26 | 19 |
| | P47 | | 37 | 15 | K3 | 27 | 20 |
| | P48 | 39 | 17 | K6 | 29 | - | |
| | P49 | 40 | 18 | J6 | 30 | 22 | |
| | P4A | 41 | 19 | L7 | 31 | 23 | |
| | P4B | 42 | 20 | K7 | 32 | 24 | |
| | P4C | 43 | 21 | H6 | 33 | 25 | |
| | P4D | 44 | 22 | J7 | 34 | 26 | |
| | P4E | 45 | 23 | K8 | 35 | 27 | |
| | P50 | 2 | General-purpose I/O port 5 | 80 | C1 | 2 | 2 |
| | P51 | 3 | | 81 | C2 | 3 | 3 |
| | P52 | 4 | | 82 | B3 | 4 | 4 |
| | P53 | 5 | | 83 | D1 | 5 | - |
| | P54 | 6 | | 84 | D2 | 6 | - |
| | P55 | 7 | | 85 | D3 | 7 | - |
| | P56 | 8 | | 86 | D5 | 8 | - |
| | P60 | 96 | | 74 | C4 | 76 | 60 |
| | P61 | 95 | 73 | B4 | 75 | 59 | |
| | P62 | 94 | 72 | C5 | 74 | 58 | |
| | P63 | 93 | 71 | D6 | 73 | - | |
| | P80 | 98 | 76 | A3 | 78 | 62 | |
| | P81 | 99 | 77 | A2 | 79 | 63 | |
| | PE0 | 46 | 24 | K9 | 36 | 28 | |
| | PE2 | 48 | 26 | L9 | 38 | 30 | |
| | PE3 | 49 | 27 | L10 | 39 | 31 | |

| Module | Pin name | Function | Pin No | | | | |
|-------------------------|-----------------|---|----------|---------|---------|---------|-------------------|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 |
| Multi Function Serial 0 | SIN0_0 | Multifunction serial interface ch.0 input pin | 73 | 51 | C11 | 59 | 48 |
| | SIN0_1 | | 56 | 34 | H9 | 46 | - |
| | SOT0_0 (SDA0_0) | Multifunction serial interface ch.0 output pin. | 72 | 50 | E8 | 58 | 47 |
| | SOT0_1 (SDA0_1) | This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I ² C (operation mode 4). | 57 | 35 | H7 | 47 | - |
| | SCK0_0 (SCL0_0) | Multifunction serial interface ch.0 clock I/O pin. | 71 | 49 | D10 | 57 | 46 |
| | SCK0_1 (SCL0_1) | This pin operates as SCK0 when it is used in a CSIO (operation mode 2) and as SCL0 when it is used in an I ² C (operation mode 4). | 58 | 36 | G10 | 48 | - |
| Multi Function Serial 1 | SIN1_1 | Multifunction serial interface ch.1 input pin | 53 | 31 | J10 | 43 | 35 |
| | SOT1_1 (SDA1_1) | Multifunction serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I ² C (operation mode 4). | 54 | 32 | J8 | 44 | 36 |
| | SCK1_1 (SCL1_1) | Multifunction serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation mode 2) and as SCL1 when it is used in an I ² C (operation mode 4). | 55 | 33 | H10 | 45 | 37 |

| Module | Pin name | Function | Pin No | | | | |
|-------------------------|--------------------|---|----------|---------|---------|---------|-------------------|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 |
| Multi Function Serial 2 | SIN2_2 | Multifunction serial interface ch.2 input pin | 59 | 37 | G9 | 49 | 40 |
| | SOT2_2 (SDA2_2) | Multifunction serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I ² C (operation mode 4). | 63 | 41 | G8 | 53 | 44 |
| | SCK2_2 (SCL2_2) | Multifunction serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a CSIO (operation mode 2) and as SCL2 when it is used in an I ² C (operation mode 4). | 64 | 42 | F10 | 54 | 45 |
| Multi Function Serial 3 | SIN3_1 | Multifunction serial interface ch.3 input pin | 2 | 80 | C1 | 2 | 2 |
| | SIN3_2 | | 39 | 17 | K6 | 29 | - |
| | SOT3_1 (SDA3_1) | Multifunction serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I ² C (operation mode 4). | 3 | 81 | C2 | 3 | 3 |
| | SOT3_2 (SDA3_2) | 40 | 18 | J6 | 30 | - | |
| | SCK3_1 (SCL3_1) | Multifunction serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a CSIO (operation mode 2) and as SCL3 when it is used in an I ² C (operation mode 4). | 4 | 82 | B3 | 4 | 4 |
| | SCK3_2 (SCL3_2) | 41 | 19 | L7 | 31 | - | |

| Module | Pin name | Function | Pin No | | | | |
|-------------------------|-----------------|---|----------|---------|---------|---------|----------------|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 |
| Multi Function Serial 4 | SIN4_0 | Multifunction serial interface ch.4 input pin | 87 | 65 | D7 | 67 | 54 |
| | SIN4_1 | | 65 | 43 | F9 | 55 | - |
| | SIN4_2 | | 82 | 60 | C8 | - | - |
| | SOT4_0 (SDA4_0) | Multifunction serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I ² C (operation mode 4). | 88 | 66 | A6 | 68 | 55 |
| | SOT4_1 (SDA4_1) | | 66 | 44 | E11 | 56 | - |
| | SOT4_2 (SDA4_2) | | 83 | 61 | D9 | - | - |
| | SCK4_0 (SCL4_0) | Multifunction serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a CSIO (operation mode 2) and as SCL4 when it is used in an I ² C (operation mode 4). | 89 | 67 | B6 | 69 | 56 |
| | SCK4_1 (SCL4_1) | | 67 | 45 | E10 | - | - |
| | SCK4_2 (SCL4_2) | | 84 | 62 | A7 | - | - |
| | RTS4_0 | Multifunction serial interface ch.4 RTS output pin | 90 | 68 | C6 | 70 | - |
| | RTS4_1 | | 69 | 47 | E9 | - | - |
| | RTS4_2 | | 86 | 64 | C7 | - | - |
| | CTS4_0 | Multifunction serial interface ch.4 CTS input pin | 91 | 69 | A5 | 71 | - |
| | CTS4_1 | | 68 | 46 | F8 | - | - |
| | CTS4_2 | | 85 | 63 | B7 | - | - |
| Multi Function Serial 5 | SIN5_0 | Multifunction serial interface ch.5 input pin | 96 | 74 | C4 | 76 | 60 |
| | SIN5_2 | | 15 | 93 | F3 | - | - |
| | SOT5_0 (SDA5_0) | Multifunction serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I ² C (operation mode 4). | 95 | 73 | B4 | 75 | 59 |
| | SOT5_2 (SDA5_2) | | 16 | 94 | G1 | - | - |
| | SCK5_0 (SCL5_0) | Multifunction serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I ² C (operation mode 4). | 94 | 72 | C5 | 74 | 58 |
| | SCK5_2 (SCL5_2) | | 17 | 95 | G2 | - | - |

| Module | Pin name | Function | Pin No | | | | |
|-------------------------|-----------------|---|----------|---------|---------|---------|-------------------|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 |
| Multi Function Serial 6 | SIN6_0 | Multifunction serial interface ch.6 input pin | 5 | 83 | D1 | 5 | - |
| | SIN6_1 | | 12 | 90 | E4 | 12 | 8 |
| | SOT6_0 (SDA6_0) | Multifunction serial interface ch.6 output pin. | 6 | 84 | D2 | 6 | - |
| | SOT6_1 (SDA6_1) | This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I ² C (operation mode 4). | 11 | 89 | E3 | 11 | 7 |
| | SCK6_0 (SCL6_0) | Multifunction serial interface ch.6 clock I/O pin. | 7 | 85 | D3 | 7 | - |
| | SCK6_1 (SCL6_1) | This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I ² C (operation mode 4). | 10 | 88 | E2 | 10 | 6 |
| Multi Function Serial 7 | SIN7_1 | Multifunction serial interface ch.7 input pin | 45 | 23 | K8 | 35 | 27 |
| | SOT7_1 (SDA7_1) | Multifunction serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I ² C (operation mode 4). | 44 | 22 | J7 | 34 | 26 |
| | SCK7_1 (SCL7_1) | Multifunction serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a CSIO (operation mode 2) and as SCL7 when it is used in an I ² C (operation mode 4). | 43 | 21 | H6 | 33 | 25 |

| Module | Pin name | Function | Pin No | | | | | |
|------------------------|-------------------|--|--|---------|---------|---------|-------------------|----|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 | |
| Multi Function Timer 0 | DTTIOX_0 | Input signal of waveform generator to control outputs RTO00 to RTO05 of multi-function timer 0 | 18 | 96 | F4 | 13 | 9 | |
| | DTTIOX_1 | | 69 | 47 | E9 | - | - | |
| | FRCK0_0 | 16-bit free-run timer external clock input pin | 13 | 91 | F1 | - | - | |
| | FRCK0_1 | | 70 | 48 | D11 | - | - | |
| | FRCK0_2 | | 53 | 31 | J10 | 43 | 35 | |
| | IC00_0 | 16-bit input capture input pin of multi-function timer 0. ICxx describes channel number. | 17 | 95 | G2 | - | - | |
| | IC00_1 | | 65 | 43 | F9 | 55 | - | |
| | IC00_2 | | 54 | 32 | J8 | 44 | 36 | |
| | IC01_0 | | 16 | 94 | G1 | - | - | |
| | IC01_1 | | 66 | 44 | E11 | 56 | - | |
| | IC01_2 | | 55 | 33 | H10 | 45 | 37 | |
| | IC02_0 | | 15 | 93 | F3 | - | - | |
| | IC02_1 | | 67 | 45 | E10 | - | - | |
| | IC02_2 | | 56 | 34 | H9 | 46 | 38 | |
| | IC03_0 | | 14 | 92 | F2 | - | - | |
| | IC03_1 | | 68 | 46 | F8 | - | - | |
| | IC03_2 | | 57 | 35 | H7 | 47 | 39 | |
| | RTO00_0 (PPG00_0) | | Waveform generator output of multi-function timer 0. | 19 | 97 | G3 | 14 | 10 |
| | RTO00_1 (PPG00_1) | | This pin operates as PPG00 when it is used in PPG 0 output mode. | 71 | 49 | D10 | - | - |
| | RTO01_0 (PPG00_0) | | Waveform generator output of multi-function timer 0. This pin operates as PPG00 when it is used in PPG 0 output mode. | 20 | 98 | H1 | 15 | 11 |
| | RTO02_0 (PPG02_0) | Waveform generator output of multi-function timer 0. This pin operates as PPG02 when it is used in PPG 0 output mode. | 21 | 99 | H2 | 16 | 12 | |
| | RTO03_0 (PPG02_0) | Waveform generator output of multi-function timer 0. This pin operates as PPG02 when it is used in PPG 0 output mode. | 22 | 100 | G4 | 17 | 13 | |
| | RTO04_0 (PPG04_0) | Waveform generator output of multi-function timer 0. This pin operates as PPG04 when it is used in PPG 0 output mode. | 23 | 1 | H3 | 18 | 14 | |
| | RTO05_0 (PPG04_0) | Waveform generator output of multi-function timer 0. This pin operates as PPG04 when it is used in PPG 0 output mode. | 24 | 2 | J2 | 19 | 15 | |

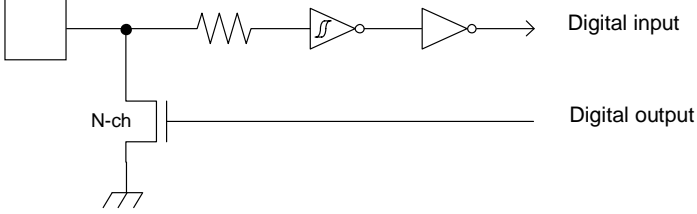
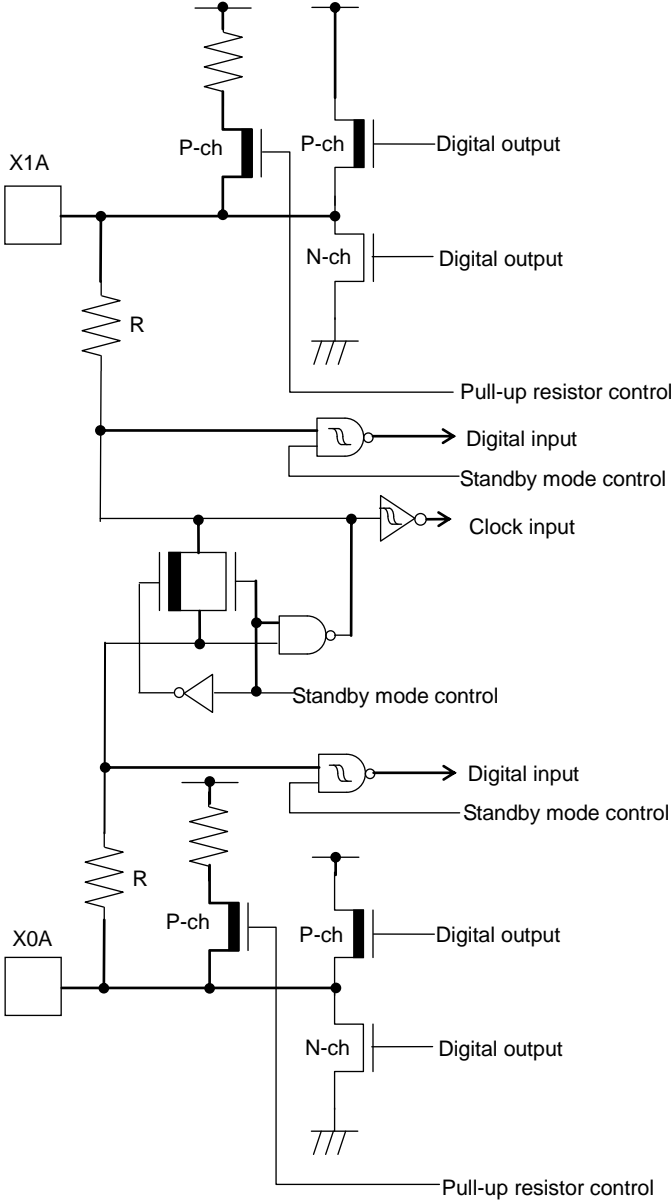
| Module | Pin name | Function | Pin No | | | | | |
|------------------------|--|--|--|---------|---------|---------|----------------|---|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 | |
| Multi Function Timer 1 | DTT1X_0 | Input signal of waveform generator to control outputs RTO10 to RTO15 of multi-function timer 1 | 8 | 86 | D5 | 8 | - | |
| | DTT1X_1 | | 39 | 17 | K6 | 29 | - | |
| | FRCK1_0 | 16-bit free-run timer ch.1 external clock input pin | 87 | 65 | D7 | 67 | - | |
| | FRCK1_1 | | 44 | 22 | J7 | 34 | - | |
| | IC10_0 | 16-bit input capture input pin of multi-function timer 1. ICxx describes channel number. | 88 | 66 | A6 | 68 | - | |
| | IC10_1 | | 40 | 18 | J6 | 30 | - | |
| | IC11_0 | | 89 | 67 | B6 | 69 | - | |
| | IC11_1 | | 41 | 19 | L7 | 31 | - | |
| | IC12_0 | | 90 | 68 | C6 | 70 | - | |
| | IC12_1 | | 42 | 20 | K7 | 32 | - | |
| | IC13_0 | | 91 | 69 | A5 | 71 | - | |
| | IC13_1 | | 43 | 21 | H6 | 33 | - | |
| | RTO10_0 (PPG10_0) | | Waveform generator output of multi-function timer 1. | 2 | 80 | C1 | 2 | - |
| | RTO10_1 (PPG10_1) | | This pin operates as PPG10 when it is used in PPG 1 output mode. | 27 | 5 | J4 | - | - |
| | RTO11_0 (PPG10_0) | Waveform generator output of multi-function timer 1. | 3 | 81 | C2 | 3 | - | |
| | RTO11_1 (PPG10_1) | This pin operates as PPG10 when it is used in PPG 1 output mode. | 28 | 6 | L5 | - | - | |
| | RTO12_0 (PPG12_0) | Waveform generator output of multi-function timer 1. | 4 | 82 | B3 | 4 | - | |
| | RTO12_1 (PPG12_1) | This pin operates as PPG12 when it is used in PPG 1 output mode. | 29 | 7 | K5 | - | - | |
| | RTO13_0 (PPG12_0) | Waveform generator output of multi-function timer 1. | 5 | 83 | D1 | 5 | - | |
| | RTO13_1 (PPG12_1) | This pin operates as PPG12 when it is used in PPG 1 output mode. | 30 | 8 | J5 | - | - | |
| | RTO14_0 (PPG14_0) | Waveform generator output of multi-function timer 1. | 6 | 84 | D2 | 6 | - | |
| | RTO14_1 (PPG14_1) | This pin operates as PPG14 when it is used in PPG 1 output mode. | 31 | 9 | H5 | 21 | - | |
| | RTO15_0 (PPG14_0) | Waveform generator output of multi-function timer 1. | 7 | 85 | D3 | 7 | - | |
| RTO15_1 (PPG14_1) | This pin operates as PPG14 when it is used in PPG 1 output mode. | 32 | 10 | L6 | 22 | - | | |

| Module | Pin name | Function | Pin No | | | | |
|---|----------|-------------------------|----------|---------|---------|---------|-------------------|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 |
| Quadrature Position/ Revolution Counter 0 | AIN0_0 | QPRC ch.0 AIN input pin | 9 | 87 | E1 | 9 | 5 |
| | AIN0_1 | | 40 | 18 | J6 | 30 | 22 |
| | AIN0_2 | | 2 | 80 | C1 | 2 | 2 |
| | BIN0_0 | QPRC ch.0 BIN input pin | 10 | 88 | E2 | 10 | 6 |
| | BIN0_1 | | 41 | 19 | L7 | 31 | 23 |
| | BIN0_2 | | 3 | 81 | C2 | 3 | 3 |
| | ZIN0_0 | QPRC ch.0 ZIN input pin | 11 | 89 | E3 | 11 | 7 |
| | ZIN0_1 | | 42 | 20 | K7 | 32 | 24 |
| | ZIN0_2 | | 4 | 82 | B3 | 4 | 4 |
| Quadrature Position/ Revolution Counter 1 | AIN1_1 | QPRC ch.1 AIN input pin | 74 | 52 | C10 | 60 | - |
| | AIN1_2 | | 43 | 21 | H6 | 33 | 25 |
| | BIN1_1 | QPRC ch.1 BIN input pin | 73 | 51 | C11 | 59 | - |
| | BIN1_2 | | 44 | 22 | J7 | 34 | 26 |
| | ZIN1_1 | QPRC ch.1 ZIN input pin | 72 | 50 | E8 | 58 | - |
| | ZIN1_2 | | 45 | 23 | K8 | 35 | 27 |

| Module | Pin name | Function | Pin No | | | | |
|-----------|----------|--|----------|---------|---------|---------|-------------------|
| | | | LQFP-100 | QFP-100 | BGA-112 | LQFP-80 | LQFP-64 QFN-64 |
| RESET | INITX | External Reset Input. A reset is valid when INITX= "L" | 38 | 16 | K4 | 28 | 21 |
| Mode | MD0 | Mode 0 pin. During normal operation, MD0= "L" must be input. During serial programming to flash memory, MD0= "H" must be input. | 47 | 25 | L8 | 37 | 29 |
| | MD1 | Mode 1 pin. During serial programming to flash memory, MD1= "L" must be input. | 46 | 24 | K9 | 36 | 28 |
| POWER | VCC | Power supply pin | 1 | 79 | B1 | 1 | 1 |
| | VCC | Power supply pin | 26 | 4 | J1 | - | - |
| | VCC | Power supply pin | 35 | 13 | K1 | 25 | 18 |
| | VCC | Power supply pin | 51 | 29 | K11 | 41 | 33 |
| | VCC | Power supply pin | 76 | 54 | A10 | - | - |
| | VCC | Power supply pin | 97 | 75 | A4 | 77 | 61 |
| GND | VSS | GND pin | - | - | B2 | - | - |
| | VSS | GND pin | 25 | 3 | L1 | 20 | 16 |
| | VSS | GND pin | - | - | K2 | - | - |
| | VSS | GND pin | - | - | J3 | - | - |
| | VSS | GND pin | - | - | H4 | - | - |
| | VSS | GND pin | 34 | 12 | L4 | 24 | - |
| | VSS | GND pin | 50 | 28 | L11 | 40 | 32 |
| | VSS | GND pin | - | - | K10 | - | - |
| | VSS | GND pin | - | - | J9 | - | - |
| | VSS | GND pin | - | - | H8 | - | - |
| | VSS | GND pin | - | - | B10 | - | - |
| | VSS | GND pin | - | - | C9 | - | - |
| | VSS | GND pin | 75 | 53 | A11 | - | - |
| | VSS | GND pin | - | - | D8 | - | - |
| | VSS | GND pin | - | - | D4 | - | - |
| | VSS | GND pin | - | - | C3 | - | - |
| | VSS | GND pin | 100 | 78 | A1 | 80 | 64 |
| CLOCK | X0 | Main clock (oscillation) input pin | 48 | 26 | L9 | 38 | 30 |
| | X0A | Sub clock (oscillation) input pin | 36 | 14 | L3 | 26 | 19 |
| | X1 | Main clock (oscillation) I/O pin | 49 | 27 | L10 | 39 | 31 |
| | X1A | Sub clock (oscillation) I/O pin | 37 | 15 | K3 | 27 | 20 |
| | CROUT_0 | Built-in high-speed CR-osc clock output port | 74 | 52 | C10 | 60 | - |
| | CROUT_1 | | 92 | 70 | B5 | 72 | 57 |
| ADC POWER | AVCC | A/D converter analog power supply pin | 60 | 38 | H11 | 50 | 41 |
| | AVRH | A/D converter analog reference voltage input pin | 61 | 39 | F11 | 51 | 42 |
| ADC GND | AVSS | A/D converter GND pin | 62 | 40 | G11 | 52 | 43 |
| C pin | C | Power supply stabilization capacity pin | 33 | 11 | L2 | 23 | 17 |

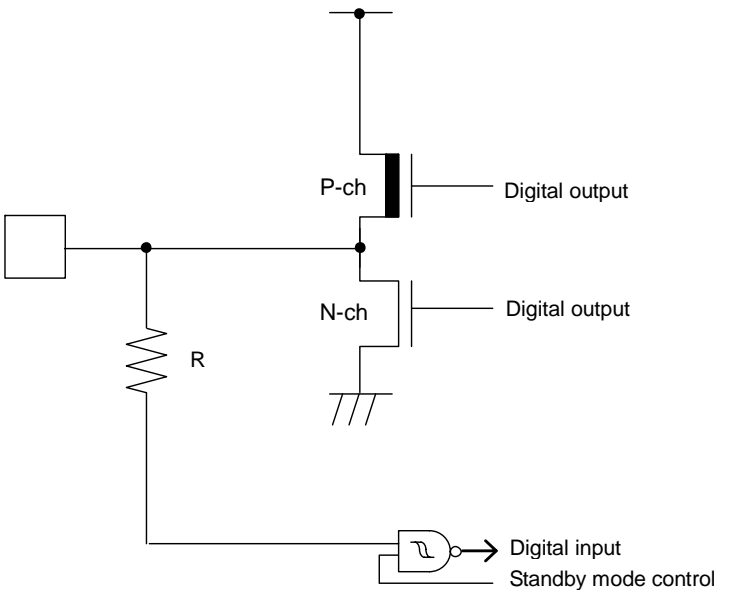
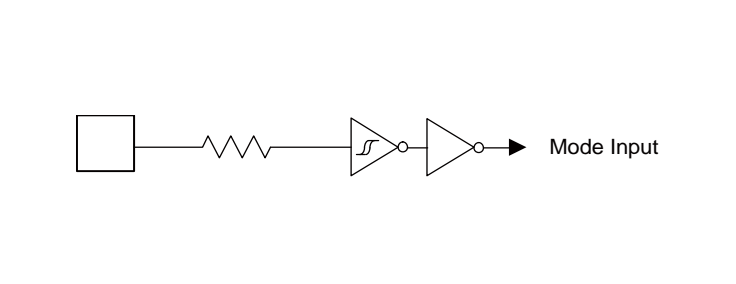
■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|------|---------|--|
| A | | <p>It is possible to select the main oscillation / GPIO function</p> <p>When the main oscillation is selected.</p> <ul style="list-style-type: none"> • Oscillation feedback resistor : Approximately 1MΩ • With Standby mode control <p>When the GPIO is selected.</p> <ul style="list-style-type: none"> • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • $I_{OH} = -4mA, I_{OL} = 4mA$ |
| B | | <ul style="list-style-type: none"> • CMOS level hysteresis input • Pull-up resistor : Approximately 50kΩ |

| Type | Circuit | Remarks |
|------|--|--|
| C |  | <ul style="list-style-type: none"> • Open drain output • CMOS level hysteresis input |
| D |  | <ul style="list-style-type: none"> • It is possible to select the sub oscillation / GPIO function <p>When the sub oscillation is selected.</p> <ul style="list-style-type: none"> • Oscillation feedback resistor : Approximately 5MΩ • With Standby mode control <p>When the GPIO is selected.</p> <ul style="list-style-type: none"> • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • I_{OH} = -4mA, I_{OL} = 4mA |

| Type | Circuit | Remarks |
|------|---|--|
| E | <p>The diagram for Type E shows a CMOS output stage. A pull-up resistor R is connected to the output node. The output node is driven by a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch MOSFET's gate is connected to a digital input through an inverter. The N-ch MOSFET's gate is connected to a digital input through an AND gate. The output node is also connected to a pull-up resistor control input. The output node is labeled 'Digital output'. The N-ch MOSFET's source is connected to ground, labeled 'Digital output'. The pull-up resistor control input is labeled 'Pull-up resistor control'. The digital input is labeled 'Digital input' and 'Standby mode control'.</p> | <ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • $I_{OH} = -4\text{mA}$, $I_{OL} = 4\text{mA}$ |
| F | <p>The diagram for Type F shows a CMOS output stage similar to Type E. It includes a pull-up resistor R, P-ch and N-ch MOSFETs, and control inputs for digital output, pull-up resistor control, digital input, standby mode control, analog input, and input control. The output node is labeled 'Digital output'. The N-ch MOSFET's source is connected to ground, labeled 'Digital output'. The pull-up resistor control input is labeled 'Pull-up resistor control'. The digital input is labeled 'Digital input'. The standby mode control input is labeled 'Standby mode control'. The analog input is labeled 'Analog input'. The input control input is labeled 'Input control'.</p> | <ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • $I_{OH} = -4\text{mA}$, $I_{OL} = 4\text{mA}$ |

| Type | Circuit | Remarks |
|------|---|--|
| G | <p> P-ch P-ch N-ch R Digital output Digital output Pull-up resistor control Digital input Standby mode control </p> | <ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50kΩ • $I_{OH} = -12\text{mA}$, $I_{OL} = 12\text{mA}$ |
| H | <p> P-ch N-ch R Digital output Digital output Digital input Standby mode control </p> | <ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • With standby mode control • $I_{OH} = -20.5\text{mA}$, $I_{OL} = 18.5\text{mA}$ |

| Type | Circuit | Remarks |
|------|---|---|
| I |  <p>The diagram shows a CMOS output stage. A pull-up resistor labeled 'R' is connected to a supply rail. The other end of the resistor is connected to the gates of both a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch MOSFET's source is connected to the supply rail, and its drain is labeled 'Digital output'. The N-ch MOSFET's source is connected to ground, and its drain is also labeled 'Digital output'. A digital input pin, which also serves as a standby mode control, is connected to the gates of both MOSFETs through a small capacitor.</p> | <ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • 5V tolerant • With standby mode control • $I_{OH} = -4\text{mA}$, $I_{OL} = 4\text{mA}$ |
| J |  <p>The diagram shows a CMOS level hysteresis input circuit. It consists of a resistor connected to a supply rail, followed by two inverters in series. The output of the second inverter is labeled 'Mode Input'.</p> | <p>CMOS level hysteresis input</p> |

■ HANDLING PRECAUTIONS

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Spansion semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

• Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

• Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

• Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

• Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNP junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

(1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

(2) Be sure that abnormal current flows do not occur during the power-on sequence.

- **Observance of Safety Regulations and Standards**

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- **Fail-Safe Design**

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- **Precautions Related to Usage of Devices**

Spansion semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Spansion's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- **Lead Insertion Type**

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Spansion recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- **Surface Mount Type**

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Spansion recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Spansion ranking of recommended conditions.

- **Lead-Free Packaging**

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- **Storage of Semiconductor Devices**

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
- (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.
- (3) When necessary, Spansion packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- **Baking**

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Spansion recommended conditions for baking.

Condition: 125°C/24 h

- **Static Electricity**

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- (1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
- (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (4) Ground all fixtures and instruments, or protect with anti-static measures.
- (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Spansion products in other special environmental conditions should consult with sales representatives.

Please check the latest handling precautions at the following URL.

<http://www.spansion.com/fjdocuments/fj/datasheet/e-ds/DS00-00004.pdf>

■ HANDLING DEVICES

- Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 μF be connected as a bypass capacitor between each Power supply pin and GND pin near this device.

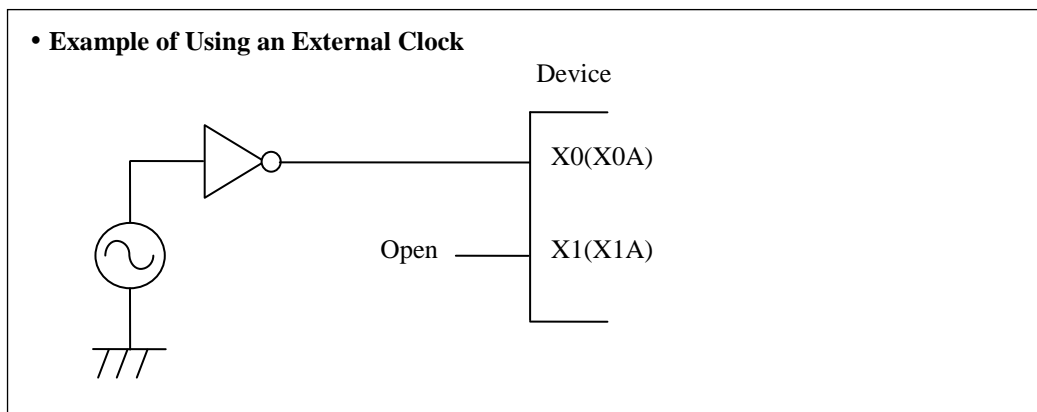
- Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

- Using an external clock

When using an external clock, the clock signal should be input to the X0,X0A pin only and the X1,X1A pin should be kept open.

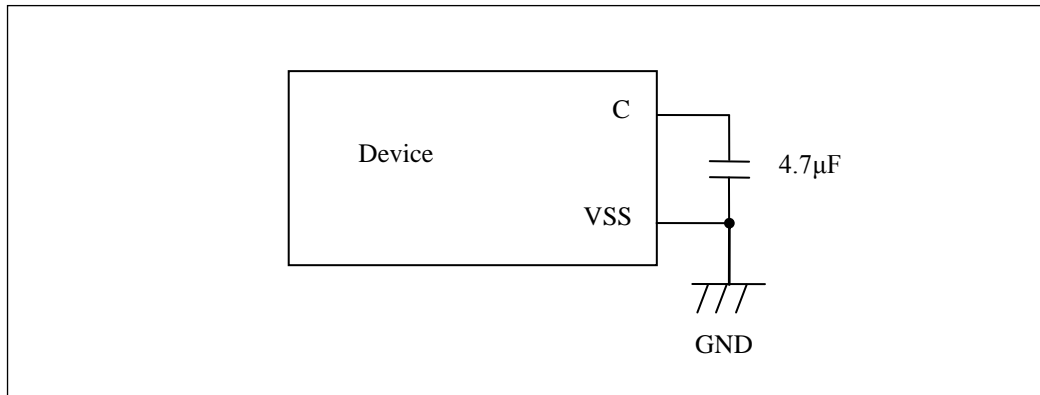


- Handling when using Multi function serial pin as I²C pin

If it is using the multi function serial pin as I²C pins, P-ch transistor of digital output is always disabled. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

- C Pin

As this series includes an internal regulator, always connect a bypass capacitor of approximately 4.7 μF to the C pin for use by the regulator.



- Mode pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

- Notes on power-on

Turn power on/off in the following order or at the same time.

If not using the A/D converter, connect AVCC = VCC and AVSS = VSS.

Turning on : VCC \rightarrow AVCC \rightarrow AVRH

Turning off : AVRH \rightarrow AVCC \rightarrow VCC

- Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.

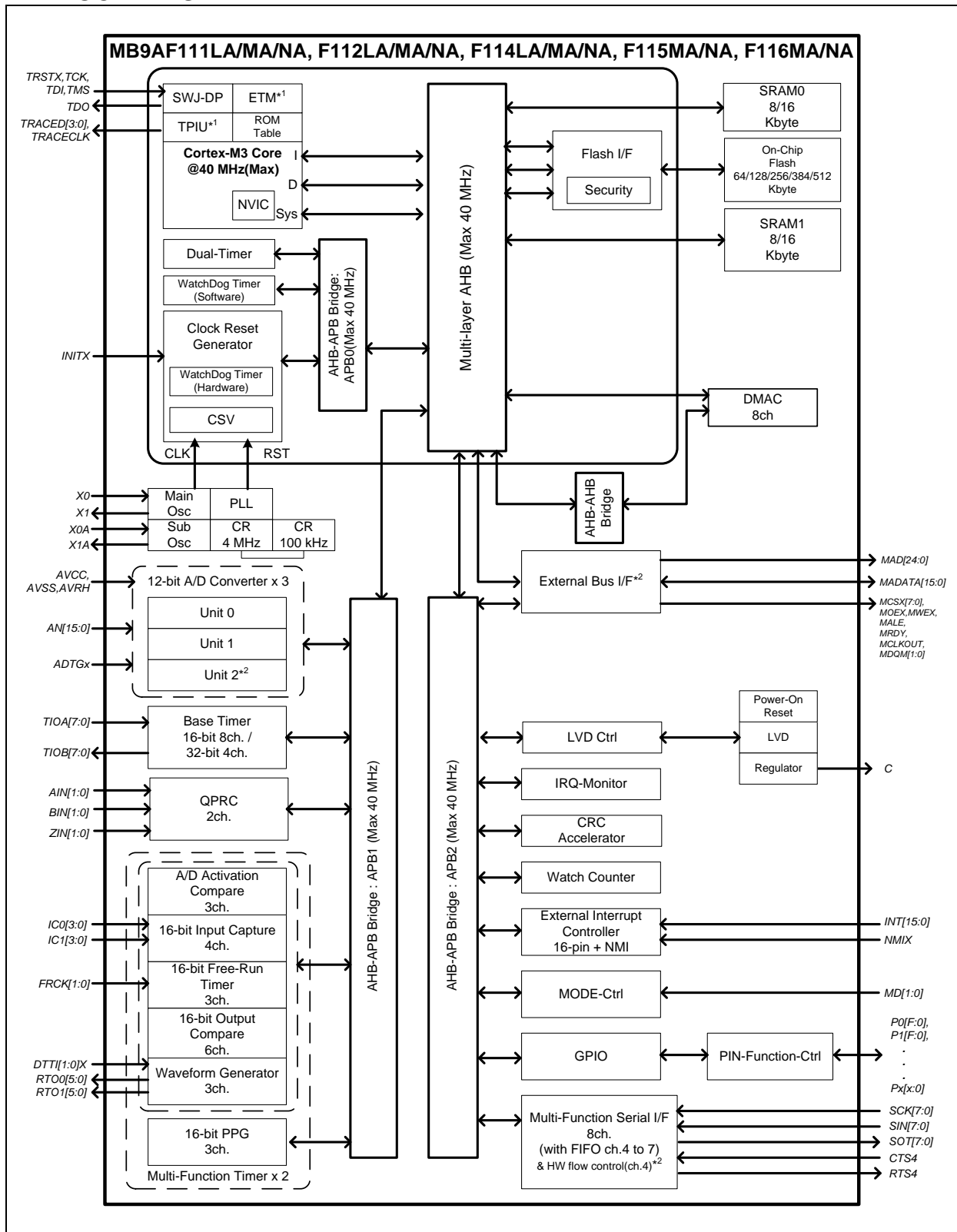
Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

- Differences in features among the products with different memory sizes and between Flash products and MASK products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

■ BLOCK DIAGRAM



*1: For the MB9AF111LA/MA, F112LA/MA, MB9AF114LA/MA, MB9AF115MA and MB9AF116MA, ETM is not available.

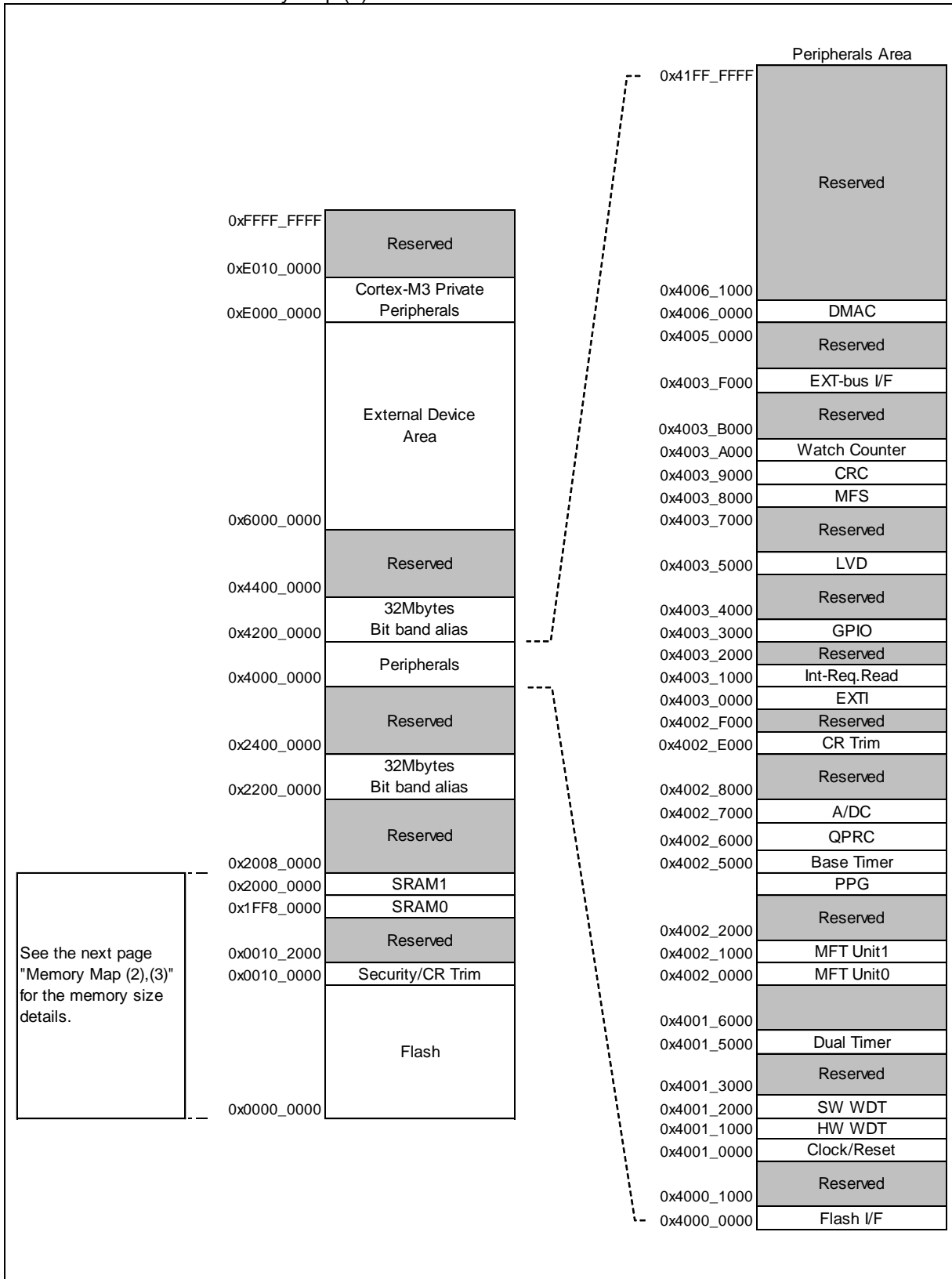
*2: For the MB9AF111LA, F112LA and MB9AF114LA, the External Bus Interface and 12-bit A/D Converter (unit 2) are not available. And the Multi-function Serial Interface does not support hardware flow control in these products.

■ MEMORY SIZE

See "●Memory size" in "■PRODUCT LINEUP" to confirm the memory size.

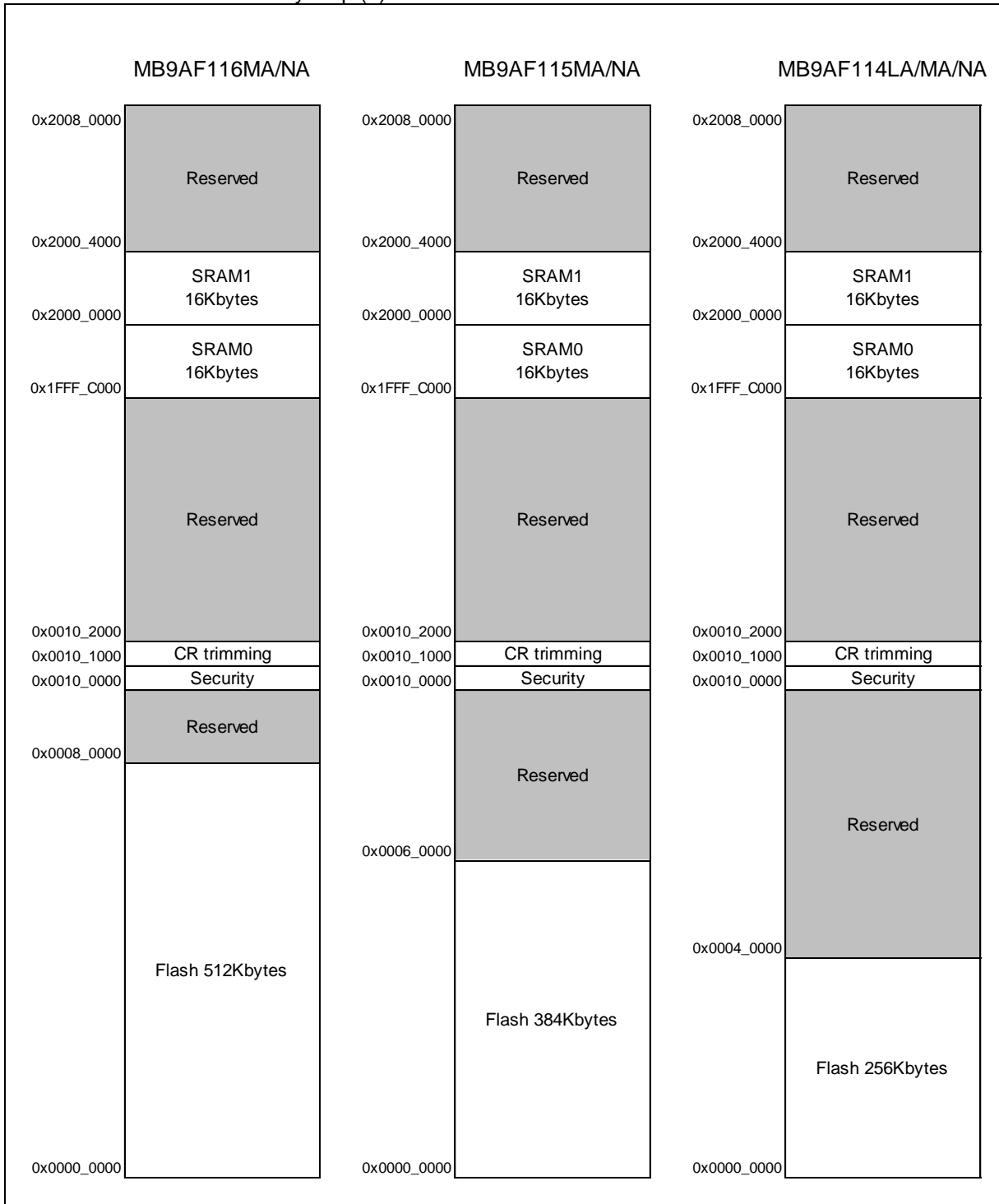
■ MEMORY MAP

● MB9A110A Series Memory Map (1)

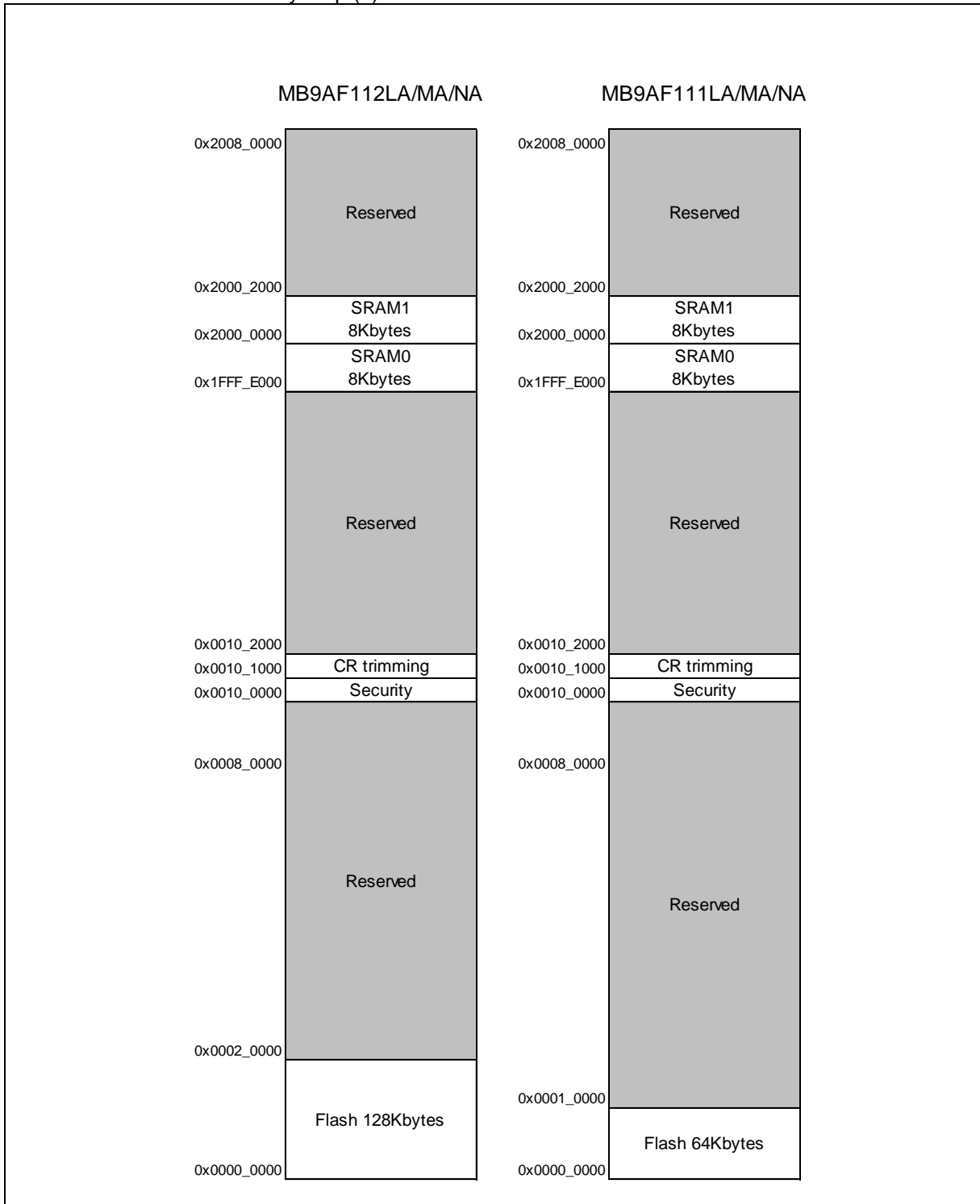


See the next page "Memory Map (2),(3)" for the memory size details.

● MB9A110A Series Memory Map (2)



● MB9A110A Series Memory Map (3)



● Peripheral Address Map

| Start address | End address | Bus | Peripherals |
|--------------------------|--------------------------|---|---------------------------------|
| 0x4000_0000 _H | 0x4000_0FFF _H | AHB | Flash I/F register |
| 0x4000_1000 _H | 0x4000_FFFF _H | | Reserved |
| 0x4001_0000 _H | 0x4001_0FFF _H | APB0 | Clock/Reset Control |
| 0x4001_1000 _H | 0x4001_1FFF _H | | Hardware Watchdog timer |
| 0x4001_2000 _H | 0x4001_2FFF _H | | Software Watchdog timer |
| 0x4001_3000 _H | 0x4001_4FFF _H | | Reserved |
| 0x4001_5000 _H | 0x4001_5FFF _H | | Dual-Timer |
| 0x4001_6000 _H | 0x4001_FFFF _H | | Reserved |
| 0x4002_0000 _H | 0x4002_0FFF _H | | APB1 |
| 0x4002_1000 _H | 0x4002_1FFF _H | Multi-function timer unit1 | |
| 0x4002_2000 _H | 0x4002_3FFF _H | Reserved | |
| 0x4002_4000 _H | 0x4002_4FFF _H | PPG | |
| 0x4002_5000 _H | 0x4002_5FFF _H | Base Timer | |
| 0x4002_6000 _H | 0x4002_6FFF _H | Quadrature Position/Revolution Counter (QPRC) | |
| 0x4002_7000 _H | 0x4002_7FFF _H | A/D Converter | |
| 0x4002_8000 _H | 0x4002_DFFF _H | Reserved | |
| 0x4002_E000 _H | 0x4002_EFFF _H | Built-in CR trimming | |
| 0x4002_F000 _H | 0x4002_FFFF _H | Reserved | |
| 0x4003_0000 _H | 0x4003_0FFF _H | APB2 | |
| 0x4003_1000 _H | 0x4003_1FFF _H | | Interrupt Source Check Register |
| 0x4003_2000 _H | 0x4003_2FFF _H | | Reserved |
| 0x4003_3000 _H | 0x4003_3FFF _H | | GPIO |
| 0x4003_4000 _H | 0x4003_4FFF _H | | Reserved |
| 0x4003_5000 _H | 0x4003_5FFF _H | | Low-Voltage Detector |
| 0x4003_6000 _H | 0x4003_6FFF _H | | Reserved |
| 0x4003_7000 _H | 0x4003_7FFF _H | | Reserved |
| 0x4003_8000 _H | 0x4003_8FFF _H | | Multi-function serial Interface |
| 0x4003_9000 _H | 0x4003_9FFF _H | | CRC |
| 0x4003_A000 _H | 0x4003_AFFF _H | | Watch Counter |
| 0x4003_B000 _H | 0x4003_EFFF _H | | Reserved |
| 0x4003_F000 _H | 0x4003_FFFF _H | | External Bus interface |
| 0x4004_0000 _H | 0x4004_FFFF _H | | AHB |
| 0x4005_0000 _H | 0x4005_FFFF _H | Reserved | |
| 0x4006_0000 _H | 0x4006_0FFF _H | DMAC register | |
| 0x4006_1000 _H | 0x4006_1FFF _H | Reserved | |
| 0x4006_2000 _H | 0x4006_2FFF _H | Reserved | |
| 0x4006_3000 _H | 0x4006_3FFF _H | Reserved | |
| 0x4006_4000 _H | 0x41FF_FFFF _H | Reserved | |

■ PIN STATUS IN EACH CPU STATE

The terms used for pin status have the following meanings.

- INITX=0
This is the period when the INITX pin is the "L" level.
- INITX=1
This is the period when the INITX pin is the "H" level.
- SPL=0
This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to "0".
- SPL=1
This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to "1".
- Input enabled
Indicates that the input function can be used.
- Internal input fixed at "0"
This is the status that the input function cannot be used. Internal input is fixed at "L".
- Hi-Z
Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.
- Setting disabled
Indicates that the setting is disabled.
- Maintain previous state
Maintains the state that was immediately prior to entering the current mode.
If a built-in peripheral function is operating, the output follows the peripheral function.
If the pin is being used as a port, that output is maintained.
- Analog input is enabled
Indicates that the analog input is enabled.
- Trace output
Indicates that the trace function can be used.

● List of Pin Status

| Pin status type | Function group | Power-on reset or low-voltage detection state | INITX input state | Device internal reset state | Run mode or SLEEP mode state | Timer mode or STOP mode state | |
|-----------------|--|--|--------------------------------------|--------------------------------------|------------------------------|--|--|
| | | Power supply unstable | Power supply stable | | Power supply stable | Power supply stable | |
| | | - | INITX=0 | INITX=1 | INITX=1 | INITX=1 | |
| | | - | - | - | - | SPL=0 | SPL=1 |
| A | GPIO selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z/ Internal input fixed at "0" |
| | Main crystal oscillator input pin | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled |
| B | GPIO selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z/ Internal input fixed at "0" |
| | Main crystal oscillator output pin | Hi-Z/ Internal input fixed at "0"/ or Input enable | Hi-Z/ Internal input fixed at "0" | Hi-Z/ Internal input fixed at "0" | Maintain previous state | Maintain previous state/ Hi-Z at oscillation stop*1/ Internal input fixed at "0" | Maintain previous state/ Hi-Z at oscillation stop*1/ Internal input fixed at "0" |
| C | INITX input pin | Pull-up/ Input enabled | Pull-up/ Input enabled | Pull-up/ Input enabled | Pull-up/ Input enabled | Pull-up/ Input enabled | Pull-up/ Input enabled |
| D | Mode input pin | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled |
| E | JTAG selected | Hi-Z | Pull-up/ Input enabled | Pull-up/ Input enabled | Maintain previous state | Maintain previous state | Maintain previous state |
| | GPIO selected | Setting disabled | Setting disabled | Setting disabled | | | Hi-Z/ Internal input fixed at "0" |
| F | Trace selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Trace output |
| | External interrupt enabled selected | | | | | | Maintain previous state |
| | GPIO selected, or resource other than above selected | Hi-Z | Hi-Z/ Input enabled | Hi-Z/ Input enabled | | | Hi-Z/ Internal input fixed at "0" |

| Pin status type | Function group | Power-on reset or low-voltage detection state | INITX input state | Device internal reset state | Run mode or SLEEP mode state | Timer mode or STOP mode state | |
|-----------------|--|---|------------------------|-----------------------------|------------------------------|-------------------------------|--------------------------------------|
| | | Power supply unstable | Power supply stable | | Power supply stable | Power supply stable | |
| | | - | INITX=0 | INITX=1 | INITX=1 | INITX=1 | |
| | | - | - | - | - | SPL=0 | SPL=1 |
| G | Trace selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Trace output |
| | GPIO selected, or resource other than above selected | Hi-Z | Hi-Z/ Input enabled | Hi-Z/ Input enabled | | | Hi-Z/ Internal input fixed at "0" |
| H | External interrupt enabled selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Maintain previous state |
| | GPIO selected, or resource other than above selected | Hi-Z | Hi-Z/ Input enabled | Hi-Z/ Input enabled | | | Hi-Z/ Internal input fixed at "0" |
| I | GPIO selected, resource selected | Hi-Z | Hi-Z/ Input enabled | Hi-Z/ Input enabled | Maintain previous state | Maintain previous state | Hi-Z/ Internal input fixed at "0" |
| J | NMIX selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Maintain previous state |
| | GPIO selected, or resource other than above selected | Hi-Z | Hi-Z/ Input enabled | Hi-Z/ Input enabled | | | Hi-Z/ Internal input fixed at "0" |

| Pin status type | Function group | Power-on reset or low-voltage detection state | INITX input state | Device internal reset state | Run mode or SLEEP mode state | Timer mode or STOP mode state | |
|-----------------|--|---|---|---|---|---|---|
| | | Power supply unstable | Power supply stable | | Power supply stable | Power supply stable | |
| | | - | INITX=0 | INITX=1 | INITX=1 | INITX=1 | |
| | | - | - | - | - | SPL=0 | SPL=1 |
| K | Analog input selected | Hi-Z | Hi-Z/ Internal input fixed at "0"/ Analog input enabled | Hi-Z/ Internal input fixed at "0"/ Analog input enabled | Hi-Z/ Internal input fixed at "0"/ Analog input enabled | Hi-Z/ Internal input fixed at "0"/ Analog input enabled | Hi-Z/ Internal input fixed at "0"/ Analog input enabled |
| | GPIO selected, or resource other than above selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z/ Internal input fixed at "0" |
| L | External interrupt enabled selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Maintain previous state |
| | Analog input selected | Hi-Z | Hi-Z/ Internal input fixed at "0"/ Analog input enabled | Hi-Z/ Internal input fixed at "0"/ Analog input enabled | Hi-Z/ Internal input fixed at "0"/ Analog input enabled | Hi-Z/ Internal input fixed at "0"/ Analog input enabled | Hi-Z/ Internal input fixed at "0"/ Analog input enabled |
| | GPIO selected, or resource other than above selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z/ Internal input fixed at "0" |
| M | GPIO selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z/ Internal input fixed at "0" |
| | Sub crystal oscillator input pin | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled |

| Pin status type | Function group | Power-on reset or low-voltage detection state | INITX input state | Device internal reset state | Run mode or SLEEP mode state | Timer mode or STOP mode state | |
|-----------------|-----------------------------------|---|-----------------------------------|-----------------------------------|------------------------------|--|--|
| | | Power supply unstable | Power supply stable | | Power supply stable | Power supply stable | |
| | | - | INITX=0 | INITX=1 | INITX=1 | INITX=1 | |
| | | - | - | - | - | SPL=0 | SPL=1 |
| N | GPIO selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z/ Internal input fixed at "0" |
| | Sub crystal oscillator output pin | Hi-Z/ Internal input fixed at "0"/ or Input enabled | Hi-Z/ Internal input fixed at "0" | Hi-Z/ Internal input fixed at "0" | Maintain previous state | Maintain previous state/ Hi-Z at oscillation stop*2/ Internal input fixed at "0" | Maintain previous state/ Hi-Z at oscillation stop*2/ Internal input fixed at "0" |
| O | GPIO pin | Hi-Z | Hi-Z/ Input enabled | Hi-Z/ Input enabled | Maintain previous state | Maintain previous state | Hi-Z/ Internal input fixed at "0" |
| P | Mode input pin | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled | Input enabled |
| | GPIO selected | Setting disabled | Setting disabled | Setting disabled | Maintain previous state | Maintain previous state | Hi-Z/ Input enabled |

*1 : Oscillation is stopped at sub timer mode, low-speed CR timer mode, and stop mode.

*2 : Oscillation is stopped at stop mode.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|--------------------|-----------------------|------------------------------------|------|-------------|
| | | Min | Max | | |
| Supply voltage* ¹ , * ² | V _{CC} | V _{SS} - 0.5 | V _{SS} + 6.5 | V | |
| Analog supply voltage* ¹ , * ³ | AV _{CC} | V _{SS} - 0.5 | V _{SS} + 6.5 | V | |
| Analog reference voltage* ¹ , * ³ | AV _{RH} | V _{SS} - 0.5 | V _{SS} + 6.5 | V | |
| Input voltage* ¹ | V _I | V _{SS} - 0.5 | V _{CC} + 0.5 (≤ 6.5V) | V | |
| | | V _{SS} - 0.5 | V _{SS} + 6.5 | V | 5V tolerant |
| Analog pin input voltage* ¹ | V _{IA} | V _{SS} - 0.5 | AV _{CC} + 0.5 (≤ 6.5V) | V | |
| Output voltage* ¹ | V _O | V _{SS} - 0.5 | V _{CC} + 0.5 (≤ 6.5V) | V | |
| "L" level maximum output current* ⁴ | I _{OL} | - | 10 | mA | 4mA type |
| | | | 20 | mA | 12mA type |
| "L" level average output current* ⁵ | I _{OLAV} | - | 4 | mA | 4mA type |
| | | | 12 | mA | 12mA type |
| "L" level total maximum output current | ∑I _{OL} | - | 100 | mA | |
| "L" level total average output current* ⁶ | ∑I _{OLAV} | - | 50 | mA | |
| "H" level maximum output current* ⁴ | I _{OH} | - | - 10 | mA | 4mA type |
| | | | - 20 | mA | 12mA type |
| "H" level average output current* ⁵ | I _{OHAV} | - | - 4 | mA | 4mA type |
| | | | - 12 | mA | 12mA type |
| "H" level total maximum output current | ∑I _{OH} | - | - 100 | mA | |
| "H" level total average output current* ⁶ | ∑I _{OHAV} | - | - 50 | mA | |
| Power consumption | P _D | - | 300 | mW | |
| Storage temperature | T _{STG} | - 55 | + 150 | °C | |

*1 : These parameters are based on the condition that V_{SS} = AV_{SS} = 0.0V.

*2 : V_{CC} must not drop below V_{SS} - 0.5V.

*3 : Be careful not to exceed V_{CC} + 0.5 V, for example, when the power is turned on.

*4 : The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*5 : The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.

*6 : The total average output current is defined as the average current value flowing through all of corresponding pins for a 100ms.

<WARNING>

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0V)

| Parameter | Symbol | Conditions | Value | | Unit | Remarks | |
|--------------------------|--|----------------|---|------------------|-------|------------------------------------|------------------------|
| | | | Min | Max | | | |
| Supply voltage | V _{CC} | - | 2.7 | 5.5 | V | | |
| Analog supply voltage | AV _{CC} | - | 2.7 | 5.5 | V | AV _{CC} = V _{CC} | |
| Analog reference voltage | AV _{RH} | - | AV _{SS} | AV _{CC} | V | | |
| Operating temperature | FPT-100P-M20, FPT-100P-M23, FPT-80P-M21, FPT-80P-M37, FPT-64P-M24, FPT-64P-M38, FPT-64P-M23, FPT-64P-M39, LCC-64P-M24, BGA-112P-M04 | T _a | - | - 40 | + 105 | °C | |
| | FPT-100P-M06 | T _a | When mounted on four-layer PCB | - 40 | + 105 | °C | |
| | | | When mounted on double-sided single-layer PCB | - 40 | + 105 | °C | I _{CC} ≤ 35mA |
| | | | | - 40 | + 85 | °C | I _{CC} > 35mA |

<WARNING>

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(1) Current rating

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V, Ta = - 40°C to + 105°C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|----------------------|--------|----------|---|-------|------|-----|------|---|
| | | | | Min | Typ | Max | | |
| Power supply current | Icc | VCC | Normal operation (PLL) Vcc=5.5V | - | 32 | 41 | mA | CPU : 40MHz, Peripheral : 40MHz, Flash 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000 *1 |
| | | | | - | 21 | 28 | mA | CPU : 40MHz, Peripheral : 40MHz, Flash 3Wait FRWTR.RWT = 00 FSYNDN.SD = 011 *1 |
| | | | Normal operation (built-in high-speed CR) Vcc=5.5V | - | 3.9 | 7.7 | mA | CPU/ Peripheral : 4MHz *1, *2 Flash 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000 |
| | | | Normal operation (sub oscillation) Vcc=5.5V | - | 0.15 | 3.2 | mA | CPU/ Peripheral : 32kHz Flash 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000 *1 |
| | | | Normal operation (built-in low-speed CR) Vcc=5.5V | - | 0.2 | 3.3 | mA | CPU/ Peripheral : 100kHz Flash 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000 *1 |
| | | | SLEEP operation (PLL) Vcc=5.5V | - | 10 | 15 | mA | Peripheral : 40MHz *1 |
| | Iccs | | SLEEP operation (built-in high-speed CR) Vcc=5.5V | - | 1.2 | 4.4 | mA | Peripheral : 4MHz *1, *2 |
| | | | SLEEP operation (sub oscillation) Vcc=5.5V | - | 0.1 | 3.1 | mA | Peripheral : 32kHz *1 |
| | | | SLEEP operation (built in low-speed CR) Vcc=5.5V | - | 0.1 | 3.1 | mA | Peripheral : 100kHz *1 |

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|--|--------------------|----------|--|-------|-----|-----|------|--|
| | | | | Min | Typ | Max | | |
| Power supply current | I _{CCH} | VCC | STOP mode V _{CC} =5.5V | - | 35 | 200 | μA | Ta = + 25°C, When LVD is off *1 |
| | | | | - | - | 3 | mA | Ta = + 105°C, When LVD is off *1 |
| | I _{CCT} | | TIMER mode (sub oscillation) V _{CC} =5.5V | - | 60 | 230 | μA | Ta = + 25°C, When LVD is off *1 |
| | | | | - | - | 3.1 | mA | Ta = + 105°C, When LVD is off *1 |
| Low-voltage detection circuit (LVD) power supply current | I _{CCLVD} | | At operation V _{CC} =5.5V | - | 4 | 7 | μA | for occurrence of interrupt |

*1: When all ports are fixed.

*2: When setting it to 4MHz by trimming.

(2) Pin Characteristics

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -40^{\circ}C$ to $+105^{\circ}C$)

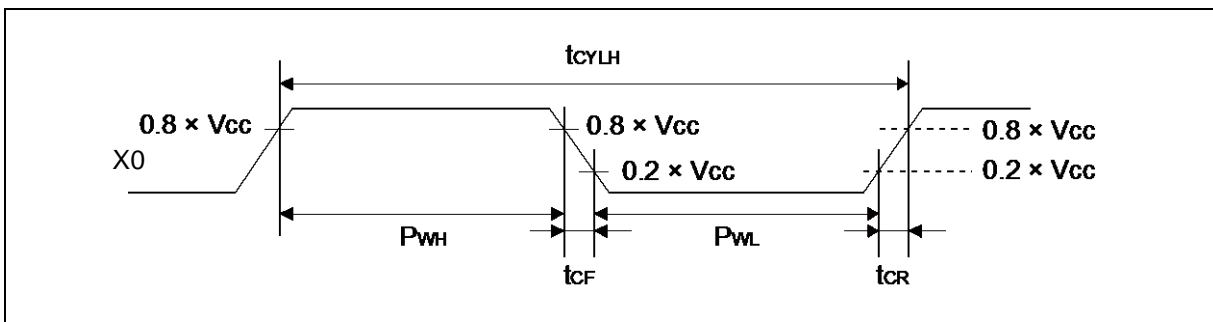
| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|--|-----------|---|--|---------------------|-----|---------------------|------------|---------|
| | | | | Min | Typ | Max | | |
| "H" level input voltage (hysteresis input) | V_{IHS} | CMOS hysteresis input pin, MD0, MD1 | - | $V_{CC} \times 0.8$ | - | $V_{CC} + 0.3$ | V | |
| | | 5V tolerant I/O | - | $V_{CC} \times 0.8$ | - | $V_{SS} + 5.5$ | V | |
| "L" level input voltage (hysteresis input) | V_{ILS} | CMOS hysteresis input pin, MD0, MD1 | - | $V_{SS} - 0.3$ | - | $V_{CC} \times 0.2$ | V | |
| "H" level output voltage | V_{OH} | 4mA type | $V_{CC} \geq 4.5V$ $I_{OH} = -4mA$ | $V_{CC} - 0.5$ | - | V_{CC} | V | |
| | | | $V_{CC} < 4.5V$ $I_{OH} = -2mA$ | | | | | |
| | | 12mA type | $V_{CC} \geq 4.5V$ $I_{OH} = -12mA$ | $V_{CC} - 0.5$ | - | V_{CC} | V | |
| | | | $V_{CC} < 4.5V$ $I_{OH} = -8mA$ | | | | | |
| | | P80, P81 | $V_{CC} \geq 4.5V$ $I_{OH} = -20.5mA$ | $V_{CC} - 0.4$ | - | V_{CC} | V | |
| | | | $V_{CC} < 4.5V$ $I_{OH} = -13.0mA$ | | | | | |
| "L" level output voltage | V_{OL} | 4mA type | $V_{CC} \geq 4.5V$ $I_{OL} = 4mA$ | V_{SS} | - | 0.4 | V | |
| | | | $V_{CC} < 4.5V$ $I_{OL} = 2mA$ | | | | | |
| | | 12mA type | $V_{CC} \geq 4.5V$ $I_{OL} = 12mA$ | V_{SS} | - | 0.4 | V | |
| | | | $V_{CC} < 4.5V$ $I_{OL} = 8mA$ | | | | | |
| | | P80, P81 | $V_{CC} \geq 4.5V$ $I_{OL} = 18.5mA$ | V_{SS} | - | 0.4 | V | |
| | | | $V_{CC} < 4.5V$ $I_{OL} = 10.5mA$ | | | | | |
| Input leak current | I_{IL} | - | - | -5 | - | +5 | μA | |
| Pull-up resistance value | R_{PU} | Pull-up pin | $V_{CC} \geq 4.5V$ | 25 | 50 | 100 | k Ω | |
| | | | $V_{CC} < 4.5V$ | 80 | 80 | 200 | | |
| Input capacitance | C_{IN} | Other than V_{CC} , V_{SS} , AV_{CC} , AV_{SS} , $AVRH$ | - | - | 5 | 15 | pF | |

4. AC Characteristics

(1) Main Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 105°C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks | |
|--|--------------------------------------|-----------|------------------------|--|-----|------|--------------------------------------|---------------------------|
| | | | | Min | Max | | | |
| Input frequency | F _{CH} | X0, X1 | V _{CC} ≥ 4.5V | 4 | 48 | MHz | When crystal oscillator is connected | |
| | | | V _{CC} < 4.5V | 4 | 20 | | | |
| | | | V _{CC} ≥ 4.5V | 4 | 48 | MHz | | |
| | | | V _{CC} < 4.5V | 4 | 20 | | | |
| Input clock cycle | t _{CY_{LH}} | | V _{CC} ≥ 4.5V | 20.83 | 250 | ns | When using external clock | |
| | | | V _{CC} < 4.5V | 50 | 250 | | | |
| Input clock pulse width | - | | | P _{WH} /t _{CY_{LH}} , P _{WL} /t _{CY_{LH}} | 45 | 55 | % | When using external clock |
| Input clock rising time and falling time | t _{CF} , t _{CR} | | | - | - | 5 | ns | When using external clock |
| Internal operating clock frequency | F _{CM} | - | - | - | 40 | MHz | Master clock | |
| | F _{CC} | - | - | - | 40 | MHz | Base clock (HCLK/FCLK) | |
| | F _{CP0} | - | - | - | 40 | MHz | APB0 bus clock (PCLK0) | |
| | F _{CP1} | - | - | - | 40 | MHz | APB1 bus clock (PCLK1) | |
| | F _{CP2} | - | - | - | 40 | MHz | APB2 bus clock (PCLK2) | |
| Internal operating clock cycle time | t _{CY_{CC}} | - | - | 25 | - | ns | Base clock (HCLK/FCLK) | |
| | t _{CY_{CP0}} | - | - | 25 | - | ns | APB0 bus clock (PCLK0) | |
| | t _{CY_{CP1}} | - | - | 25 | - | ns | APB1 bus clock (PCLK1) | |
| | t _{CY_{CP2}} | - | - | 25 | - | ns | APB2 bus clock (PCLK2) | |



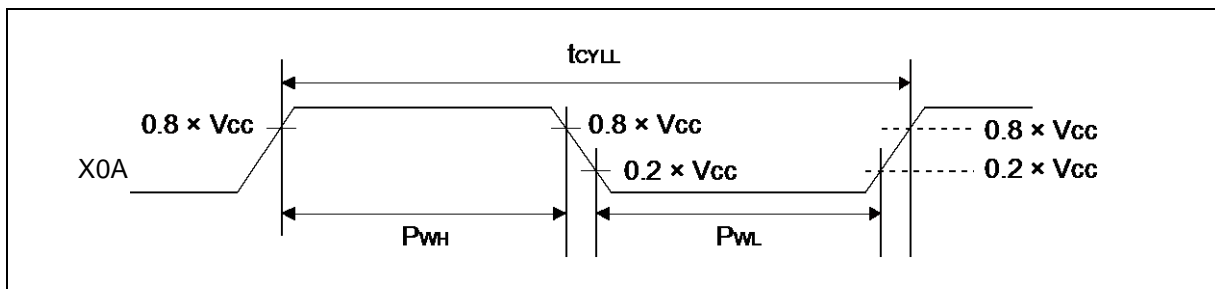
Note: For about each APB bus which each peripheral is connected to, see "■BLOCK DIAGRAM" in this data sheet.

For more information about each internal operating clock, see "Chapter: Clock" in "FM3 Family PERIPHERAL MANUAL".

(2) Sub Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 105°C)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|-------------------------|-------------------|-------------|--|-------|--------|-------|------|--------------------------------------|
| | | | | Min | Typ | Max | | |
| Input frequency | F _{CL} | X0A, X1A | - | - | 32.768 | - | kHz | When crystal oscillator is connected |
| | | | - | 32 | - | 100 | kHz | When using external clock |
| Input clock cycle | t _{CYLL} | | - | 10 | - | 31.25 | μs | When using external clock |
| Input clock pulse width | - | | P _{WH} /t _{CYLL} , P _{WL} /t _{CYLL} | 45 | - | 55 | % | When using external clock |



(3) Built-in CR Oscillation Characteristics

- Built-in high-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 105°C)

| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|-----------------|------------------|------------------------------------|-------|-----|------|------|-------------------|
| | | | Min | Typ | Max | | |
| Clock frequency | F _{CRH} | T _a = + 25°C | 3.96 | 4 | 4.04 | MHz | When trimming* |
| | | T _a = 0°C to + 70°C | 3.84 | 4 | 4.16 | | |
| | | T _a = - 40°C to + 105°C | 3.8 | 4 | 4.2 | | When not trimming |
| | | T _a = - 40°C to + 105°C | 3 | 4 | 5 | | |

*: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming.

- Built-in low-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 105°C)

| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|-----------------|------------------|------------|-------|-----|-----|------|---------|
| | | | Min | Typ | Max | | |
| Clock frequency | F _{CRL} | - | 50 | 100 | 150 | kHz | |

(4-1) Operating Conditions of Main PLL (In the case of using main clock for input clock of PLL)
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 105°C)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|-------------------|-------|-----|-----|------------|---------|
| | | Min | Typ | Max | | |
| PLL oscillation stabilization wait time (LOCK UP time)* | t _{LOCK} | 100 | - | - | μs | |
| PLL input clock frequency | F _{PLLI} | 4 | - | 16 | MHz | |
| PLL multiplication rate | - | 13 | - | 75 | multiplier | |
| PLL macro oscillation clock frequency | F _{PLLO} | 200 | - | 300 | MHz | |

*: Time from when the PLL starts operating until the oscillation stabilizes.

(4-2) Operating Conditions of Main PLL (In the case of using built-in high-speed CR clock for the input clock of the main PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 105°C)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|-------------------|-------|-----|-----|------------|---------|
| | | Min | Typ | Max | | |
| PLL oscillation stabilization wait time (LOCK UP time)* | t _{LOCK} | 100 | - | - | μs | |
| PLL input clock frequency | F _{PLLI} | 3.8 | 4 | 4.2 | MHz | |
| PLL multiplication rate | - | 50 | - | 71 | multiplier | |
| PLL macro oscillation clock frequency | F _{PLLO} | 190 | - | 300 | MHz | |

*: Time from when the PLL starts operating until the oscillation stabilizes.

Note: Make sure to input the built-in high-speed CR clock that has been trimmed.

When setting PLL multiplication rate, please take the accuracy of the built-in high-speed CR into account and prevent the master clock from exceeding the maximum frequency.

(5) Reset Input Characteristics

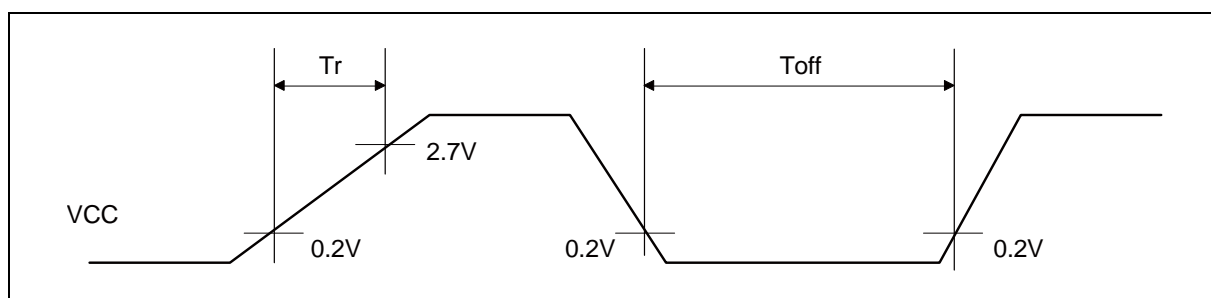
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 105°C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|------------------|--------------------|----------|------------|-------|-----|------|---------|
| | | | | Min | Max | | |
| Reset input time | t _{INITX} | INITX | - | 500 | - | ns | |

(6) Power-on Reset Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 105°C)

| Parameter | Symbol | Pin name | Value | | Unit | Remarks |
|-----------------------------|--------|----------|-------|-----|------|---------|
| | | | Min | Max | | |
| Power supply rising time | Tr | VCC | 0 | - | ms | |
| Power supply shut down time | Toff | | 1 | - | ms | |



(7) External Bus Timing

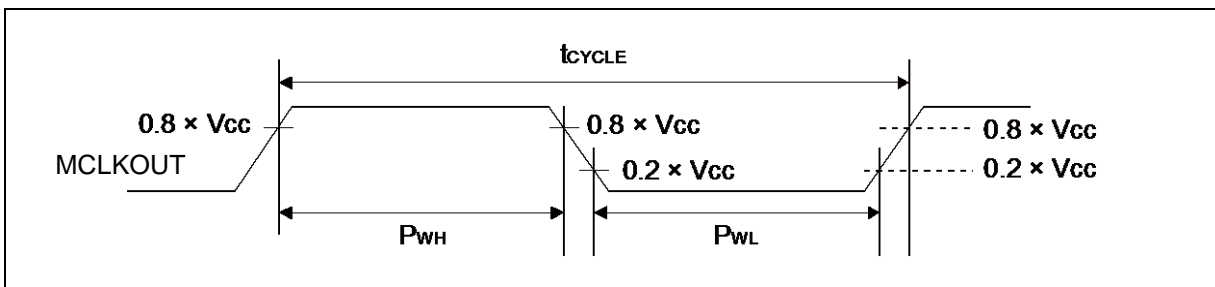
- External bus clock output Characteristics

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40^{\circ}C$ to $+105^{\circ}C$)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|--------------------------|-------------|----------|--------------------|-------|-----|------|
| | | | | Min | Max | |
| Output frequency | t_{CYCLE} | MCLKOUT | $V_{CC} \geq 4.5V$ | - | 40 | MHz |
| | | | $V_{CC} < 4.5V$ | - | 32 | MHz |
| Minimum clock cycle time | - | | $V_{CC} \geq 4.5V$ | 25 | - | ns |
| | | | $V_{CC} < 4.5V$ | 31.25 | - | ns |

Note: The external bus clock output is the divided clock of HCLK. For more information about settings of clock divider, see "Chapter: External Bus Interface" in "FM3 Family PERIPHERAL MANUAL".

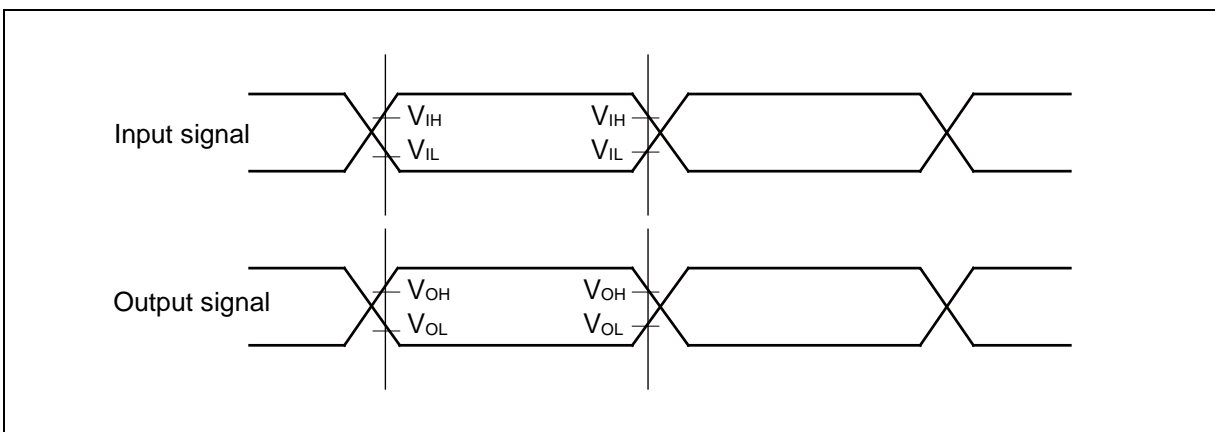
When the external bus clock is not output, this characteristics does not give any effect on external bus operation.



- External bus signal input/output Characteristics

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40^{\circ}C$ to $+105^{\circ}C$)

| Parameter | Symbol | Conditions | Value | Unit | Remarks |
|-------------------------------|----------|------------|---------------------|------|---------|
| Signal input characteristics | V_{IH} | - | $0.8 \times V_{CC}$ | V | |
| | V_{IL} | | $0.2 \times V_{CC}$ | V | |
| Signal output characteristics | V_{OH} | | $0.8 \times V_{CC}$ | V | |
| | V_{OL} | | $0.2 \times V_{CC}$ | V | |

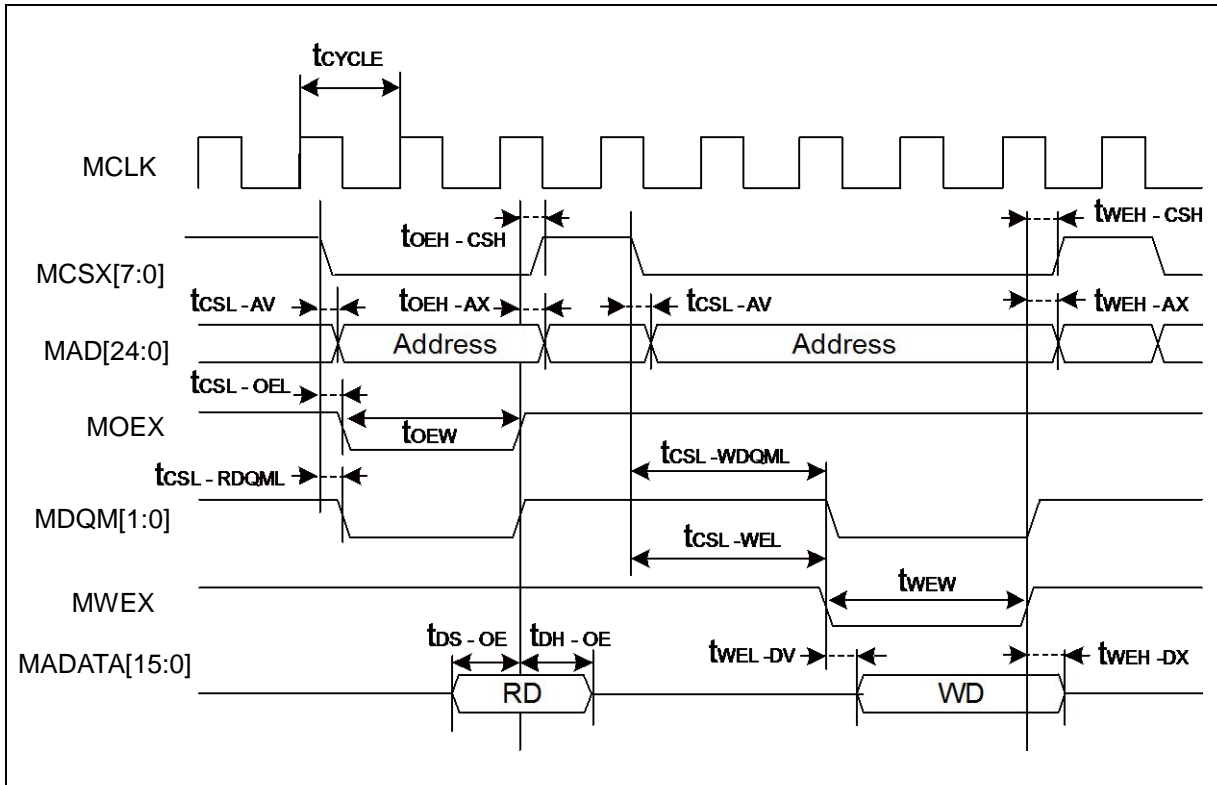


• Separate Bus Access Asynchronous SRAM Mode

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40^{\circ}C$ to $+105^{\circ}C$)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|---------------------|-------------------------|---------------------------------------|---|---|------|
| | | | | Min | Max | |
| MOEX Min pulse width | $t_{OE\bar{W}}$ | MOEX | $V_{CC} \geq 4.5V$ $V_{CC} < 4.5V$ | MCLK \times n-3 | - | ns |
| MCSX $\downarrow \rightarrow$ Address output delay time | t_{CSL-AV} | MCSX[7:0], MAD[24:0] | $V_{CC} \geq 4.5V$ $V_{CC} < 4.5V$ | - 9 - 12 | + 9 + 12 | ns |
| MOEX $\uparrow \rightarrow$ Address hold time | $t_{OE\bar{H}-AX}$ | MOEX, MAD[24:0] | $V_{CC} \geq 4.5V$ $V_{CC} < 4.5V$ | 0 | MCLK \times m+9 MCLK \times m+12 | ns |
| MCSX $\downarrow \rightarrow$ MOEX \downarrow delay time | $t_{CSL-OEL}$ | MOEX, MCSX[7:0] | $V_{CC} \geq 4.5V$ $V_{CC} < 4.5V$ | MCLK \times m-9 MCLK \times m-12 | MCLK \times m+9 MCLK \times m+12 | ns |
| MOEX $\uparrow \rightarrow$ MCSX \uparrow time | $t_{OE\bar{H}-OSH}$ | | $V_{CC} \geq 4.5V$ $V_{CC} < 4.5V$ | 0 | MCLK \times m+9 MCLK \times m+12 | ns |
| MCSX $\downarrow \rightarrow$ MDQM \downarrow delay time | $t_{CSL-RDQML}$ | MOEX, MDQM[1:0] | $V_{CC} \geq 4.5V$ $V_{CC} < 4.5V$ | MCLK \times m-9 MCLK \times m-12 | MCLK \times m+9 MCLK \times m+12 | ns |
| Data set up \rightarrow MOEX \uparrow time | t_{DS-OE} | MOEX, MADATA[15:0] | $V_{CC} \geq 4.5V$ $V_{CC} < 4.5V$ | 20 38 | - - | ns |
| MOEX $\uparrow \rightarrow$ Data hold time | t_{DH-OE} | MOEX, MADATA[15:0] | $V_{CC} \geq 4.5V$ $V_{CC} < 4.5V$ | 0 | - | ns |
| MWEX Min pulse width | $t_{WE\bar{W}}$ | MWEX | $V_{CC} \geq 4.5V$ $V_{CC} < 4.5V$ | MCLK \times n-3 | - | ns |
| MWEX $\uparrow \rightarrow$ Address output delay time | $t_{WE\bar{H}-AX}$ | MWEX, MAD[24:0] | $V_{CC} \geq 4.5V$ $V_{CC} < 4.5V$ | 0 | MCLK \times m+9 MCLK \times m+12 | ns |
| MCSX $\downarrow \rightarrow$ MWEX \downarrow delay time | $t_{CSL-WEL}$ | MWEX, MCSX[7:0] | $V_{CC} \geq 4.5V$ $V_{CC} < 4.5V$ | MCLK \times n-9 MCLK \times n-12 | MCLK \times n+9 MCLK \times n+12 | ns |
| MWEX $\uparrow \rightarrow$ MCSX \uparrow delay time | $t_{WE\bar{H}-CSH}$ | | $V_{CC} \geq 4.5V$ $V_{CC} < 4.5V$ | 0 | MCLK \times m+9 MCLK \times m+12 | ns |
| MCSX $\downarrow \rightarrow$ MDQM \downarrow delay time | $t_{CSL-WDQML}$ | MCSX, MDQM[1:0] | $V_{CC} \geq 4.5V$ $V_{CC} < 4.5V$ | MCLK \times n-9 MCLK \times n-12 | MCLK \times n+9 MCLK \times n+12 | ns |
| MWEX $\downarrow \rightarrow$ Data output time | t_{WEL-DV} | MWEX, MADATA[15:0] | $V_{CC} \geq 4.5V$ $V_{CC} < 4.5V$ | - 9 - 12 | + 9 + 12 | ns |
| MWEX $\uparrow \rightarrow$ Data hold time | $t_{WE\bar{H}-DX}$ | | $V_{CC} \geq 4.5V$ $V_{CC} < 4.5V$ | 0 | MCLK \times m+9 MCLK \times m+12 | ns |

Note: When the external load capacitance $C_L = 30pF$ ($m = 0$ to 15 , $n = 1$ to 16).

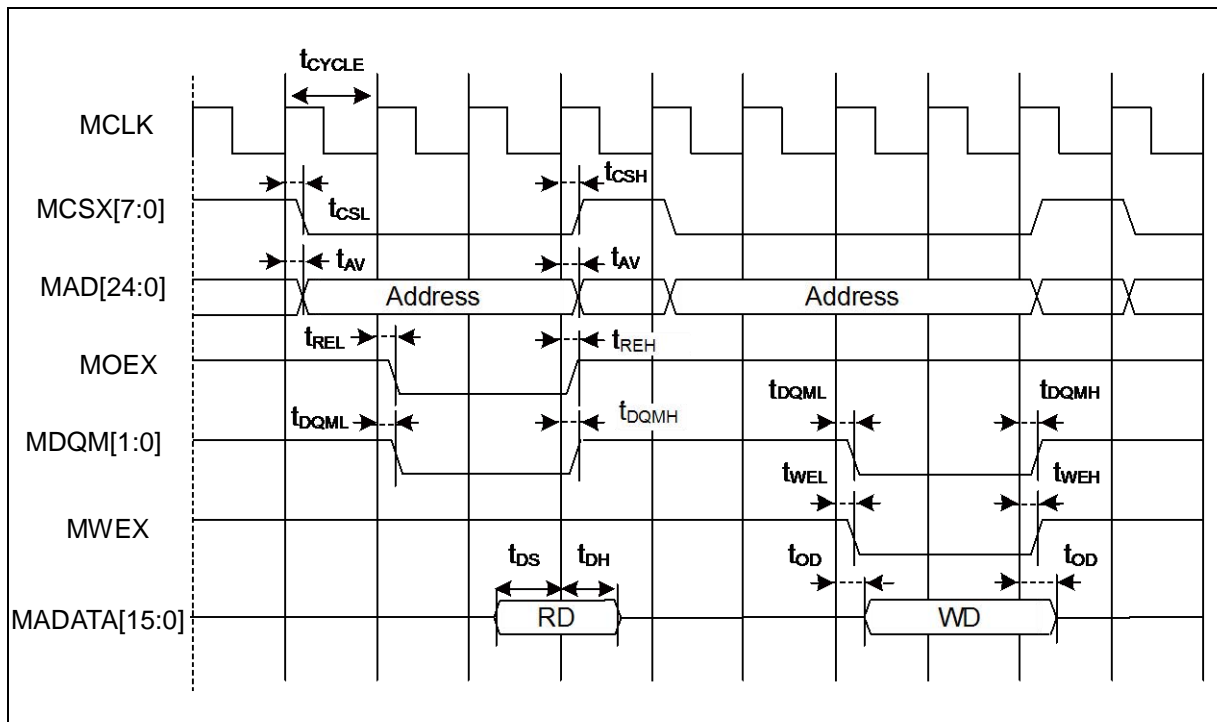


• Separate Bus Access Synchronous SRAM Mode

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40^{\circ}C$ to $+105^{\circ}C$)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|---|------------|-----------------------|--------------------|-------|-----|------|
| | | | | Min | Max | |
| Address delay time | t_{AV} | MCLK, MAD[24:0] | $V_{CC} \geq 4.5V$ | 1 | 9 | ns |
| | | | $V_{CC} < 4.5V$ | | 12 | |
| MCSX delay time | t_{CSL} | MCLK, MCSX[7:0] | $V_{CC} \geq 4.5V$ | 1 | 9 | ns |
| | | | $V_{CC} < 4.5V$ | | 12 | |
| | t_{CSH} | | $V_{CC} \geq 4.5V$ | 1 | 9 | ns |
| | | | $V_{CC} < 4.5V$ | | 12 | |
| MOEX delay time | t_{REL} | MCLK, MOEX | $V_{CC} \geq 4.5V$ | 1 | 9 | ns |
| | | | $V_{CC} < 4.5V$ | | 12 | |
| | t_{REH} | | $V_{CC} \geq 4.5V$ | 1 | 9 | ns |
| | | | $V_{CC} < 4.5V$ | | 12 | |
| Data set up \rightarrow MCLK \uparrow time | t_{DS} | MCLK, MADATA[15:0] | $V_{CC} \geq 4.5V$ | 19 | - | ns |
| | | | $V_{CC} < 4.5V$ | 37 | | |
| MCLK $\uparrow \rightarrow$ Data hold time | t_{DH} | MCLK, MADATA[15:0] | $V_{CC} \geq 4.5V$ | 0 | - | ns |
| | | | $V_{CC} < 4.5V$ | | | |
| MWEX delay time | t_{WEL} | MCLK, MWEX | $V_{CC} \geq 4.5V$ | 1 | 9 | ns |
| | | | $V_{CC} < 4.5V$ | | 12 | |
| | t_{WEH} | | $V_{CC} \geq 4.5V$ | 1 | 9 | ns |
| | | | $V_{CC} < 4.5V$ | | 12 | |
| MDQM[1:0] delay time | t_{DQML} | MCLK, MDQM[1:0] | $V_{CC} \geq 4.5V$ | 1 | 9 | ns |
| | | | $V_{CC} < 4.5V$ | | 12 | |
| | t_{DQMH} | | $V_{CC} \geq 4.5V$ | 1 | 9 | ns |
| | | | $V_{CC} < 4.5V$ | | 12 | |
| MCLK $\uparrow \rightarrow$ Data output time | t_{OD} | MCLK, MADATA[15:0] | $V_{CC} \geq 4.5V$ | 2 | 18 | ns |
| | | | $V_{CC} < 4.5V$ | 2 | 24 | |

Note: When the external load capacitance $C_L = 30pF$.

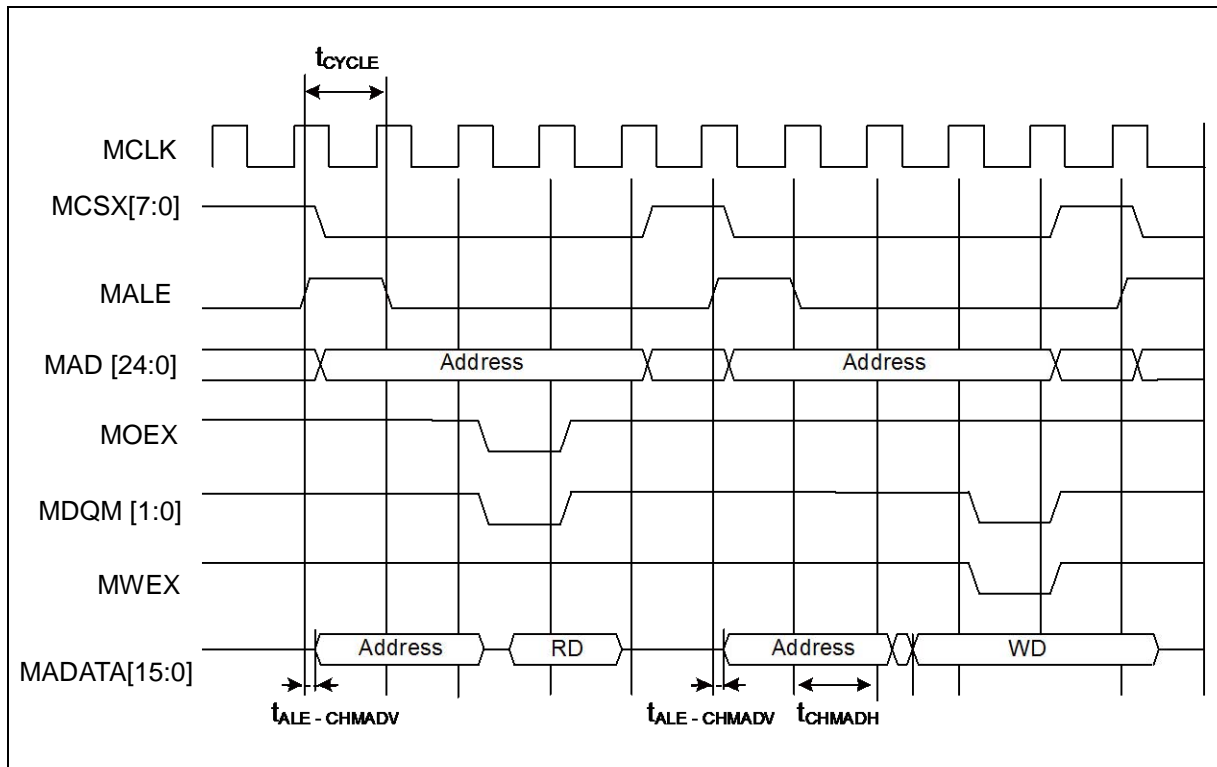


• Multiplexed Bus Access Asynchronous SRAM Mode

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40^{\circ}C$ to $+105^{\circ}C$)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|--------------------------------|------------------|--------------------|--------------------|---------------------|----------------------|------|
| | | | | Min | Max | |
| Multiplexed Address delay time | $t_{ALE-CHMADV}$ | MALE, MADATA[15:0] | $V_{CC} \geq 4.5V$ | 0 | 10 | ns |
| | | | $V_{CC} < 4.5V$ | | 20 | |
| Multiplexed Address hold time | t_{CHMADH} | MALE, MADATA[15:0] | $V_{CC} \geq 4.5V$ | $MCLK \times n + 0$ | $MCLK \times n + 10$ | ns |
| | | | $V_{CC} < 4.5V$ | $MCLK \times n + 0$ | $MCLK \times n + 20$ | |

Note: When the external load capacitance $C_L = 30pF$ ($m = 0$ to 15 , $n = 1$ to 16).

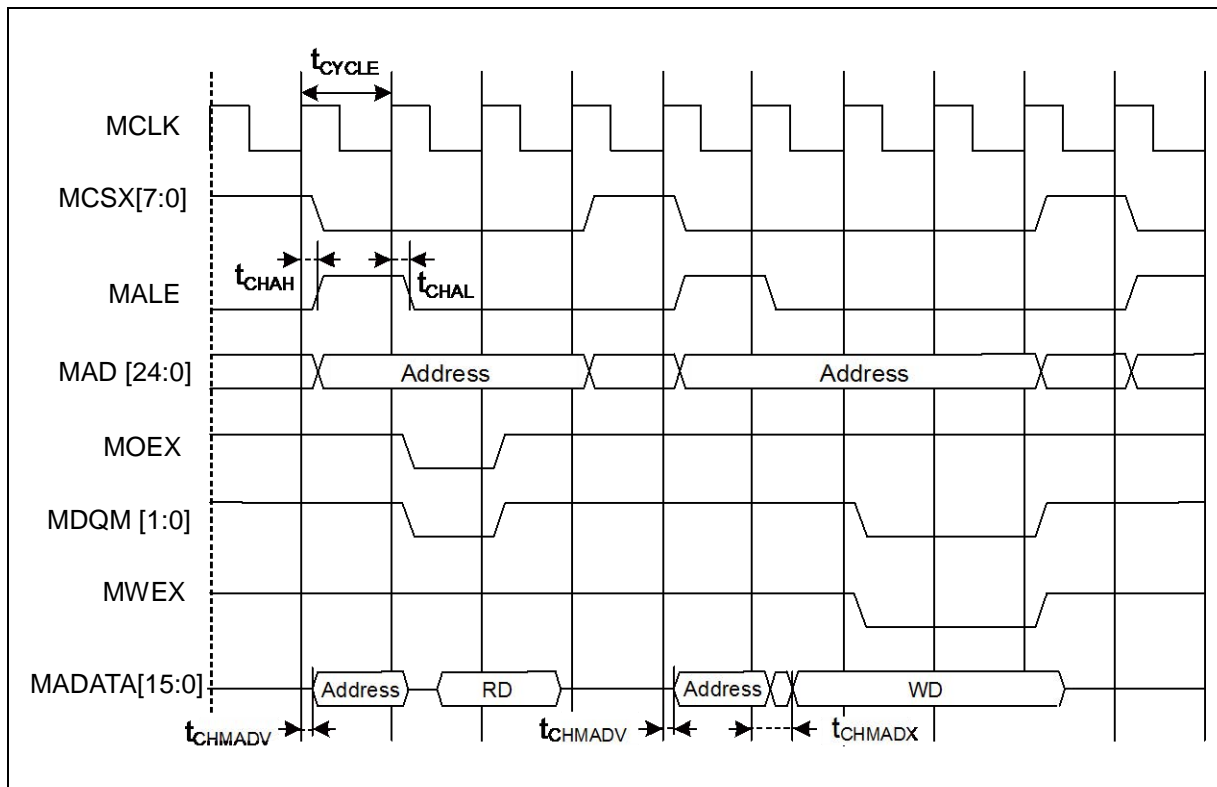


• Multiplexed Bus Access Synchronous SRAM Mode

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40^{\circ}C$ to $+105^{\circ}C$)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|--|--------------|-----------------------|--------------------|-------|----------|------|---------|
| | | | | Min | Max | | |
| MALE delay time | t_{CHAL} | MCLK, ALE | $V_{CC} \geq 4.5V$ | 1 | 9 | ns | |
| | | | $V_{CC} < 4.5V$ | | 12 | | |
| | t_{CHAH} | | $V_{CC} \geq 4.5V$ | 1 | 9 | ns | |
| | | | $V_{CC} < 4.5V$ | | 12 | | |
| MCLK $\uparrow \rightarrow$ Multiplexed Address delay time | t_{CHMADV} | MCLK, MADATA[15:0] | $V_{CC} \geq 4.5V$ | 1 | t_{OD} | ns | |
| | | | $V_{CC} < 4.5V$ | | | | |
| MCLK $\uparrow \rightarrow$ Multiplexed Data output time | t_{CHMADX} | | $V_{CC} \geq 4.5V$ | 1 | t_{OD} | ns | |
| | | | $V_{CC} < 4.5V$ | | | | |

Note: When the external load capacitance $C_L = 30pF$.

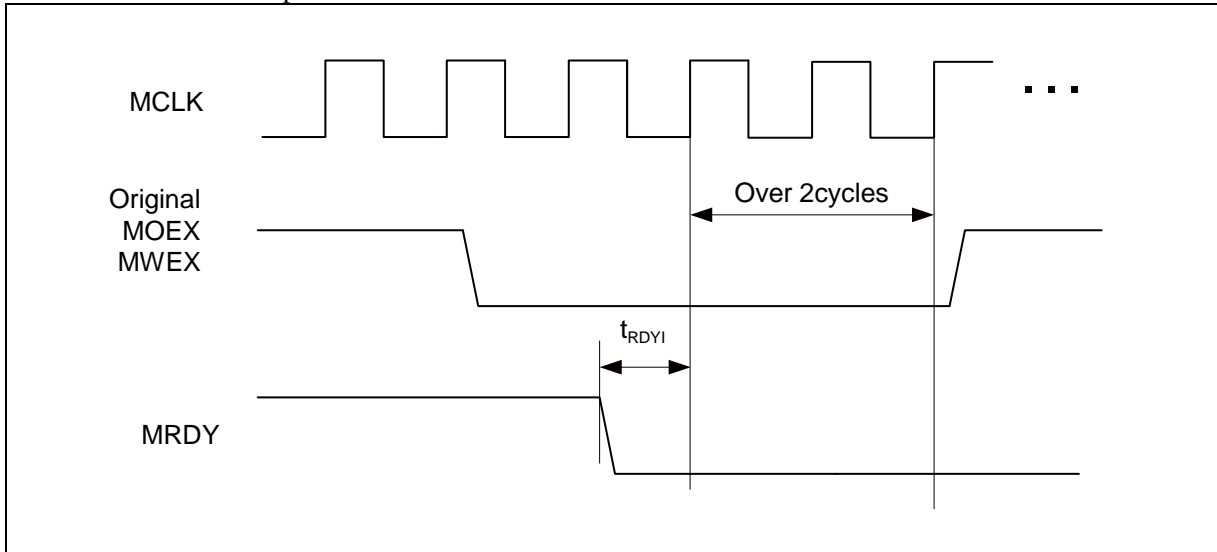


• External Ready Input Timing

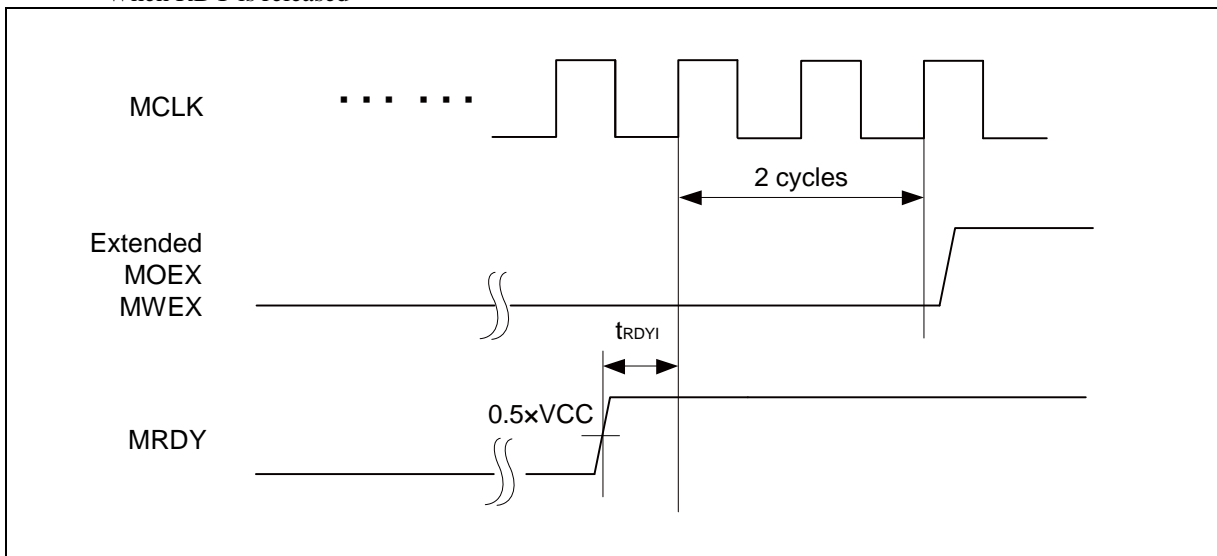
($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40^{\circ}C$ to $+105^{\circ}C$)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|------------|---------------|--------------------|-------|-----|------|---------|
| | | | | Min | Max | | |
| MCLK \uparrow MRDY input setup time | t_{RDYI} | MCLK, MRDY | $V_{CC} \geq 4.5V$ | 19 | - | ns | |
| | | | $V_{CC} < 4.5V$ | 37 | | | |

• When RDY is input



• When RDY is released

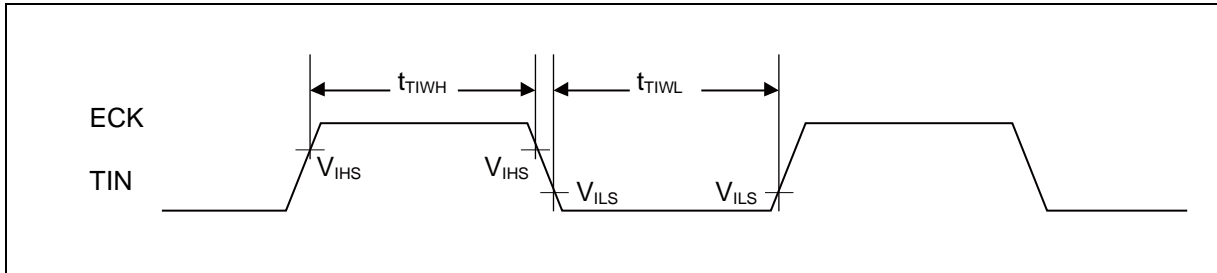


(8) Base Timer Input Timing

• Timer input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 105°C)

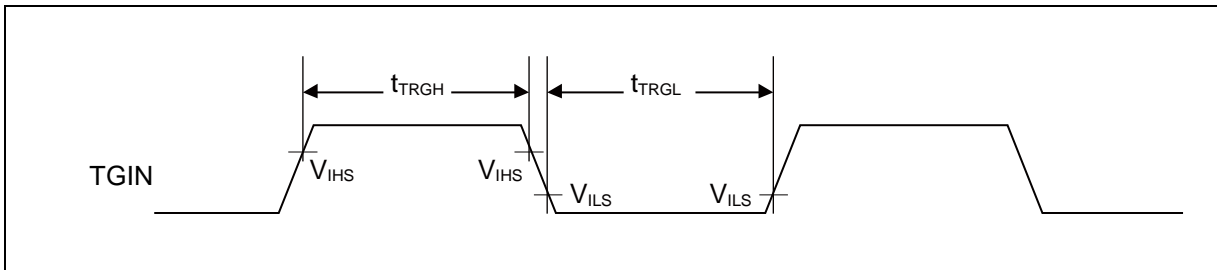
| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|-------------------|--|---|------------|--------------------|-----|------|---------|
| | | | | Min | Max | | |
| Input pulse width | t _{TIWH} , t _{TIWL} | TIOAn/TIOBn (when using as ECK,TIN) | - | 2t _{CYCP} | - | ns | |



• Trigger input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 105°C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|-------------------|--|--|------------|--------------------|-----|------|---------|
| | | | | Min | Max | | |
| Input pulse width | t _{TRGH} , t _{TRGL} | TIOAn/TIOBn (when using as TGIN) | - | 2t _{CYCP} | - | ns | |



Note: t_{CYCP} indicates the APB bus clock cycle time.

About the APB bus number which the base timer is connected to, see "■BLOCK DIAGRAM" in this data sheet.

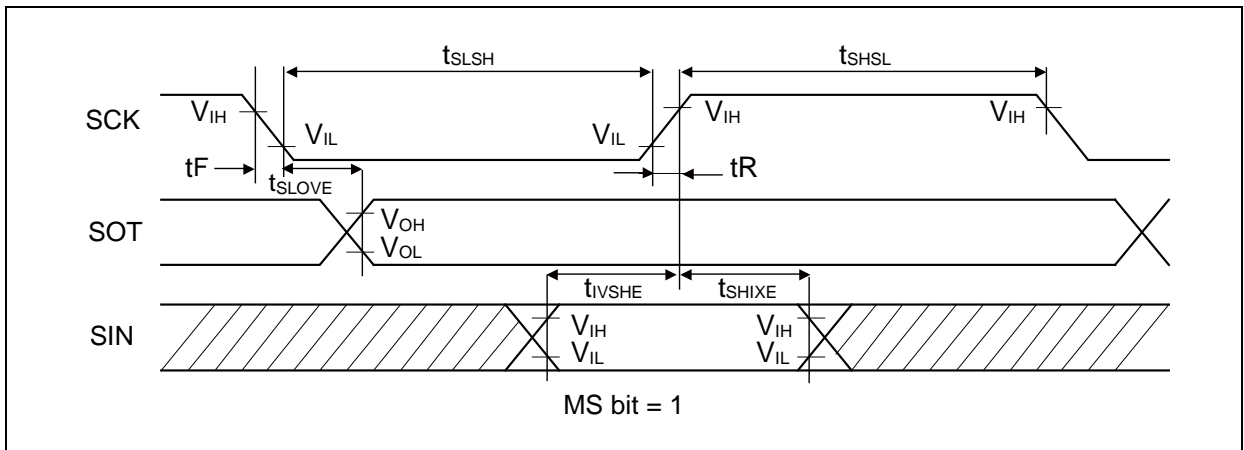
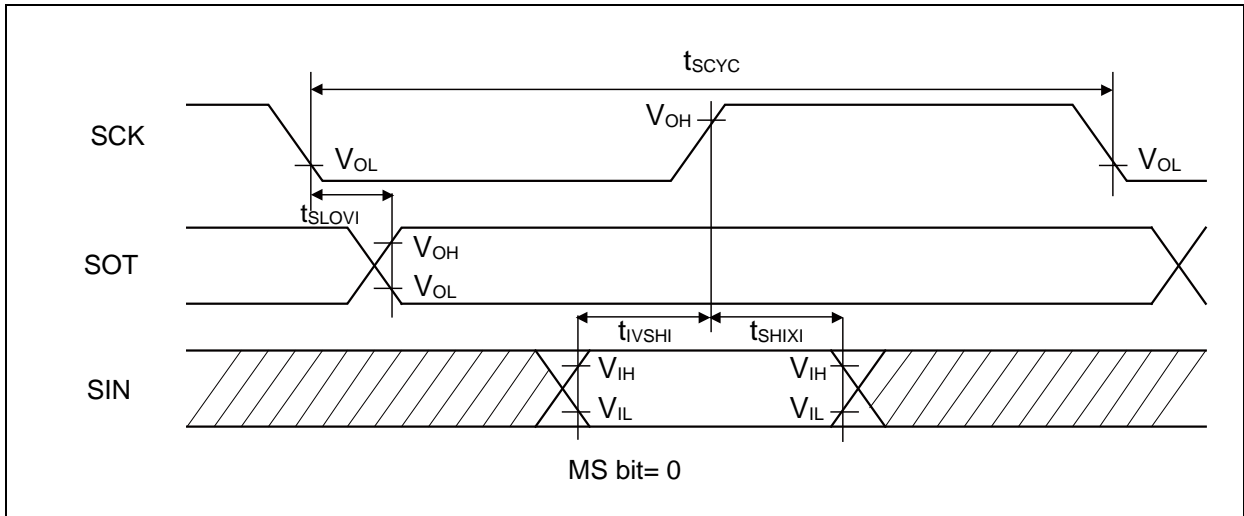
(9) UART Timing

- Synchronous serial (SPI = 0, SCINV = 0)

(Vcc = 2.7V to 5.5V, Vss = 0V, Ta = - 40°C to + 105°C)

| Parameter | Symbol | Pin name | Conditions | Vcc < 4.5V | | Vcc ≥ 4.5V | | Unit |
|------------------------------|--------------------|-------------------------------------|--------------------------------|-------------------------|------|-------------------------|------|------|
| | | | | Min | Max | Min | Max | |
| Serial clock cycle time | t _{SCYC} | SCK _X | Internal shift clock operation | 4t _{CYCP} | - | 4t _{CYCP} | - | ns |
| SCK ↓ → SOT delay time | t _{SLOVI} | SCK _X , SOT _X | | - 30 | + 30 | - 20 | + 20 | ns |
| SIN → SCK ↑ setup time | t _{IVSHI} | SCK _X , SIN _X | | 50 | - | 30 | - | ns |
| SCK ↑ → SIN hold time | t _{SHIXI} | SCK _X , SIN _X | | 0 | - | 0 | - | ns |
| Serial clock "L" pulse width | t _{SLSH} | SCK _X | External shift clock operation | 2t _{CYCP} - 10 | - | 2t _{CYCP} - 10 | - | ns |
| Serial clock "H" pulse width | t _{SHSL} | SCK _X | | t _{CYCP} + 10 | - | t _{CYCP} + 10 | - | ns |
| SCK ↓ → SOT delay time | t _{SLOVE} | SCK _X , SOT _X | | - | 50 | - | 30 | ns |
| SIN → SCK ↑ setup time | t _{IVSHE} | SCK _X , SIN _X | | 10 | - | 10 | - | ns |
| SCK ↑ → SIN hold time | t _{SHIXE} | SCK _X , SIN _X | | 20 | - | 20 | - | ns |
| SCK falling time | t _F | SCK _X | | - | 5 | - | 5 | ns |
| SCK rising time | t _R | SCK _X | | - | 5 | - | 5 | ns |

- Notes:
- The above characteristics apply to CLK synchronous mode.
 - t_{CYCP} indicates the APB bus clock cycle time. About the APB bus number which UART is connected to, see "■ BLOCK DIAGRAM" in this data sheet.
 - These characteristics only guarantee the same relocate port number.
For example, the combination of SCLK_{x_0} and SOT_{x_1} is not guaranteed.
 - When the external load capacitance C_L = 30pF.

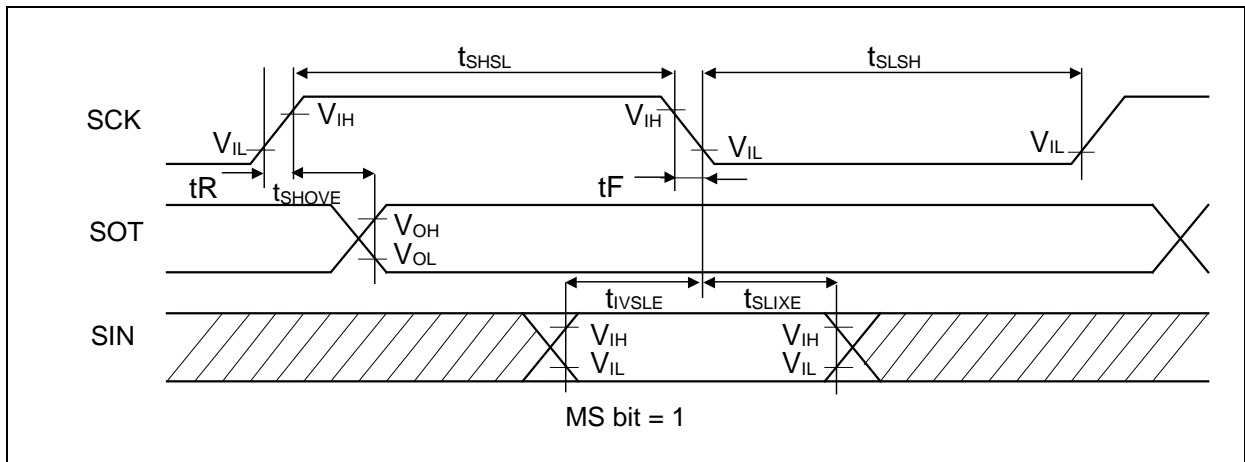
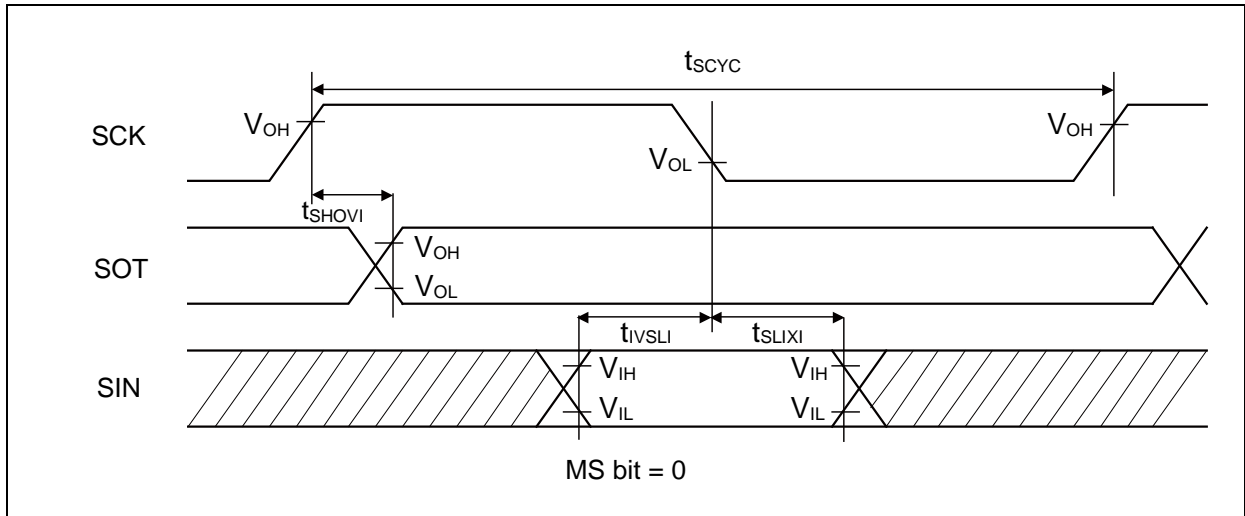


• Synchronous serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 105°C)

| Parameter | Symbol | Pin name | Conditions | V _{CC} < 4.5V | | V _{CC} ≥ 4.5V | | Unit |
|------------------------------|--------------------|-------------------------------------|--------------------------------|-------------------------|------|-------------------------|------|------|
| | | | | Min | Max | Min | Max | |
| Serial clock cycle time | t _{SCYC} | SCK _X | Internal shift clock operation | 4t _{CYCP} | - | 4t _{CYCP} | - | ns |
| SCK ↑ → SOT delay time | t _{SHOVI} | SCK _X , SOT _X | | - 30 | + 30 | - 20 | + 20 | ns |
| SIN → SCK ↓ setup time | t _{IVSLI} | SCK _X , SIN _X | | 50 | - | 30 | - | ns |
| SCK ↓ → SIN hold time | t _{SLIXI} | SCK _X , SIN _X | | 0 | - | 0 | - | ns |
| Serial clock "L" pulse width | t _{SLSH} | SCK _X | External shift clock operation | 2t _{CYCP} - 10 | - | 2t _{CYCP} - 10 | - | ns |
| Serial clock "H" pulse width | t _{SHSL} | SCK _X | | t _{CYCP} + 10 | - | t _{CYCP} + 10 | - | ns |
| SCK ↑ → SOT delay time | t _{SHOVE} | SCK _X , SOT _X | | - | 50 | - | 30 | ns |
| SIN → SCK ↓ setup time | t _{IVSLE} | SCK _X , SIN _X | | 10 | - | 10 | - | ns |
| SCK ↓ → SIN hold time | t _{SLIXE} | SCK _X , SIN _X | | 20 | - | 20 | - | ns |
| SCK falling time | t _F | SCK _X | | - | 5 | - | 5 | ns |
| SCK rising time | t _R | SCK _X | | - | 5 | - | 5 | ns |

- Notes:
- The above characteristics apply to CLK synchronous mode.
 - t_{CYCP} indicates the APB bus clock cycle time. About the APB bus number which UART is connected to, see "■ BLOCK DIAGRAM" in this data sheet.
 - These characteristics only guarantee the same relocate port number. For example, the combination of SCLK_{x_0} and SOT_{x_1} is not guaranteed.
 - When the external load capacitance C_L = 30pF.

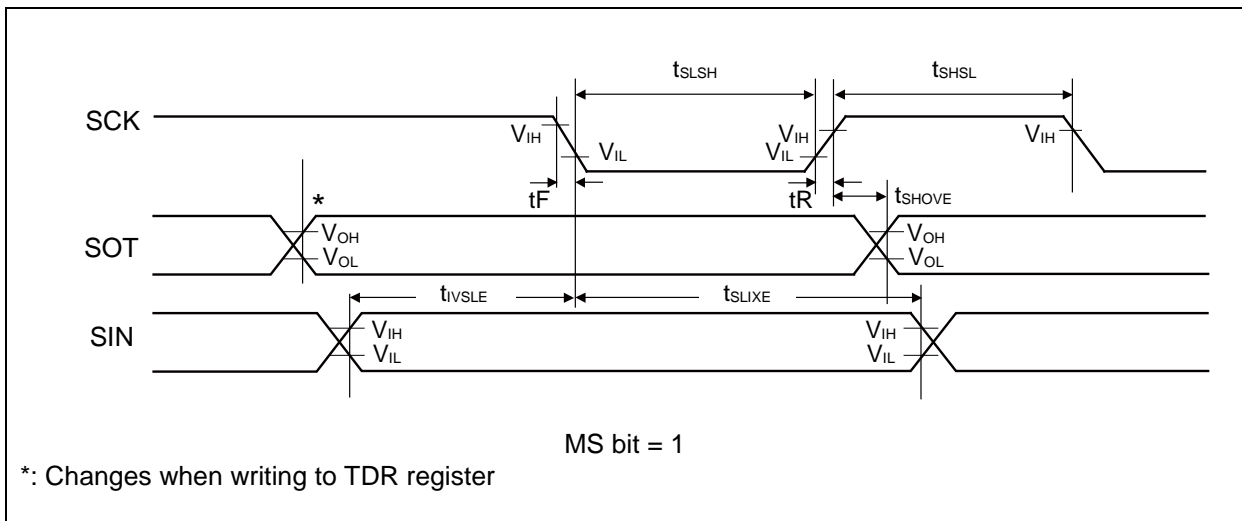
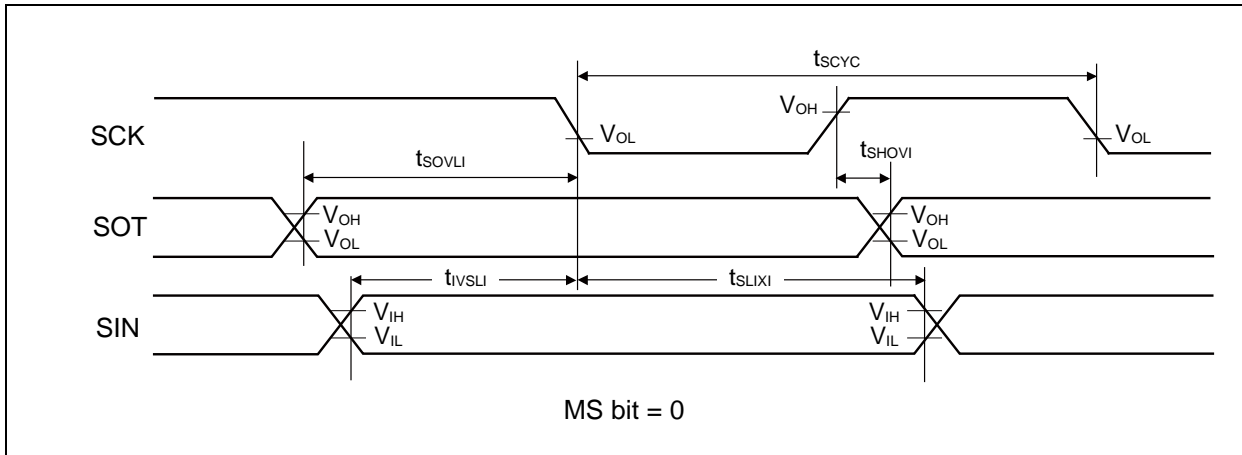


• Synchronous serial(SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, Ta = - 40°C to + 105°C)

| Parameter | Symbol | Pin name | Conditions | V _{CC} < 4.5V | | V _{CC} ≥ 4.5V | | Unit |
|------------------------------|--------------------|-------------------------------------|--------------------------------|-------------------------|------|-------------------------|------|------|
| | | | | Min | Max | Min | Max | |
| Serial clock cycle time | t _{SCYC} | SCK _X | Internal shift clock operation | 4t _{CYCP} | - | 4t _{CYCP} | - | ns |
| SCK ↑ → SOT delay time | t _{SHOVI} | SCK _X , SOT _X | | - 30 | + 30 | - 20 | + 20 | ns |
| SIN → SCK ↓ setup time | t _{IVSLI} | SCK _X , SIN _X | | 50 | - | 30 | - | ns |
| SCK ↓ → SIN hold time | t _{SLIXI} | SCK _X , SIN _X | | 0 | - | 0 | - | ns |
| SOT → SCK ↓ delay time | t _{SOVLI} | SCK _X , SOT _X | | 2t _{CYCP} - 30 | - | 2t _{CYCP} - 30 | - | ns |
| Serial clock "L" pulse width | t _{LSLH} | SCK _X | External shift clock operation | 2t _{CYCP} - 10 | - | 2t _{CYCP} - 10 | - | ns |
| Serial clock "H" pulse width | t _{SHSL} | SCK _X | | t _{CYCP} + 10 | - | t _{CYCP} + 10 | - | ns |
| SCK ↑ → SOT delay time | t _{SHOVE} | SCK _X , SOT _X | | - | 50 | - | 30 | ns |
| SIN → SCK ↓ setup time | t _{IVSLE} | SCK _X , SIN _X | | 10 | - | 10 | - | ns |
| SCK ↓ → SIN hold time | t _{SLIXE} | SCK _X , SIN _X | | 20 | - | 20 | - | ns |
| SCK falling time | t _F | SCK _X | | - | 5 | - | 5 | ns |
| SCK rising time | t _R | SCK _X | | - | 5 | - | 5 | ns |

- Notes:
- The above characteristics apply to CLK synchronous mode.
 - t_{CYCP} indicates the APB bus clock cycle time. About the APB bus number which UART is connected to, see "■ BLOCK DIAGRAM" in this data sheet.
 - These characteristics only guarantee the same relocate port number.
For example, the combination of SCLK_{x_0} and SOT_{x_1} is not guaranteed.
 - When the external load capacitance C_L = 30pF.

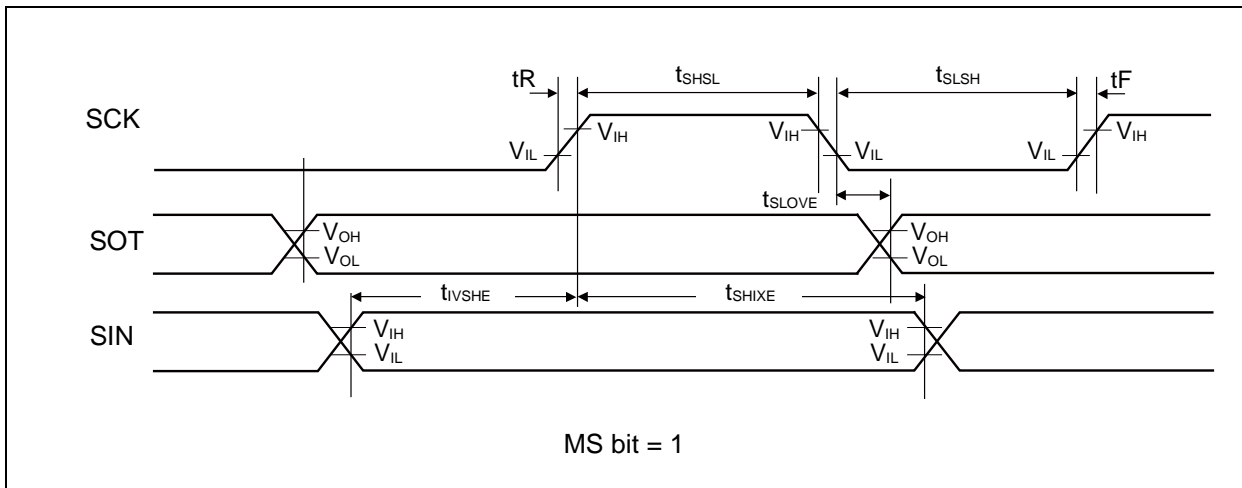
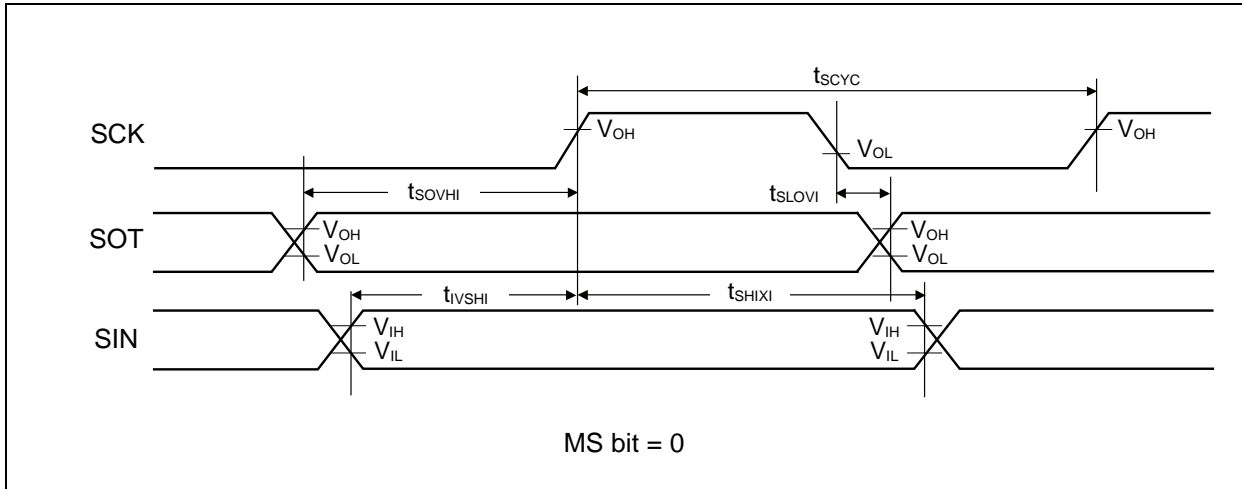


• Synchronous serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 105°C)

| Parameter | Symbol | Pin name | Conditions | V _{CC} < 4.5V | | V _{CC} ≥ 4.5V | | Unit |
|------------------------------|--------------------|-------------------------------------|--------------------------------|-------------------------|------|-------------------------|------|------|
| | | | | Min | Max | Min | Max | |
| Serial clock cycle time | t _{SCYC} | SCK _X | Internal shift clock operation | 4t _{CYCP} | - | 4t _{CYCP} | - | ns |
| SCK ↓ → SOT delay time | t _{SLOVI} | SCK _X , SOT _X | | - 30 | + 30 | - 20 | + 20 | ns |
| SIN → SCK ↑ setup time | t _{IVSHI} | SCK _X , SIN _X | | 50 | - | 30 | - | ns |
| SCK ↑ → SIN hold time | t _{SHIXI} | SCK _X , SIN _X | | 0 | - | 0 | - | ns |
| SOT → SCK ↑ delay time | t _{SOVHI} | SCK _X , SOT _X | | 2t _{CYCP} - 30 | - | 2t _{CYCP} - 30 | - | ns |
| Serial clock "L" pulse width | t _{SLSH} | SCK _X | External shift clock operation | 2t _{CYCP} - 10 | - | 2t _{CYCP} - 10 | - | ns |
| Serial clock "H" pulse width | t _{SHSL} | SCK _X | | t _{CYCP} + 10 | - | t _{CYCP} + 10 | - | ns |
| SCK ↓ → SOT delay time | t _{SLOVE} | SCK _X , SOT _X | | - | 50 | - | 30 | ns |
| SIN → SCK ↑ setup time | t _{IVSHE} | SCK _X , SIN _X | | 10 | - | 10 | - | ns |
| SCK ↑ → SIN hold time | t _{SHIXE} | SCK _X , SIN _X | | 20 | - | 20 | - | ns |
| SCK falling time | t _F | SCK _X | | - | 5 | - | 5 | ns |
| SCK rising time | t _R | SCK _X | | - | 5 | - | 5 | ns |

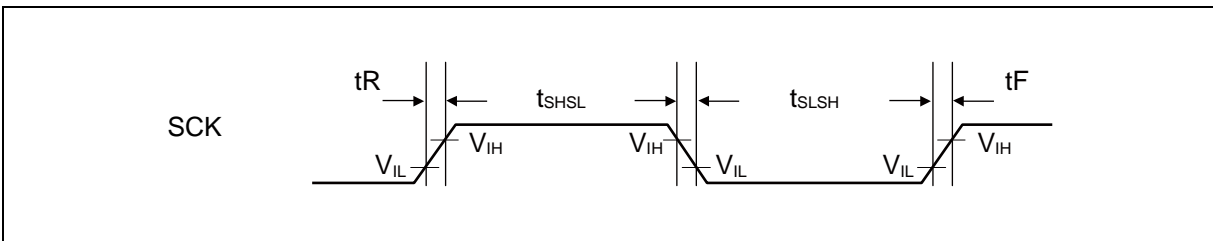
- Notes:
- The above characteristics apply to CLK synchronous mode.
 - t_{CYCP} indicates the APB bus clock cycle time. About the APB bus number which UART is connected to, see "■ BLOCK DIAGRAM" in this data sheet.
 - These characteristics only guarantee the same relocate port number.
For example, the combination of SCLK_{x_0} and SOT_{x_1} is not guaranteed.
 - When the external load capacitance C_L = 30pF.



• External clock (EXT = 1) : asynchronous only

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 105°C)

| Parameter | Symbol | Conditions | Value | | Unit | Remarks |
|------------------------------|-------------------|-----------------------|------------------------|-----|------|---------|
| | | | Min | Max | | |
| Serial clock "L" pulse width | t _{SLSH} | C _L = 30pF | t _{CYCP} + 10 | - | ns | |
| Serial clock "H" pulse width | t _{SHSL} | | t _{CYCP} + 10 | - | ns | |
| SCK falling time | t _F | | - | 5 | ns | |
| SCK rising time | t _R | | - | 5 | ns | |



(10) External Input Timing

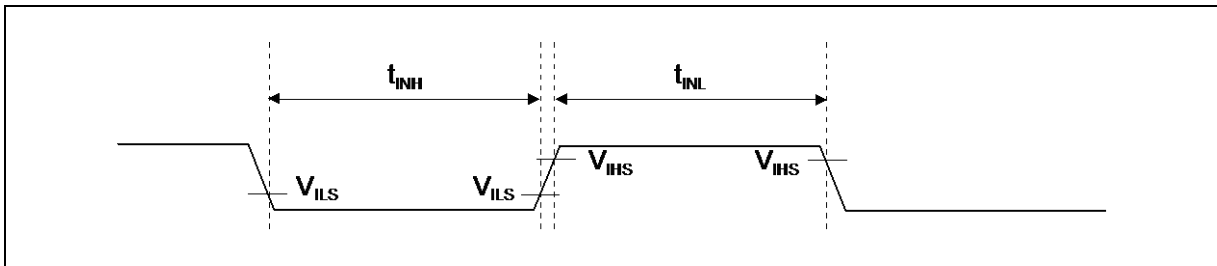
($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40^{\circ}C$ to $+105^{\circ}C$)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|-------------------|--------------------------|----------------------|------------|------------------|-----|------|-----------------------------|
| | | | | Min | Max | | |
| Input pulse width | t_{INH} , t_{INL} | ADTG | - | $2t_{CYCP}^{*1}$ | - | ns | A/D converter trigger input |
| | | FRCKx | | | | | Free-run timer input clock |
| | | ICxx | - | $2t_{CYCP}^{*1}$ | - | ns | Input capture |
| | | DTTIXX | | | | | Waveform generator |
| | | INT00 to INT15, NMIX | | | | | $2t_{CYCP} + 100^{*1}$ |
| | | | 500^{*2} | - | ns | NMI | |

*1: t_{CYCP} indicates the APB bus clock cycle time except stop when in stop mode, in timer mode.

About the APB bus number which the A/D converter, Multi-function Timer and External interrupt are connected to, see "BLOCK DIAGRAM" in this data sheet.

*2: When in stop mode, in timer mode.

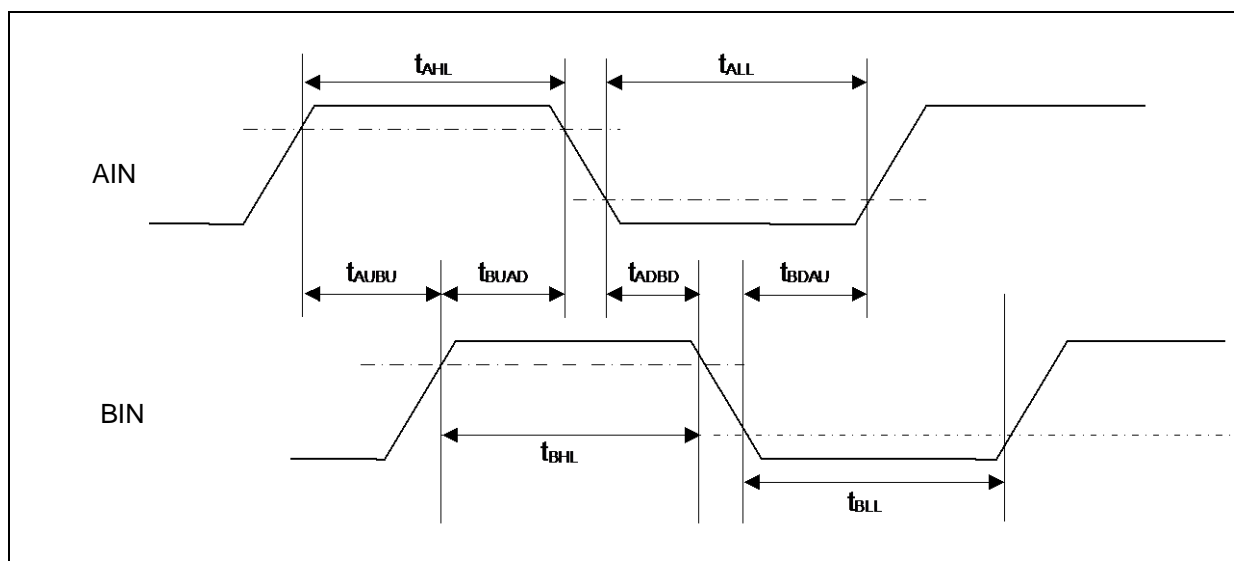


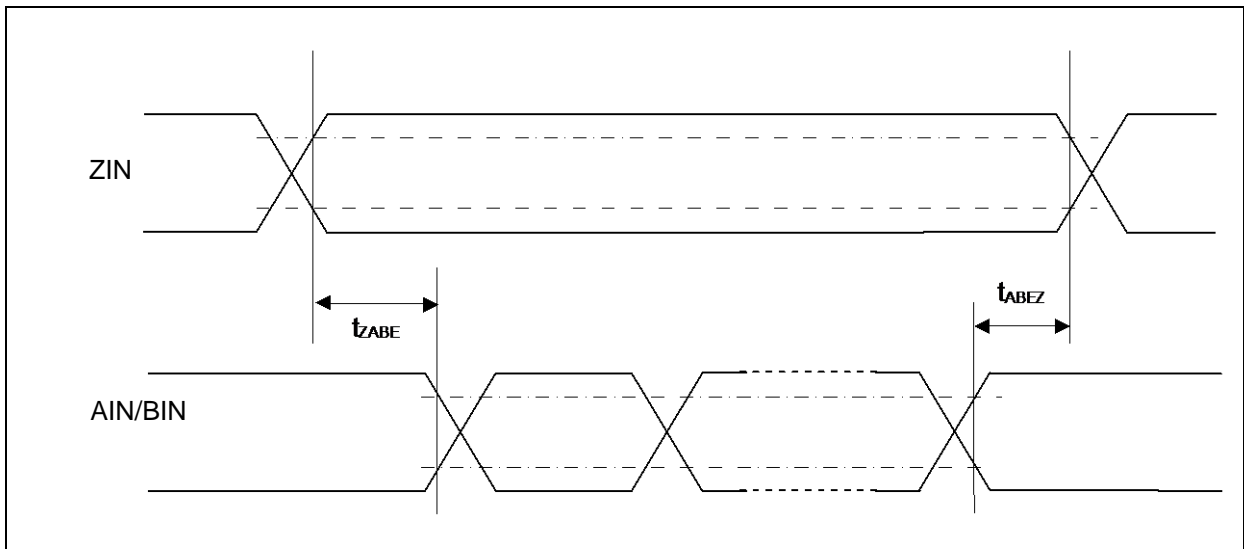
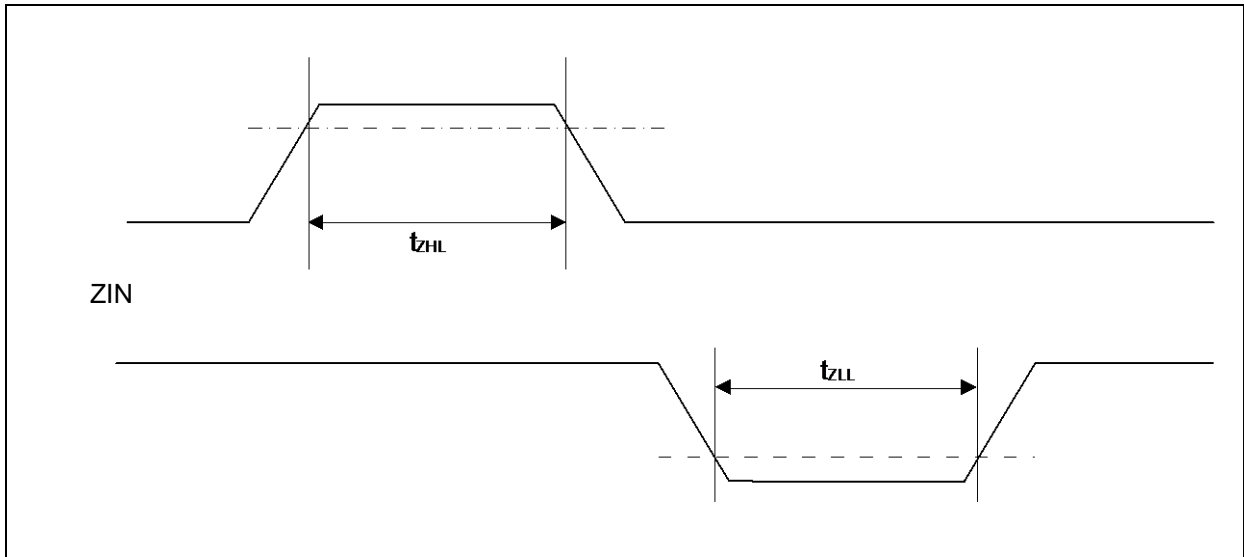
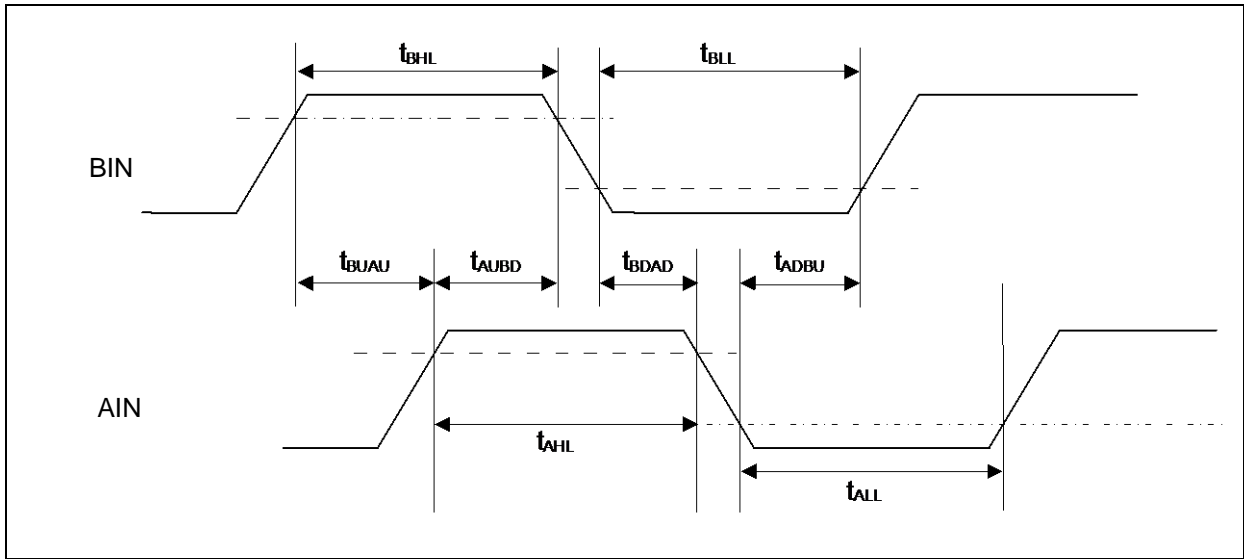
(11) Quadrature Position/Revolution Counter Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 105°C)

| Parameter | Symbol | Conditions | Value | | Unit |
|---|-------------------|----------------------|----------------------|-----|------|
| | | | Min | Max | |
| AIN pin "H" width | t _{AHL} | - | 2t _{CYCP} * | - | ns |
| AIN pin "L" width | t _{ALL} | - | | | |
| BIN pin "H" width | t _{BHL} | - | | | |
| BIN pin "L" width | t _{BLL} | - | | | |
| BIN rising time from AIN pin "H" level | t _{AUBU} | PC_Mode2 or PC_Mode3 | | | |
| AIN falling time from BIN pin "H" level | t _{BUAD} | PC_Mode2 or PC_Mode3 | | | |
| BIN falling time from AIN pin "L" level | t _{ADBD} | PC_Mode2 or PC_Mode3 | | | |
| AIN rising time from BIN pin "L" level | t _{BDAU} | PC_Mode2 or PC_Mode3 | | | |
| AIN rising time from BIN pin "H" level | t _{BUAU} | PC_Mode2 or PC_Mode3 | | | |
| BIN falling time from AIN pin "H" level | t _{AUBD} | PC_Mode2 or PC_Mode3 | | | |
| AIN falling time from BIN pin "L" level | t _{BDAD} | PC_Mode2 or PC_Mode3 | | | |
| BIN rising time from AIN pin "L" level | t _{ADBU} | PC_Mode2 or PC_Mode3 | | | |
| ZIN pin "H" width | t _{ZHL} | QCR:CGSC="0" | | | |
| ZIN pin "L" width | t _{ZLL} | QCR:CGSC="0" | | | |
| AIN/BIN rise and falling time from determined ZIN level | t _{ZABE} | QCR:CGSC="1" | | | |
| Determined ZIN level from AIN/BIN rise and falling time | t _{ABEZ} | QCR:CGSC="1" | | | |

* : t_{CYCP} indicates the APB bus clock cycle time except stop when in stop mode. About the APB bus number which QPRC is connected to, see "■BLOCK DIAGRAM" in this data sheet.





(12) I²C Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 105°C)

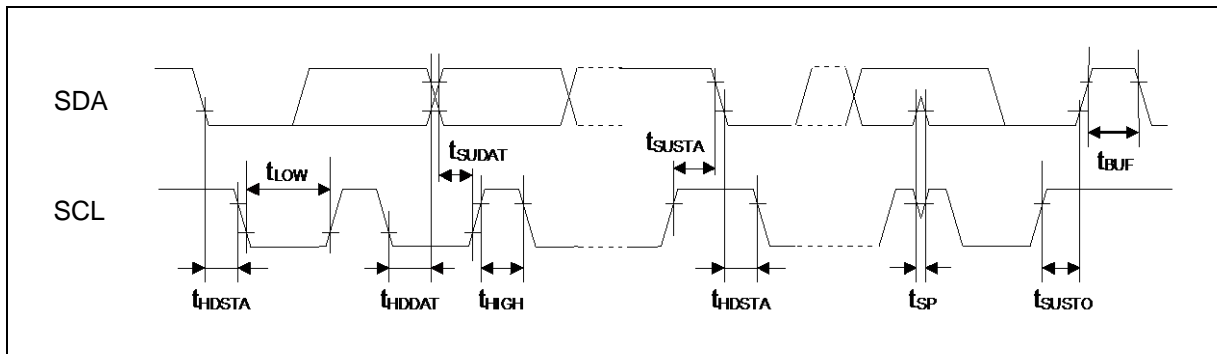
| Parameter | Symbol | Conditions | Typical mode | | High-speed mode | | Unit | Remark |
|--|--------------------|---|------------------------------------|--------------------|------------------------------------|-------------------|------|--------|
| | | | Min | Max | Min | Max | | |
| SCL clock frequency | F _{SCL} | C _L = 30pF, R = (V _p /I _{OL}) * ¹ | 0 | 100 | 0 | 400 | kHz | |
| (Repeated) START condition hold time SDA ↓ → SCL ↓ | t _{HDSTA} | | 4.0 | - | 0.6 | - | μs | |
| SCL clock "L" width | t _{LOW} | | 4.7 | - | 1.3 | - | μs | |
| SCL clock "H" width | t _{HIGH} | | 4.0 | - | 0.6 | - | μs | |
| (Repeated) START condition setup time SCL ↑ → SDA ↓ | t _{SUSTA} | | 4.7 | - | 0.6 | - | μs | |
| Data hold time SCL ↓ → SDA ↓ ↑ | t _{HDDAT} | | 0 | 3.45* ² | 0 | 0.9* ³ | μs | |
| Data setup time SDA ↓ ↑ → SCL ↑ | t _{SUDAT} | | 250 | - | 100 | - | ns | |
| STOP condition setup time SCL ↑ → SDA ↑ | t _{SUSTO} | | 4.0 | - | 0.6 | - | μs | |
| Bus free time between "STOP condition" and "START condition" | t _{BUF} | | 4.7 | - | 1.3 | - | μs | |
| Noise filter | t _{SP} | - | 2 t _{CYCP} * ⁴ | - | 2 t _{CYCP} * ⁴ | - | ns | |

*1 : R and C represent the pull-up resistor and load capacitance of the SCL and SDA lines, respectively. V_p indicates the supply voltage of the pull-up resistor and I_{OL} indicates V_{OL} guaranteed current.

*2 : The maximum t_{HDDAT} must satisfy that it does not extend at least "L" period (t_{LOW}) of device's SCL signal.

*3 : A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4 : t_{CYCP} is the APB bus clock cycle time. About the APB bus number which I²C is connected to, see "■BLOCK DIAGRAM" in this data sheet. To use I²C, set the APB bus clock at 8 MHz or more.

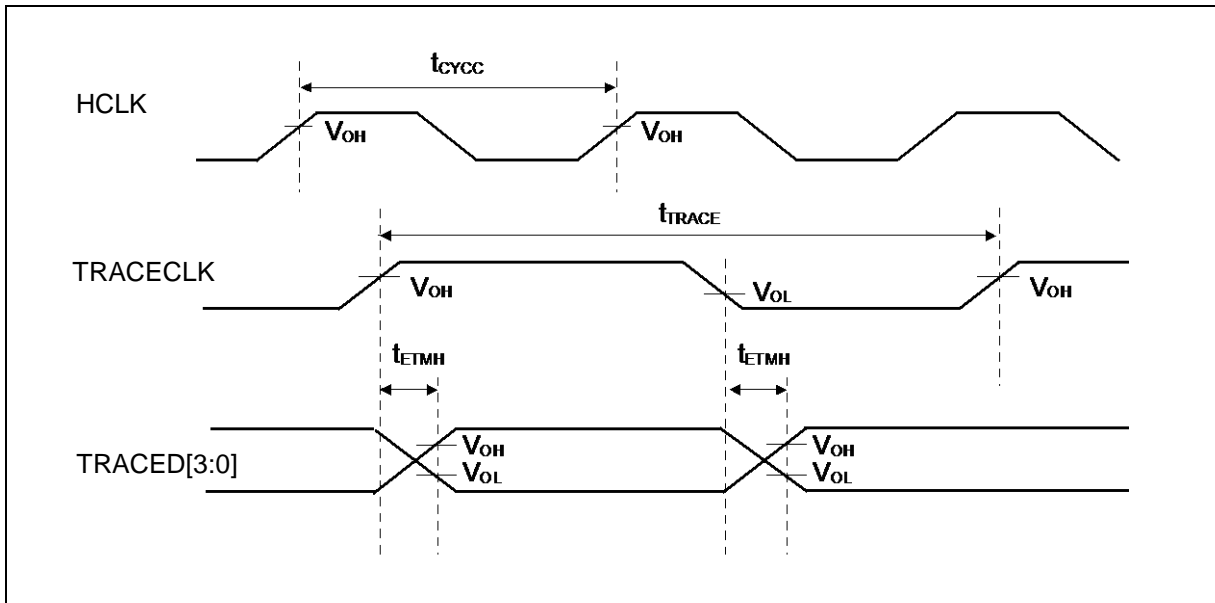


(13) ETM Timing

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$, $T_a = -40^{\circ}C$ to $+105^{\circ}C$)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---------------------------|---------------|--------------------------|--------------------|-------|-----|------|---------|
| | | | | Min | Max | | |
| Data hold | t_{ETMH} | TRACECLK, TRACED[3:0] | $V_{CC} \geq 4.5V$ | 2 | 9 | ns | |
| | | | $V_{CC} < 4.5V$ | 2 | 15 | | |
| TRACECLK frequency | $1/t_{TRACE}$ | TRACECLK | $V_{CC} \geq 4.5V$ | - | 40 | MHz | |
| | | | $V_{CC} < 4.5V$ | - | 32 | MHz | |
| TRACECLK Clock cycle time | t_{TRACE} | | $V_{CC} \geq 4.5V$ | 25 | - | ns | |
| | | | $V_{CC} < 4.5V$ | 31.25 | - | ns | |

Note: When the external load capacitance $C_L = 30pF$.

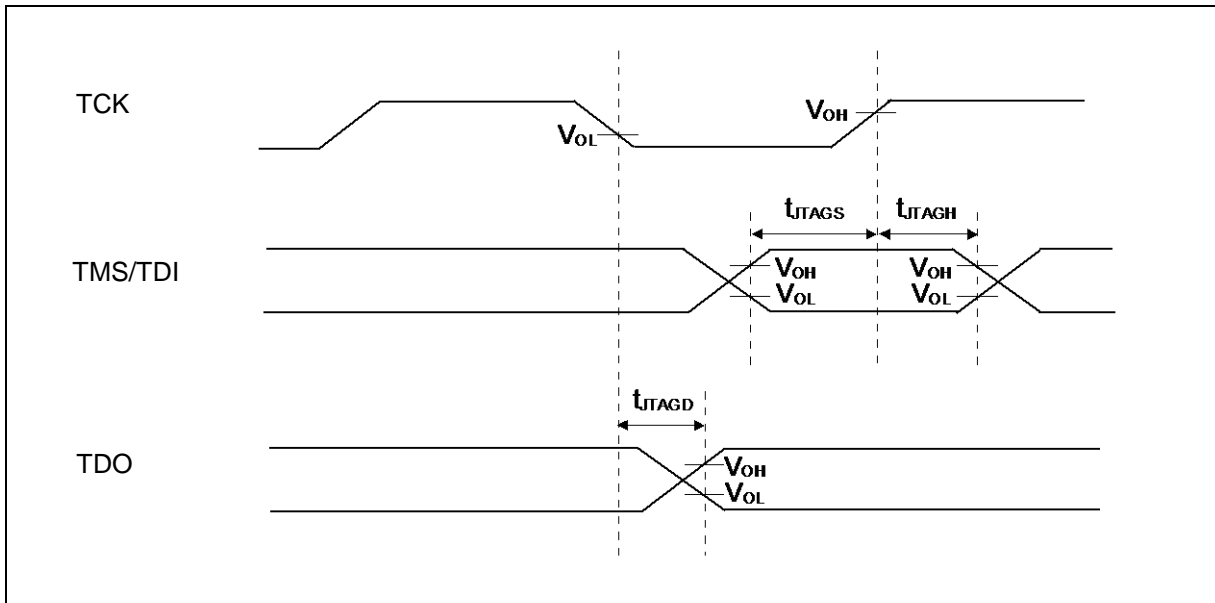


(14) JTAG Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_a = - 40°C to + 105°C)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---------------------|--------------------|---------------|------------------------|-------|-----|------|---------|
| | | | | Min | Max | | |
| TMS, TDI setup time | t _{JTAGS} | TCK, TMS, TDI | V _{CC} ≥ 4.5V | 15 | - | ns | |
| | | | V _{CC} < 4.5V | | | | |
| TMS, TDI hold time | t _{JTAGH} | TCK, TMS, TDI | V _{CC} ≥ 4.5V | 15 | - | ns | |
| | | | V _{CC} < 4.5V | | | | |
| TDO delay time | t _{JTAGD} | TCK, TDO | V _{CC} ≥ 4.5V | - | 25 | ns | |
| | | | V _{CC} < 4.5V | - | 45 | | |

Note: When the external load capacitance C_L = 30pF.



5. 12-bit A/D Converter

- Electrical characteristics for the A/D converter

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_a = -40^{\circ}C$ to $+105^{\circ}C$)

| Parameter | Pin name | Value | | | Unit | Remarks |
|---|-------------|-------------------|------|-----------|------|-------------------------------|
| | | Min | Typ | Max | | |
| Resolution | - | - | - | 12 | bit | |
| Non-linearity error | - | - 4.5 | - | + 4.5 | LSB | AVRH = 2.7V to 5.5V |
| Differential linearity error | - | - 2.5 | - | + 2.5 | LSB | |
| Zero transition voltage | AN0 to AN15 | - 20 | - | + 20 | mV | |
| Full-scale transition voltage | AN0 to AN15 | AVRH - 20 | - | AVRH + 20 | mV | |
| Conversion time | - | 1.0* ¹ | - | - | μs | AVCC ≥ 4.5V |
| Sampling time | Ts | *2 | - | - | ns | AVCC ≥ 4.5V |
| | | *2 | - | - | | AVCC < 4.5V |
| Compare clock cycle* ³ | Tcck | 50 | - | 2000 | ns | |
| State transition time to operation permission | Tstt | 1.0 | - | - | μs | |
| Power supply current (analog + digital) | AVCC | - | 0.57 | 0.72 | mA | A/D 1unit operation |
| | | - | 0.06 | 20 | μA | When A/D stops |
| Reference power supply current (between AVRH to AVSS) | AVRH | - | 1.1 | 1.96 | mA | A/D 1unit operation AVRH=5.5V |
| | | - | 0.06 | 4 | μA | When A/D stops |
| Analog input capacity | Cin | - | - | 12.9 | pF | |
| Analog input resistor | Rin | - | - | 2 | kΩ | AVCC ≥ 4.5V |
| | | | | 3.8 | | AVCC < 4.5V |
| Interchannel disparity | - | - | - | 4 | LSB | |
| Analog port input current | AN0 to AN15 | - | - | 5 | μA | |
| Analog input voltage | AN0 to AN15 | AVSS | - | AVRH | V | |
| Reference voltage | AVRH | 2.7 | - | AVCC | V | |

*1: The conversion time is the value of sampling time (Ts) + compare time (Tc).

The condition of the minimum conversion time is when the value of sampling time: 300ns, the value of compare time: 700ns (AVCC ≥ 4.5V)

Ensure that it satisfies the value of the sampling time (Ts) and compare clock cycle (Tcck).

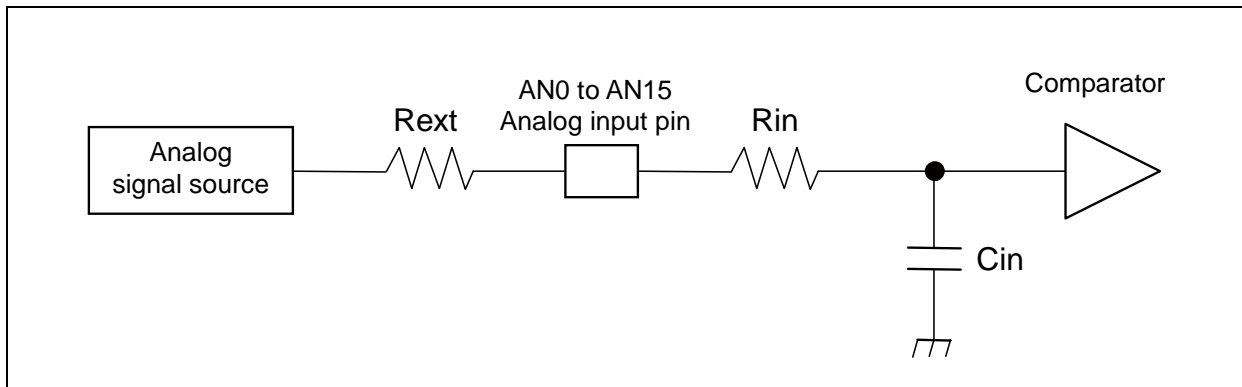
For setting of the sampling time and compare clock cycle, see "Chapter: A/D Converter" in "FM3 Family PERIPHERAL MANUAL Analog Macro Part".

The A/D Converter register is set at APB bus clock timing. The sampling clock and compare clock are set at Base clock (HCLK).

*2: A necessary sampling time changes by external impedance.

Ensure that it sets the sampling time to satisfy (Equation 1).

*3: The compare time (Tc) is the value of (Equation 2).



(Equation 1) $T_s \geq (R_{in} + R_{ext}) \times C_{in} \times 9$

T_s : Sampling time

R_{in} : input resistor of A/D = $2k\Omega$ $4.5 \leq AVCC \leq 5.5$

input resistor of A/D = $3.8k\Omega$ $2.7 \leq AVCC < 4.5$

C_{in} : input capacity of A/D = $12.9pF$ $2.7 \leq AVCC \leq 5.5$

R_{ext} : Output impedance of external circuit

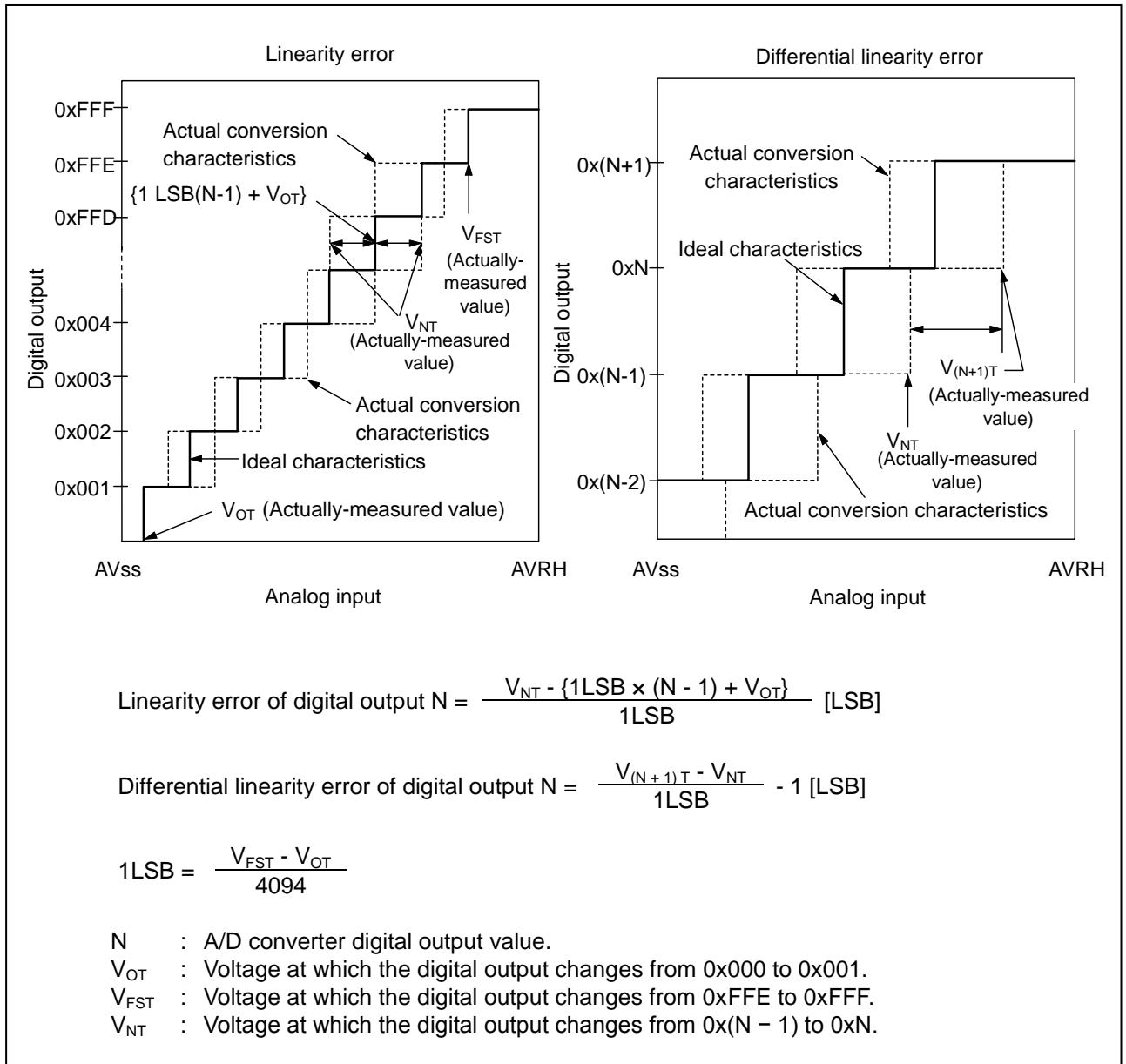
(Equation 2) $T_c = T_{cck} \times 14$

T_c : Compare time

T_{cck} : Compare clock cycle

• Definition of 12-bit A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linearity error : Deviation of the line between the zero-transition point (0b000000000000 ←→ 0b000000000001) and the full-scale transition point (0b111111111110 ←→ 0b111111111111) from the actual conversion characteristics.
- Differential linearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



6. Low-Voltage Detection Characteristics

(1) Low-Voltage Detection Reset

(Ta = - 40°C to + 105°C)

| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|------------------|--------|------------|-------|------|------|------|--------------------|
| | | | Min | Typ | Max | | |
| Detected voltage | VDL | - | 2.25 | 2.45 | 2.65 | V | When voltage drops |
| Released voltage | VDH | - | 2.30 | 2.50 | 2.70 | V | When voltage rises |

(2) Interrupt of Low-Voltage Detection

(Ta = - 40°C to + 105°C)

| Parameter | Symbol | Conditions | Value | | | Unit | Remarks |
|-----------------------------|-------------------|-------------|-------|-----|----------------------------|------|--------------------|
| | | | Min | Typ | Max | | |
| Detected voltage | VDL | SVHI = 0000 | 2.58 | 2.8 | 3.02 | V | When voltage drops |
| Released voltage | VDH | | 2.67 | 2.9 | 3.13 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 0001 | 2.76 | 3.0 | 3.24 | V | When voltage drops |
| Released voltage | VDH | | 2.85 | 3.1 | 3.34 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 0010 | 2.94 | 3.2 | 3.45 | V | When voltage drops |
| Released voltage | VDH | | 3.04 | 3.3 | 3.56 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 0011 | 3.31 | 3.6 | 3.88 | V | When voltage drops |
| Released voltage | VDH | | 3.40 | 3.7 | 3.99 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 0100 | 3.40 | 3.7 | 3.99 | V | When voltage drops |
| Released voltage | VDH | | 3.50 | 3.8 | 4.10 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 0111 | 3.68 | 4.0 | 4.32 | V | When voltage drops |
| Released voltage | VDH | | 3.77 | 4.1 | 4.42 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 1000 | 3.77 | 4.1 | 4.42 | V | When voltage drops |
| Released voltage | VDH | | 3.86 | 4.2 | 4.53 | V | When voltage rises |
| Detected voltage | VDL | SVHI = 1001 | 3.86 | 4.2 | 4.53 | V | When voltage drops |
| Released voltage | VDH | | 3.96 | 4.3 | 4.64 | V | When voltage rises |
| LVD stabilization wait time | T _{LVDW} | - | - | - | 2240 × t _{CYCP} * | μs | |

* : t_{CYCP} indicates the APB2 bus clock cycle time.

7. Flash Memory Write/Erase Characteristics

(V_{cc} = 2.7V to 5.5V, T_a = - 40°C to + 105°C)

| Parameter | | Value | | | Value | Remarks |
|-------------------------------|-------------------|-------|-----|------|-------|---|
| | | Min | Typ | Max | | |
| Sector erase time | Large Sector | - | 0.7 | 3.3 | s | Includes write time prior to internal erase |
| | Small Sector | | 0.3 | 1.1 | | |
| Half word (16-bit) write time | | - | 12 | 384 | μs | Not including system-level overhead time. |
| Chip erase time | 64K/128K/256KByte | - | 5.2 | 23.6 | s | Includes write time prior to internal erase |
| | 384K/512KByte | | 8 | 38.4 | s | |

Write cycles and data hold time

| Erase/write cycles (cycle) | Data hold time (year) | Remarks |
|----------------------------|-----------------------|---------|
| 1,000 | 20 * | |
| 10,000 | 10 * | |
| 100,000 | 5 * | |

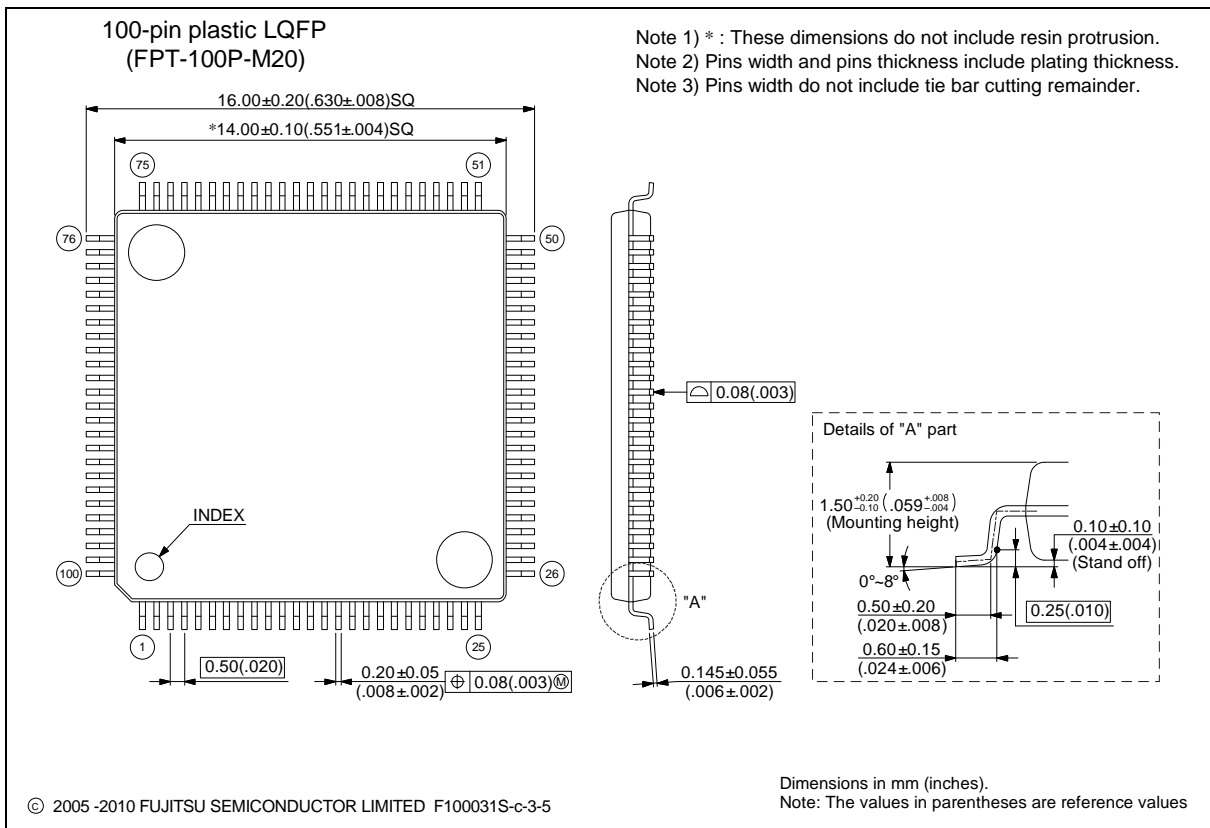
*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at + 85°C) .

■ ORDERING INFORMATION

| Part number | Package |
|----------------|--|
| MB9AF111LAPMC1 | Plastic • LQFP(0.5mm pitch), 64-pin (FPT-64P-M24/M38) |
| MB9AF112LAPMC1 | |
| MB9AF114LAPMC1 | |
| MB9AF111LAPMC | Plastic • LQFP(0.65mm pitch), 64-pin (FPT-64P-M23/M39) |
| MB9AF112LAPMC | |
| MB9AF114LAPMC | |
| MB9AF111LAQN | Plastic • QFN(0.5mm pitch), 64-pin (LCC-64P-M24) |
| MB9AF112LAQN | |
| MB9AF114LAQN | |
| MB9AF111MAPMC | Plastic • LQFP(0.5mm pitch), 80-pin (FPT-80P-M21/M37) |
| MB9AF112MAPMC | |
| MB9AF114MAPMC | |
| MB9AF115MAPMC | |
| MB9AF116MAPMC | |
| MB9AF111NAPMC | Plastic • LQFP(0.5mm pitch), 100-pin (FPT-100P-M20/M23) |
| MB9AF112NAPMC | |
| MB9AF114NAPMC | |
| MB9AF115NAPMC | |
| MB9AF116NAPMC | |
| MB9AF111NAPF | Plastic • QFP(0.65mm pitch), 100-pin (FPT-100P-M06) |
| MB9AF112NAPF | |
| MB9AF114NAPF | |
| MB9AF115NAPF | |
| MB9AF116NAPF | |
| MB9AF111NABGL | Plastic • PFPGA(0.8mm pitch), 112-pin (BGA-112P-M04) |
| MB9AF112NABGL | |
| MB9AF114NABGL | |

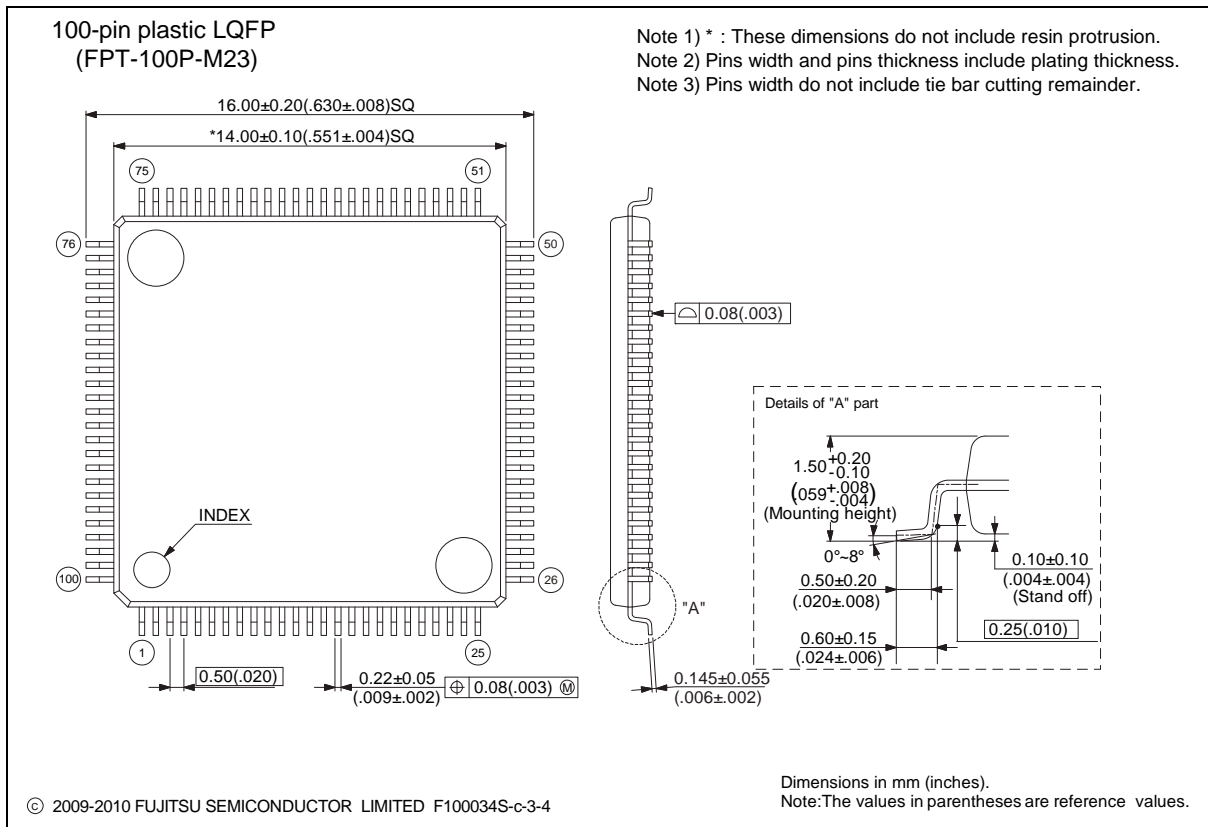
■ PACKAGE DIMENSIONS

| | | |
|---|--------------------------------|-----------------------|
| <p>100-pin plastic LQFP</p> <p>(FPT-100P-M20)</p> | Lead pitch | 0.50 mm |
| | Package width × package length | 14.0 mm × 14.0 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm Max |
| | Weight | 0.65 g |
| | Code (Reference) | P-LFQFP100-14x14-0.50 |



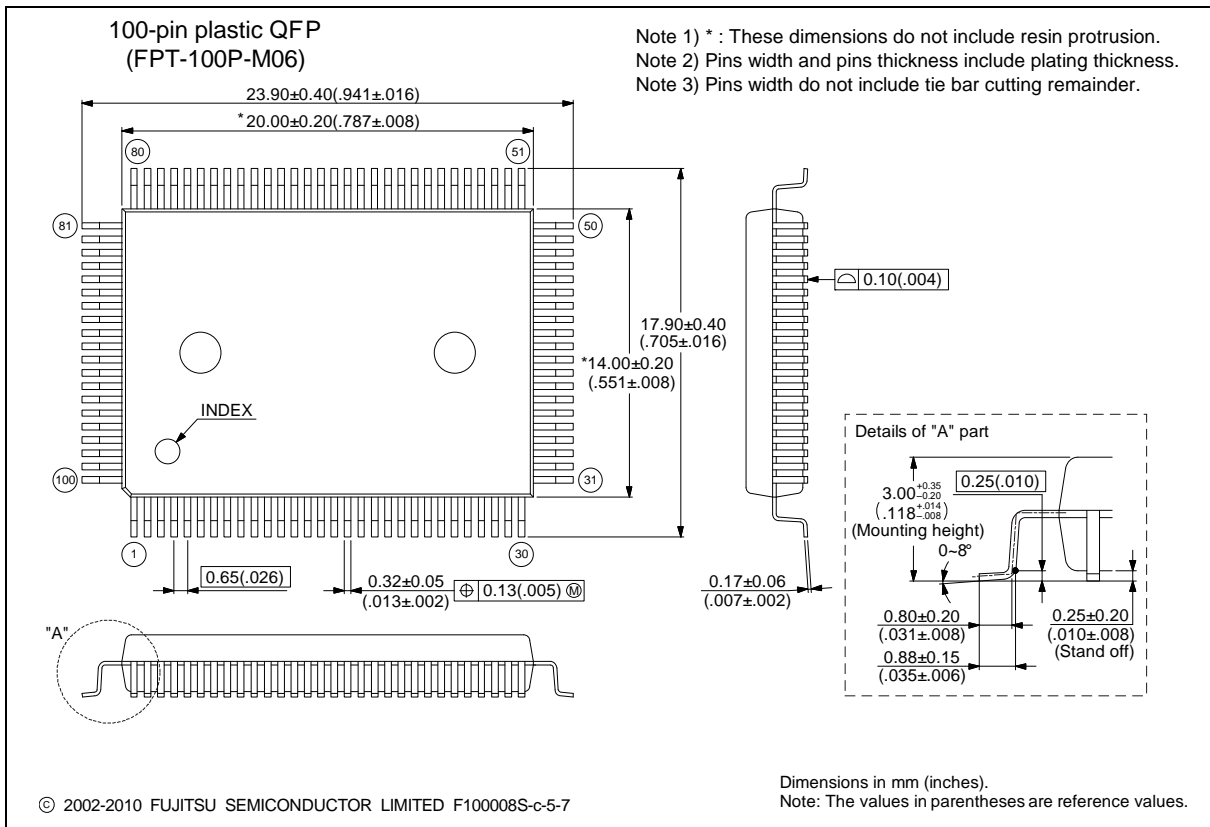
Please check the latest package dimension at the following URL.
<http://edevic.fujitsu.com/package/en-search/>

| | | |
|---|--------------------------------|---------------------|
| <p>100-pin plastic LQFP</p> <p>(FPT-100P-M23)</p> | Lead pitch | 0.50 mm |
| | Package width x package length | 14.00 mm x 14.00 mm |
| | Lead shape | Gullwing |
| | Lead bend direction | Normal bend |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.65 g |



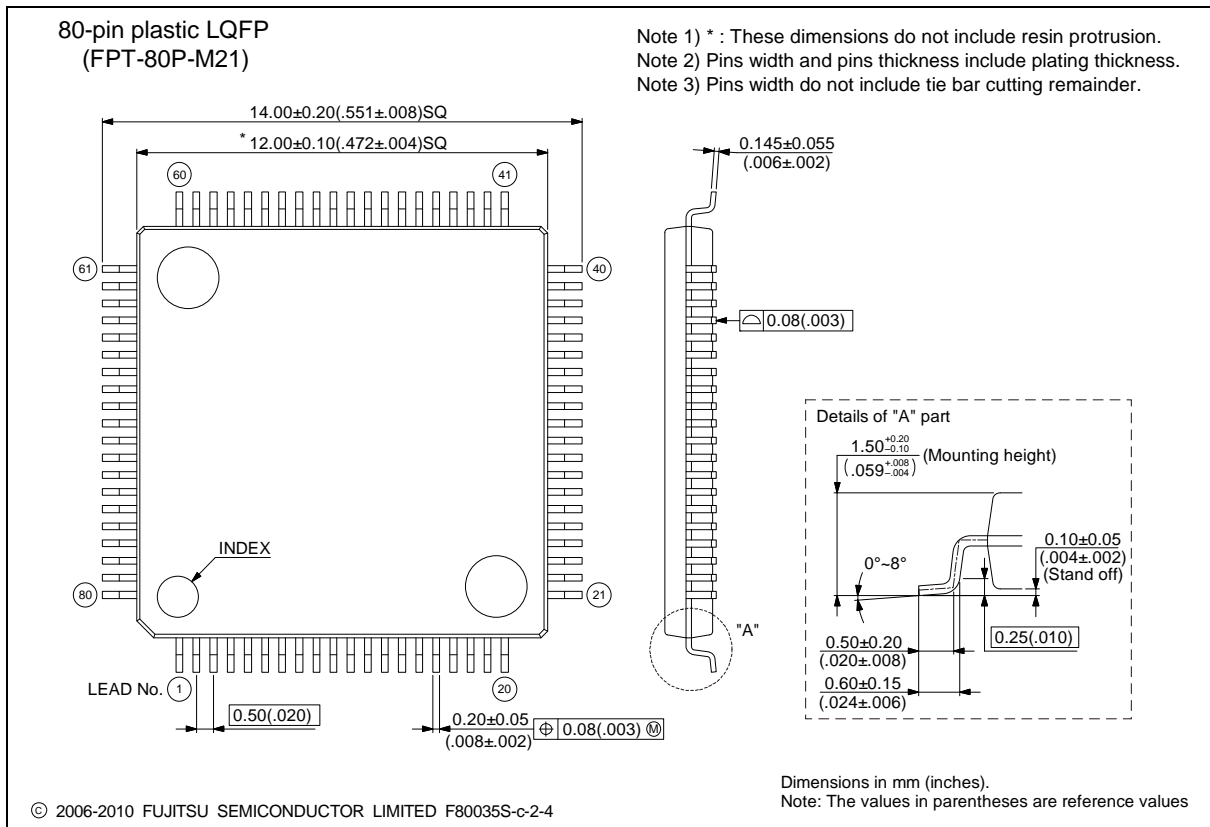
Please check the latest package dimension at the following URL.
<http://edevice.fujitsu.com/package/en-search/>

| | | |
|--|--------------------------------|---------------------|
| <p>100-pin plastic QFP</p> <p>(FPT-100P-M06)</p> | Lead pitch | 0.65 mm |
| | Package width x package length | 14.00 x 20.00 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 3.35 mm MAX |
| | Code (Reference) | P-QFP100-14x20-0.65 |
| | | |



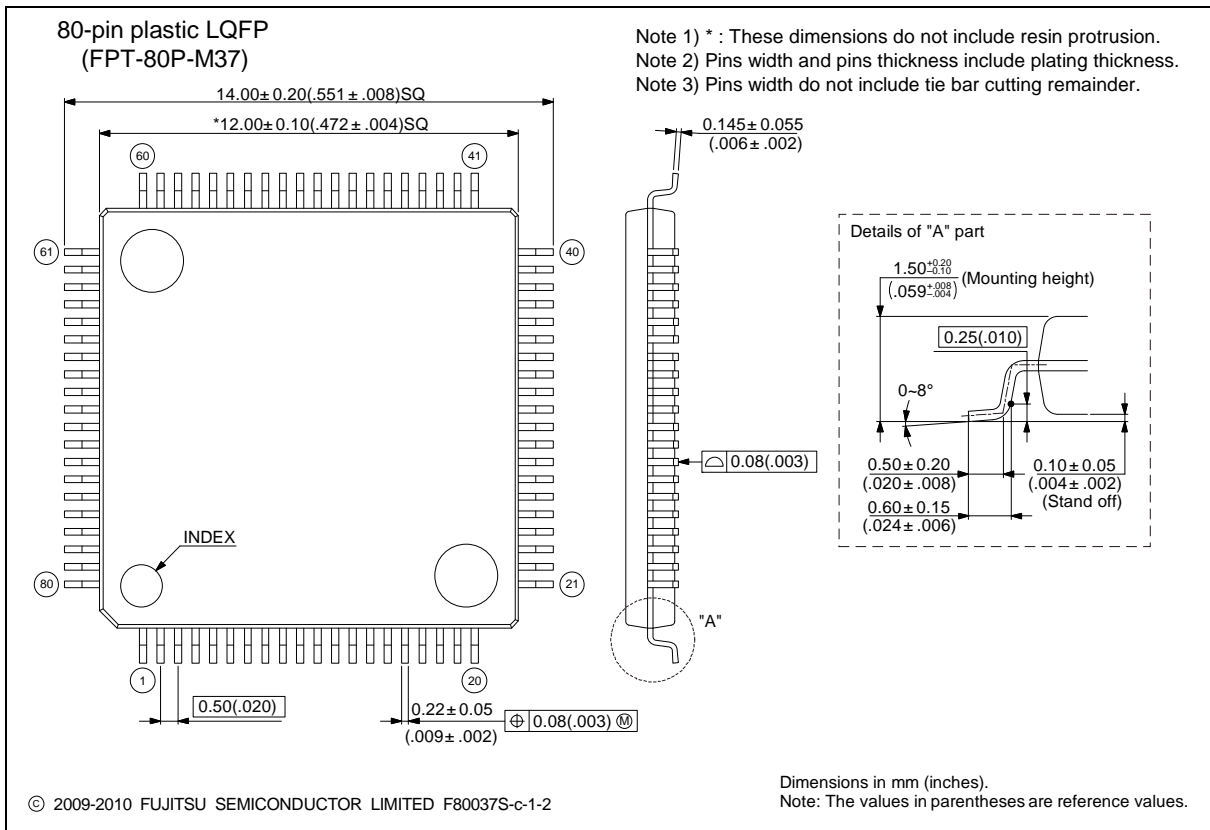
Please check the latest package dimension at the following URL.
<http://edevic.fujitsu.com/package/en-search/>

| | | |
|---|--------------------------------|----------------------|
| <p>80-pin plastic LQFP</p> <p>(FPT-80P-M21)</p> | Lead pitch | 0.50 mm |
| | Package width x package length | 12 mm x 12 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm Max |
| | Weight | 0.47 g |
| | Code (Reference) | P-LFQFP80-12x12-0.50 |



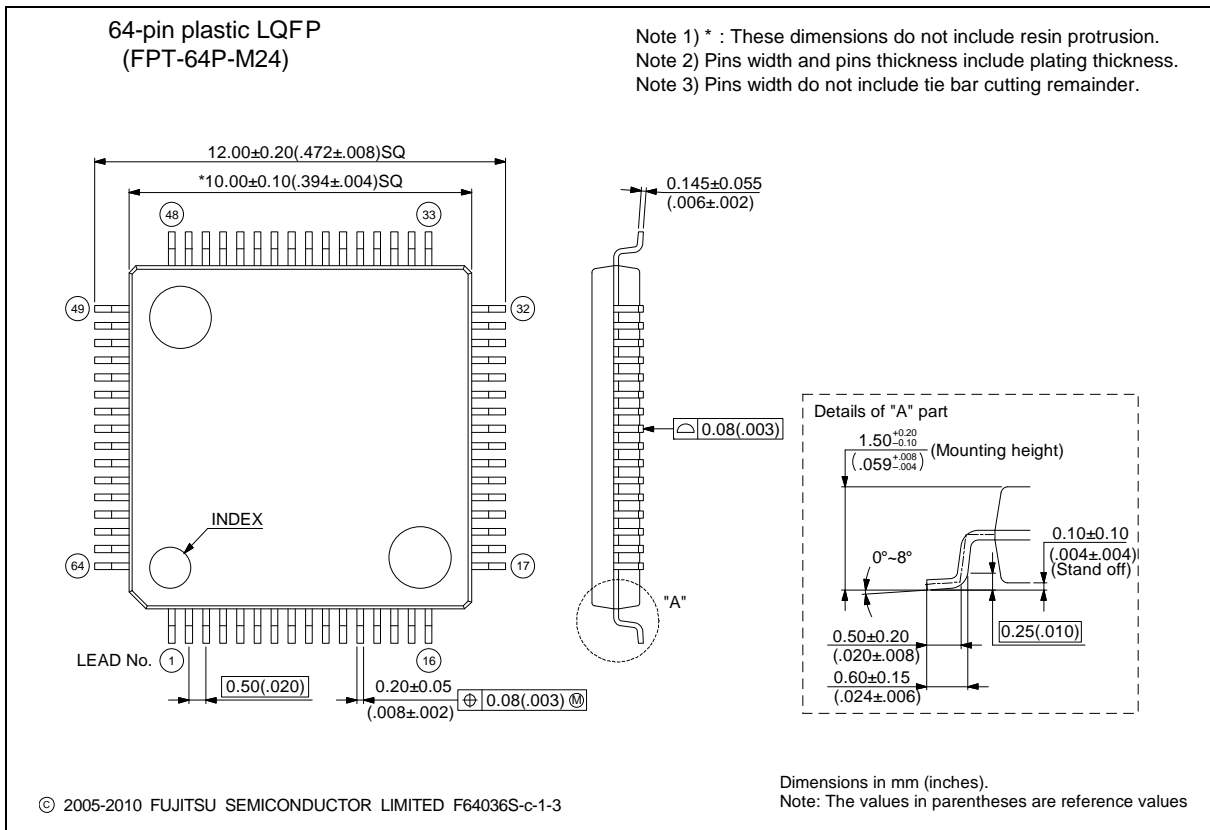
Please check the latest package dimension at the following URL.
<http://edevice.fujitsu.com/package/en-search/>

| | | |
|---|--------------------------------|---------------------|
| <p>80-pin plastic LQFP</p> <p>(FPT-80P-M37)</p> | Lead pitch | 0.50 mm |
| | Package width x package length | 12.00 mm x 12.00 mm |
| | Lead shape | Gullwing |
| | Lead bend direction | Normal bend |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.47 g |



Please check the latest package dimension at the following URL.
<http://edevice.fujitsu.com/package/en-search/>

| | | |
|---|--------------------------------|----------------------|
| <p>64-pin plastic LQFP</p> <p>(FPT-64P-M24)</p> | Lead pitch | 0.50 mm |
| | Package width x package length | 10.0 x 10.0 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.32 g |
| | Code (Reference) | P-LFQFP64-10x10-0.50 |



Please check the latest package dimension at the following URL.
<http://edevice.fujitsu.com/package/en-search/>

| | | |
|---|--------------------------------|---------------------|
| <p>64-pin plastic LQFP</p> <p>(FPT-64P-M38)</p> | Lead pitch | 0.50 mm |
| | Package width x package length | 10.00 mm x 10.00 mm |
| | Lead shape | Gullwing |
| | Lead bend direction | Normal bend |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.32 g |

64-pin plastic LQFP (FPT-64P-M38)

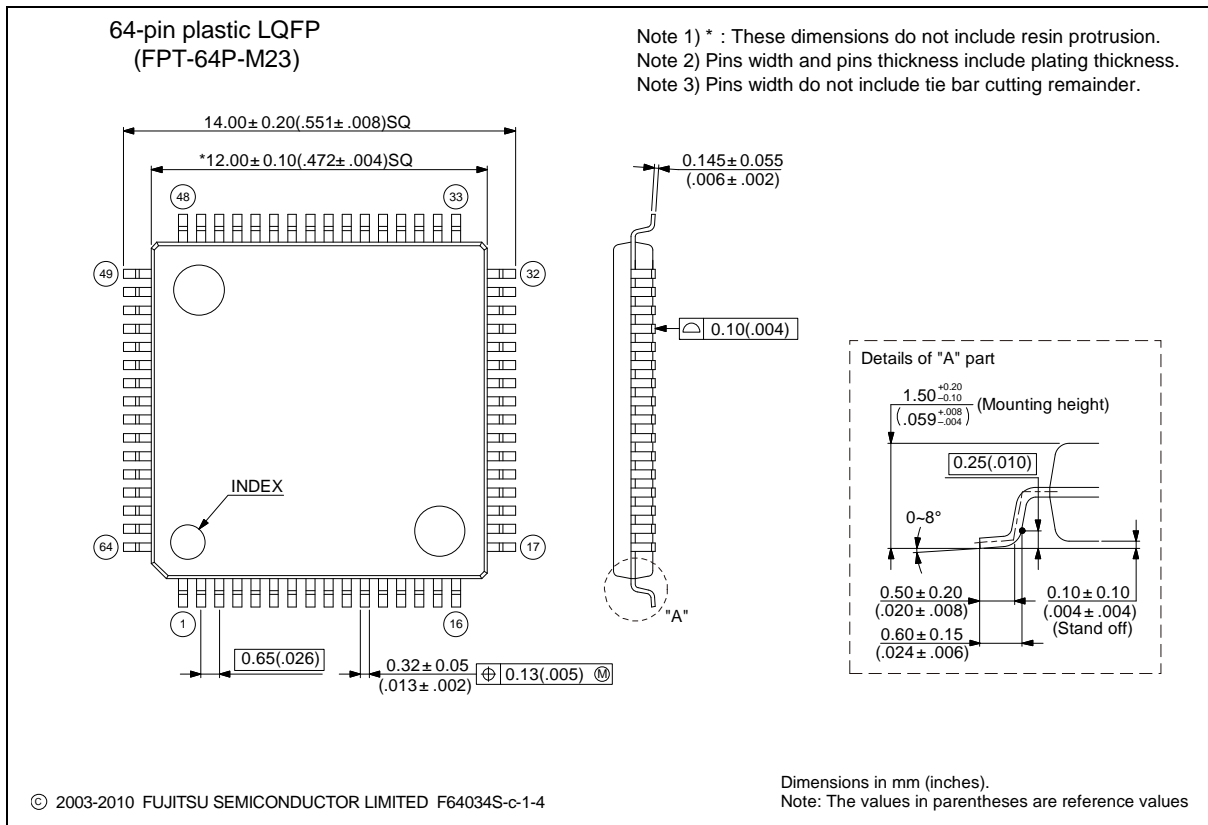
Note 1) * : These dimensions do not include resin protrusion.
 Note 2) Pins width and pins thickness include plating thickness.
 Note 3) Pins width do not include tie bar cutting remainder.

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Dimensions in mm (inches).
 Note: The values in parentheses are reference values.

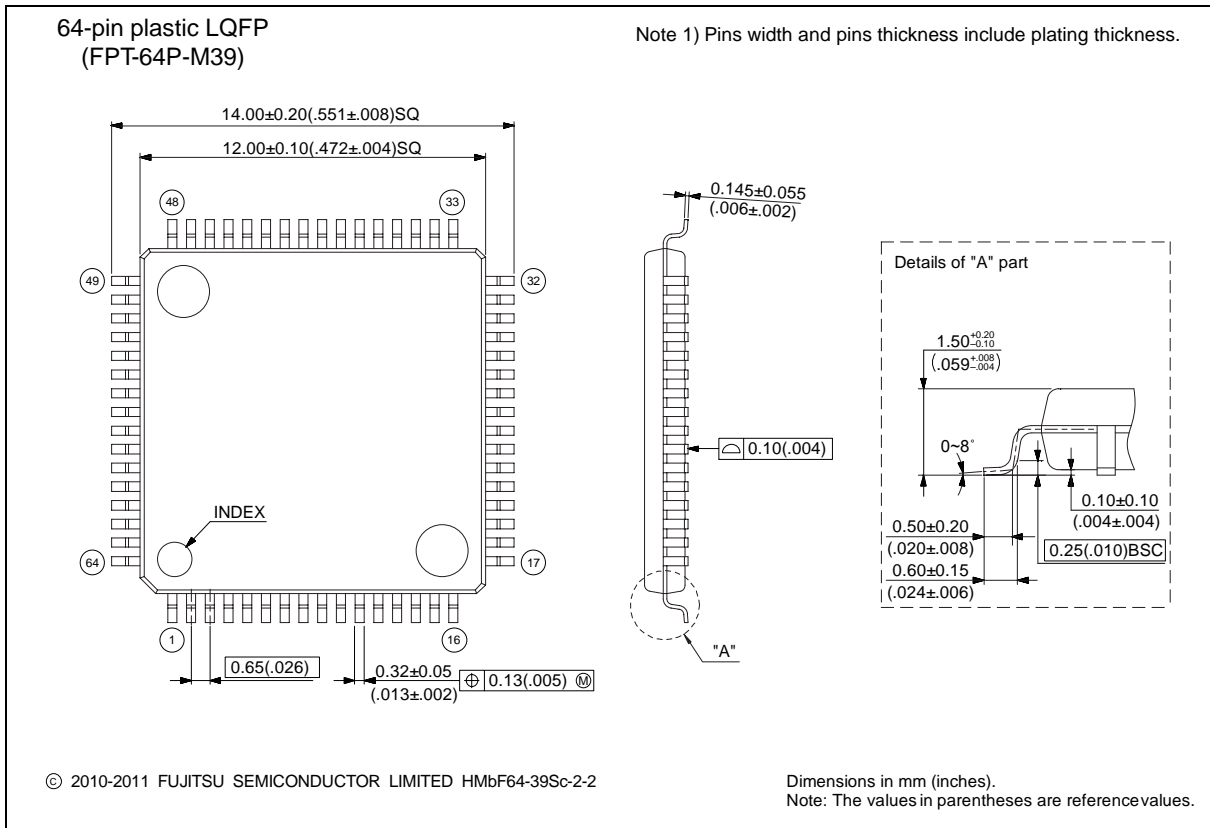
Please check the latest package dimension at the following URL.
<http://edevice.fujitsu.com/package/en-search/>

| | | |
|---|--------------------------------|-----------------------|
| <p>64-pin plastic LQFP</p> <p>(FPT-64P-M23)</p> | Lead pitch | 0.65 mm |
| | Package width × package length | 12.0 × 12.0 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.47 g |
| | Code (Reference) | P-LQFP64-12 × 12-0.65 |

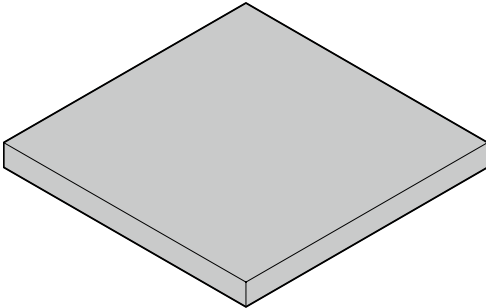


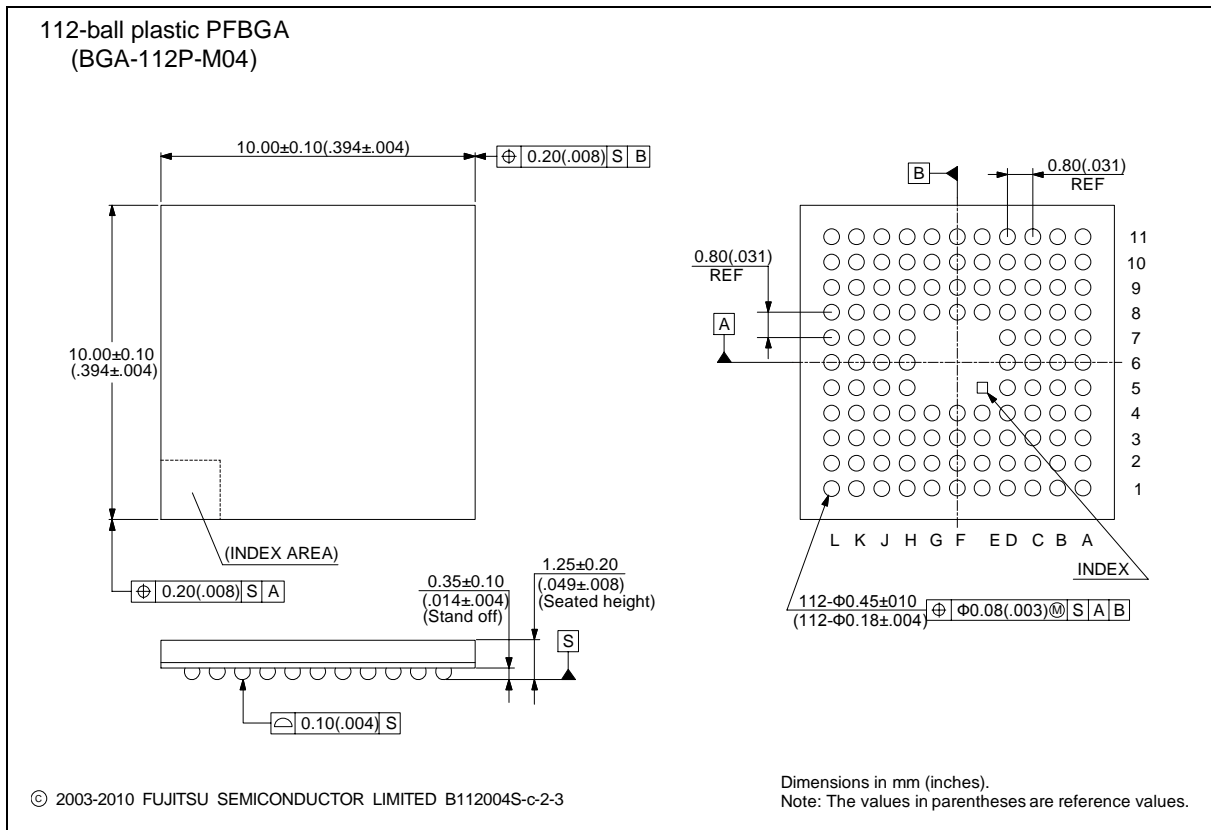
Please check the latest package dimension at the following URL.
<http://edevice.fujitsu.com/package/en-search/>

| | | |
|---|--------------------------------|---------------------|
| <p>64-pin plastic LQFP</p> <p>(FPT-64P-M39)</p> | Lead pitch | 0.65 mm |
| | Package width x package length | 12.00 mm x 12.00 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.47 g |
| | | |

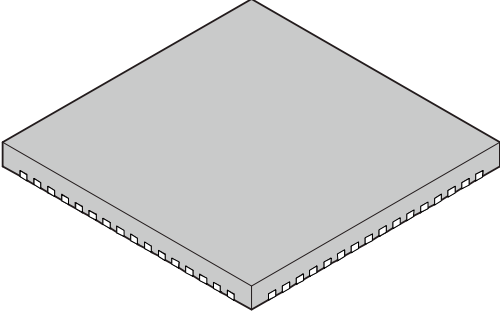


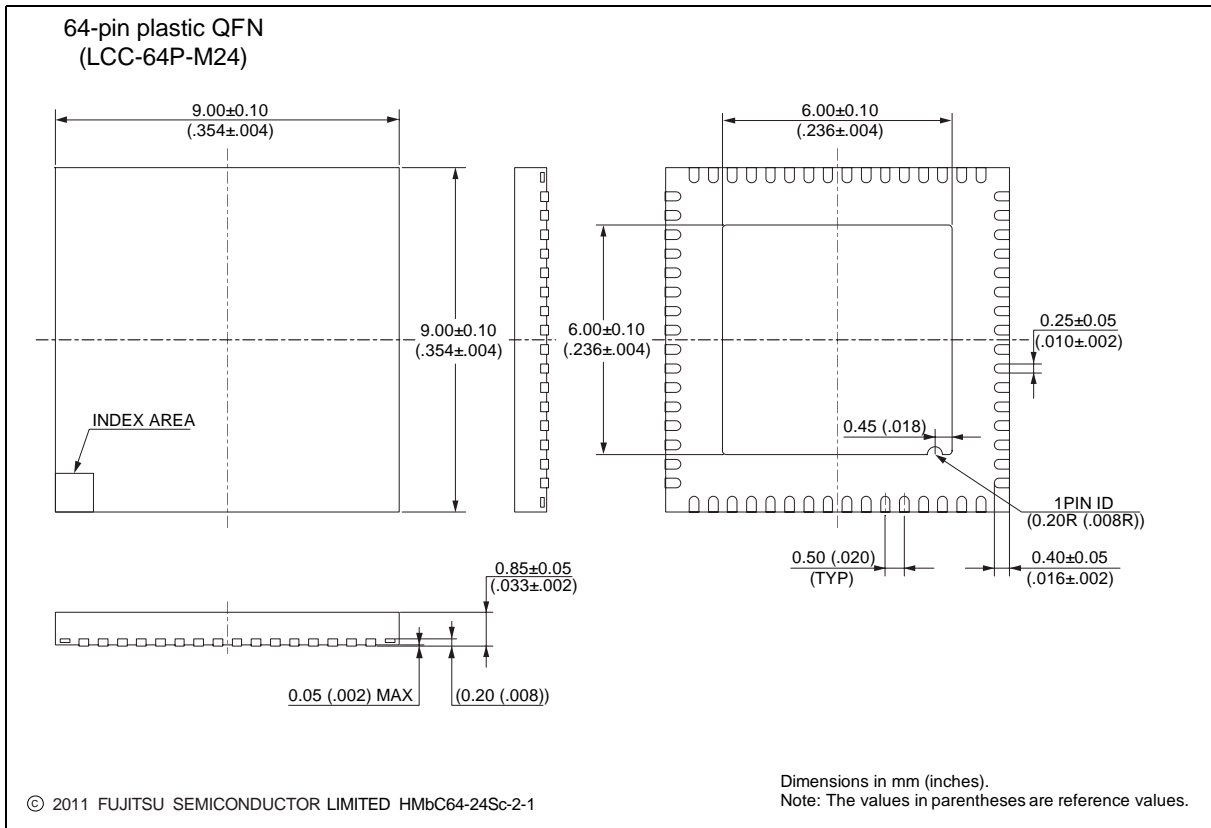
Please check the latest package dimension at the following URL.
<http://edevice.fujitsu.com/package/en-search/>

| | | |
|---|--------------------------------|------------------|
| <p>112-ball plastic PFBGA</p>  <p>(BGA-112P-M04)</p> | Ball pitch | 0.80 mm |
| | Package width × package length | 10.00 × 10.00 mm |
| | Lead shape | Soldering ball |
| | Sealing method | Plastic mold |
| | Ball size | Φ 0.45 mm |
| | Mounting height | 1.45 mm Max. |
| | Weight | 0.22 g |



Please check the latest package dimension at the following URL.
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| | | |
|--|--------------------------------|-------------------|
| <p>64-pin plastic QFN</p>  <p>(LCC-64P-M24)</p> | Lead pitch | 0.50 mm |
| | Package width x package length | 9.00 mm x 9.00 mm |
| | Sealing method | Plastic mold |
| | Mounting height | 0.90 mm MAX |
| | Weight | - |
| | | |



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■ MAJOR CHANGES

| Page | Section | Change Results |
|--------------|---|---|
| Revision 1.0 | | |
| - | - | Initial release |
| Revision 2.0 | | |
| - | - | <ul style="list-style-type: none"> Revised series name and part number: MB9A110 Series → MB9A110A Series MB9AF111L → MB9AF111LA MB9AF112L → MB9AF112LA MB9AF114L → MB9AF114LA MB9AF111M → MB9AF111MA MB9AF112M → MB9AF112MA MB9AF114M → MB9AF114MA MB9AF115M → MB9AF115MA MB9AF116M → MB9AF116MA MB9AF111N → MB9AF111NA MB9AF112N → MB9AF112NA MB9AF114N → MB9AF114NA MB9AF115N → MB9AF115NA MB9AF116N → MB9AF116NA Added the package. LCC-64P-M24 |
| 8 | ■ PRODUCT LINEUP <ul style="list-style-type: none"> Function Multi-function Serial Interface (UART/CSIO/LIN/I²C) External Interrupts | Added the following description. ch.4 to ch.7: FIFO (16steps × 9-bit) ch.0 to ch.3: No FIFO |
| 34 to 37 | ■ SIGNAL DESCRIPTION Multi-function Serial (ch.0 to ch.7) | Corrected the following description. 7pins (Max) → 8pins (Max) <ul style="list-style-type: none"> Added "LIN pin" Deleted "UART pin" |
| 42, 43 | ■ I/O CIRCUIT TYPE | <ul style="list-style-type: none"> Corrected the following schematic for "TypeB". CMOS level hysteresis input → Digital input Corrected the following schematic for "TypeC". Control Pin → Digital output |
| 51 | ■ HANDLING DEVICES <ul style="list-style-type: none"> Power supply pins | Corrected the description. |
| 54 | ■ MEMORY SIZE | Added " ■ MEMORY SIZE ". |
| 69 | ■ ELECTRICAL CHARACTERISTICS 4. AC Characteristics (1) Main Clock Input Characteristics | Added the items F _{CM} to the Internal operating clock frequency. |
| 71 | (4-2) Operating Conditions of Main PLL | Added the description. |
| 72 | (7) External Bus Timing <ul style="list-style-type: none"> External bus clock output Characteristics | |
| 79 | (8) Base Timer Input Timing <ul style="list-style-type: none"> Trigger input timing | Added the Note. |
| 88 | (10) External input timing | Corrected the footnote. |
| 94 | 6. 12-bit A/D Converter <ul style="list-style-type: none"> Electrical characteristics for the A/D converter | <ul style="list-style-type: none"> Corrected the value of "Full-scale transition voltage". Min: -20 → AVRH-20 Max: +20 → AVRH+20 Corrected the value of "Compare clock cycle". Max: 10000 → 2000 Corrected the value of "Reference voltage". Min: AVSS → 2.7 |
| Revision 2.1 | | |
| - | - | Company name and layout design change |

Colophon

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