

54F194 Shift Register

4-Bit Bidirectional Universal Shift Register

Military FAST Products

Product Specification

FEATURES

- Shift left and shift right capability
- Synchronous parallel and serial data transfers
- Easily expanded for both serial and parallel operation
- Asynchronous Master Reset
- Hold (do nothing) mode

DESCRIPTION

The functional characteristics of the 54F194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 9ns (typical), making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

ORDERING INFORMATION

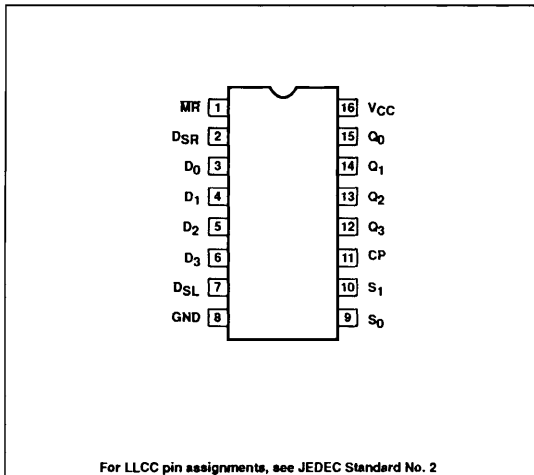
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54F194/BEA
16-Pin Ceramic FlatPack	54F194/BFA
20-Pin Ceramic LLCC	54F194/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

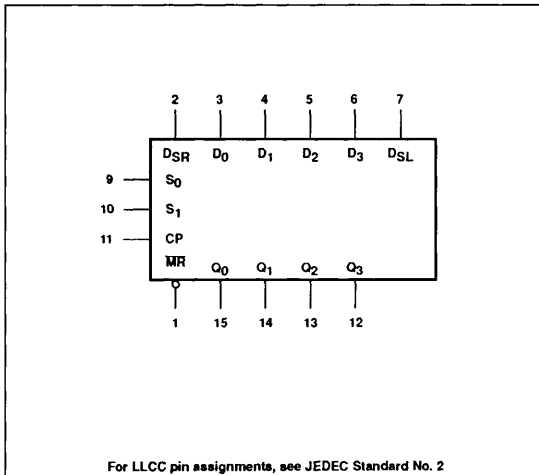
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D ₀ - D ₃	Parallel data inputs	1.0/1.0	20μA/0.6mA
S ₀ , S ₁	Mode control inputs	1.0/1.0	20μA/0.6mA
D _{SR}	Serial data input (shift right)	1.0/1.0	20μA/0.6mA
D _{SL}	Serial data input (shift left)	1.0/1.0	20μA/0.6mA
C _P	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
M _R	Asynchronous master reset (active Low)	1.0/1.0	20μA/0.6mA
Q ₀ - Q ₃	Parallel outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



LOGIC SYMBOL



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The 54F194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S_0 and S_1 . As shown in the Mode Select Table, data can be entered and shifted from left to right (shift right $Q_0 \rightarrow Q_1$, etc.), or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are Low, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data in-

puts (D_{SR} , D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

Mode Select and Data inputs on the 54F194 are edge-triggered, responding only to the Low-to-High transition of the Clock (CP). Therefore, the only timing restriction is that the Mode Control and selected Data inputs must be stable one setup time prior to the positive transition of the clock pulse. Signals on the Select, Parallel Data ($D_0 - D_3$) and Serial Data (D_{SR} , D_{SL}) inputs can change when the clock is in ei-

ther state, provided only the recommended setup and hold times, with respect to the clock rising edge, are observed.

The four Parallel Data inputs ($D_0 - D_3$) are D-type inputs. Data appearing on $D_0 - D_3$ inputs when S_0 and S_1 are High is transferred to the $Q_0 - Q_3$ outputs respectively, following the next Low-to-High transition of the clock. When Low, the asynchronous Master Reset (\overline{MR}) overrides all other input conditions and forces the Q outputs Low.

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	CP	\overline{MR}	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift left	\uparrow	H	h	l	X	l	X	q_1	q_2	q_3	L
	\uparrow	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift right	\uparrow	H	l	h	l	X	X	L	q_0	q_1	q_2
	\uparrow	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel load	\uparrow	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3

H = High voltage level

h = High voltage level one setup time prior to the Low-to-High clock transition

L = Low voltage level

l = Low voltage level one setup time prior to the Low-to-High clock transition

$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the Low-to-High clock transition

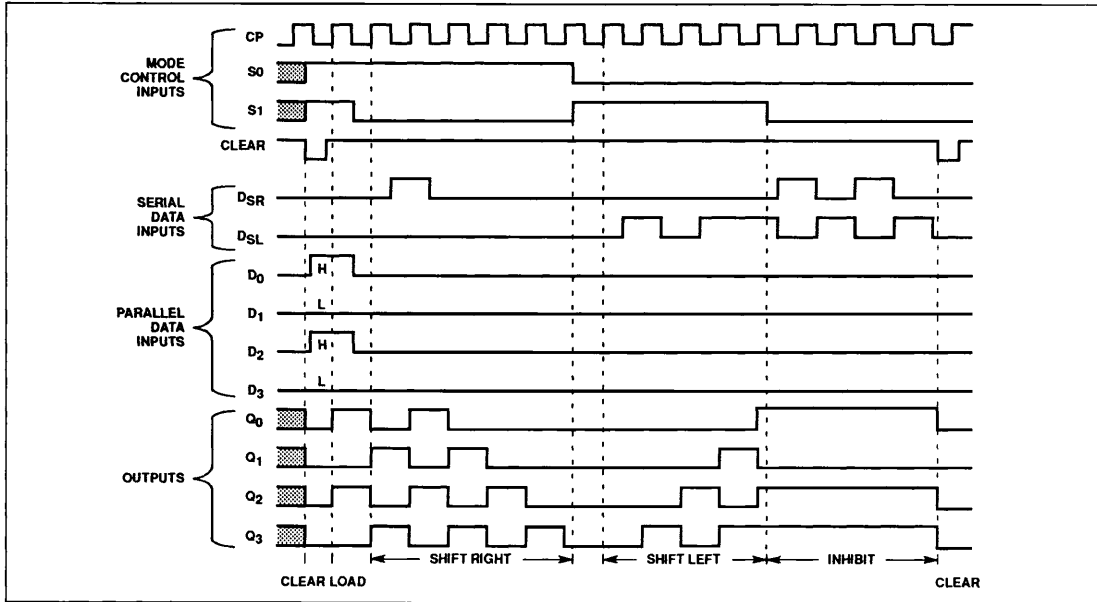
X = Don't care

\uparrow = Low-to-High clock transition

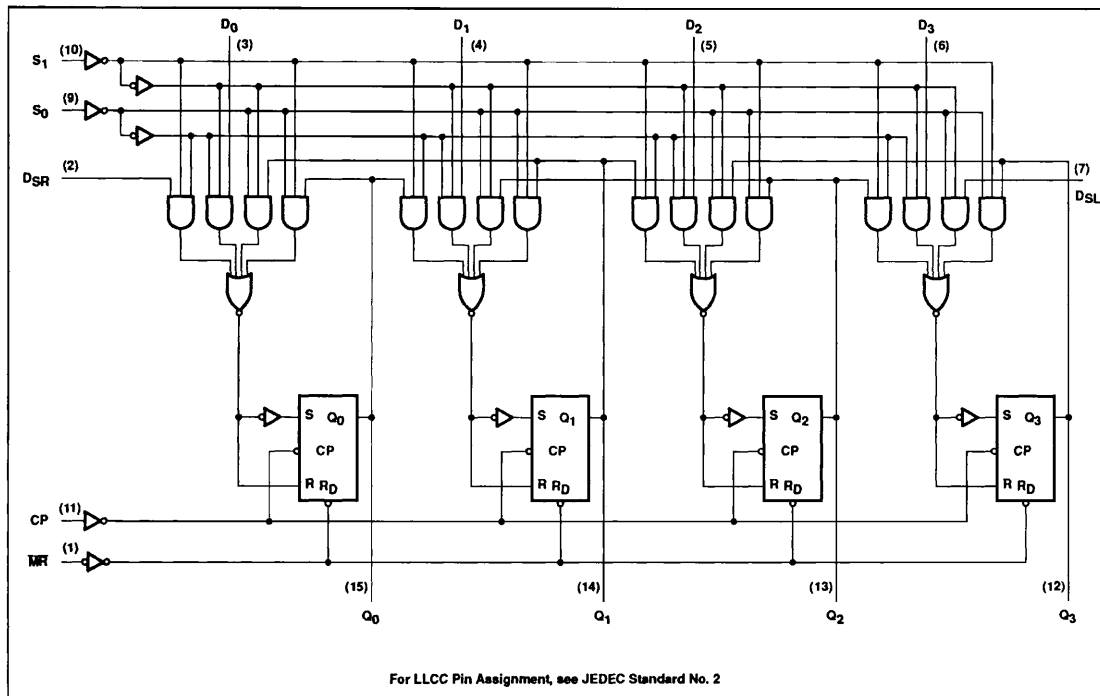
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TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT AND CLEAR SEQUENCES



LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage range	-0.5 to +7.0	V
V _I	Input voltage range	-0.5 to +7.0	V
I _I	Input current range	-30 to +5.0	mA
V _O	Voltage applied to output in High output state range	-0.5 to +V _{CC}	V
I _O	Current applied to output in Low output state	40	mA
T _{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-1	mA
I _{OL}	Low-level output current			20	mA
T _A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT
			Min	Typ ²	Max	
V _{OH}	High-level output voltage ³	V _{CC} = Min, V _{IH} = Min, V _{IL} = Max, I _{OH} = Max	2.5			V
V _{OL}	Low-level output voltage	V _{CC} = Min, V _{IH} = Min, V _{IL} = Max, I _{OL} = Max		0.35	0.50	V
V _{IK}	Input clamp voltage	V _{CC} = Min, I _I = I _{IK}		-0.73	-1.2	V
I _{IH2}	Input current at maximum input voltage	V _{CC} = Max, V _I = +7.0V		5	100	μA
I _{IH1}	High-level input current	V _{CC} = Max, V _I = 2.7V		1	20	μA
I _{IL}	Low-level input current	V _{CC} = Max, V _I = 0.5V		-0.4	-0.6	mA
I _{OS}	Short-circuit output current ⁴	V _{CC} = Max, V _O = 0.0V	-60	-90	-150	mA
I _{CC}	Supply current ⁵ (total)	V _{CC} = Max		33	46	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T _A = +25°C			T _A = -55°C to +125°C			
			Min	Typ	Max	Min	Max		
f _{MAX}	Maximum clock frequency	Waveform 1	105	150		90 ⁶		MHz	
t _{PLH}	Propagation delay CP to Q _n	Waveform 1	3.5	5.2	7.0	3.0	8.5	ns	
t _{PHL}			3.5	5.5	7.0	3.0	8.5	ns	
t _{PHL}	Propagation delay M ₁ to Q _n	Waveform 2	4.5	8.6	12	4.5	14.5	ns	

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AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}, R_L = 500\Omega$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}, R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, $D_0 - D_3$ to CP D_{SR}, D_{SL} to CP	Waveform 3	4.0			4.0		ns
			4.0			4.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low $D_0 - D_3$ to CP, D_{SR}, D_{SL} to CP	Waveform 3	0			1.0		ns
			0			1.0		ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low S_n to CP	Waveform 4	8.0			9.5		ns
			8.0			8.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low S_n to CP	Waveform 4	0			0		ns
			0			0		ns
t_{rec}	Recovery time, \overline{MR} to CP	Waveform 2	7.0			9.0		ns
$t_w(\text{H})$	CP pulse width, High	Waveform 1	5.0			5.5		ns
$t_w(\text{L})$	\overline{MR} pulse width, Low	Waveform 2	5.0			5.0		ns

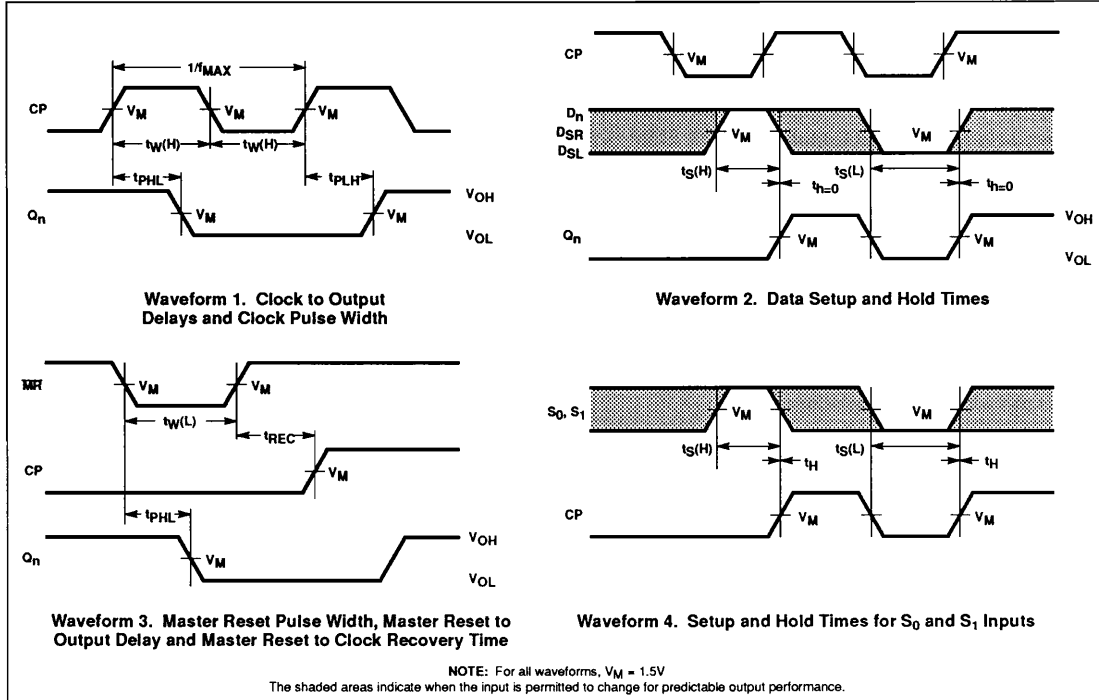
NOTES:

- For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- Output High state will change to Low state if an external voltage of less than 0.0V is applied.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- With all outputs open, D inputs grounded and $\geq 4.0\text{V}$ applied to S_0, S_1, \overline{MR} and the serial inputs, I_{CC} is tested with a momentary ground, then $\geq 4.0\text{V}$ applied to CP.
- These parameters are guaranteed, but not tested.

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AC WAVEFORMS



TEST CIRCUIT AND WAVEFORM

