

TC9809P, TC9809FW

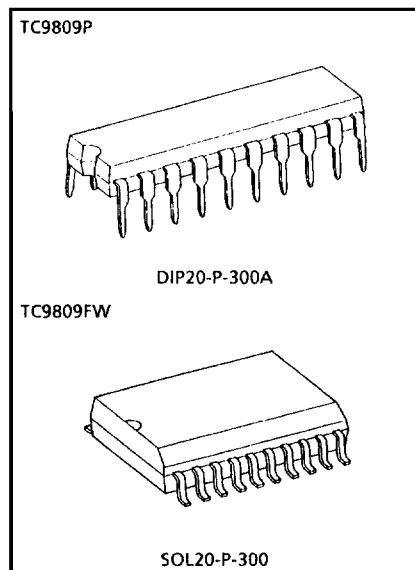
TENTATIVE DATA

TC9809 is a 20-pin CMOS programmable logic device (PLD) based on EEPROM cells. It has a zero-standby function. Designed using Toshiba's original technology, this device features low power dissipation and inputs that are compatible with TTL, NMOS, and CMOS output voltage levels. This device is applicable to a variety of electronic devices.

It has both AND and OR arrays which the user can program, like a field programmable logic array (FPLA).

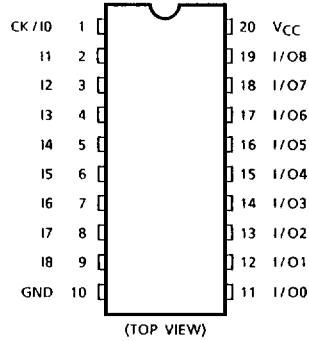
FEATURES

- Architecture 42 AND terms
9 OR terms
8 macro cells with registers
- Security cell Protection of proprietary information
- Signature word 42 bits for user ID code or inventory control
- Register initial state setting Can select initial states of registers at power-up.
Can set any input pin to sync set/reset.
- High speed operation t_{pd} (input-output) = 19ns (Typ.)
 t_{co} (clock-output) = 9ns (Typ.)
- Low power dissipation I_{CC} (standby) = 4 μ A (max. @25°C)
- Wide operating voltage range ... V_{CC} = 5V \pm 0.25V
- Package 20-pin plastic DIP (TC9809P)
20-pin plastic SOL (TC9809FW)



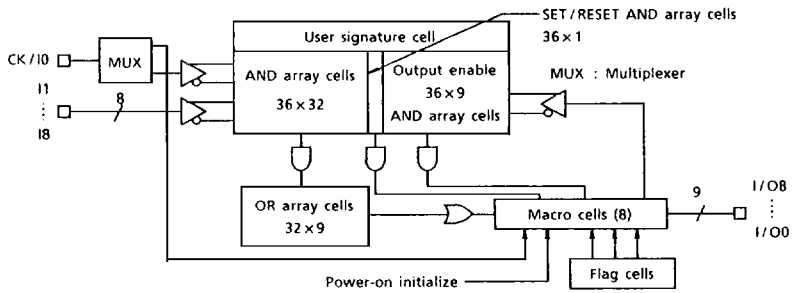
Weight DIP20-P-300A : 1.30g (Typ.)
SOL20-P-300 : 0.46g (Typ.)

PIN NAMES & FUNCTIONS



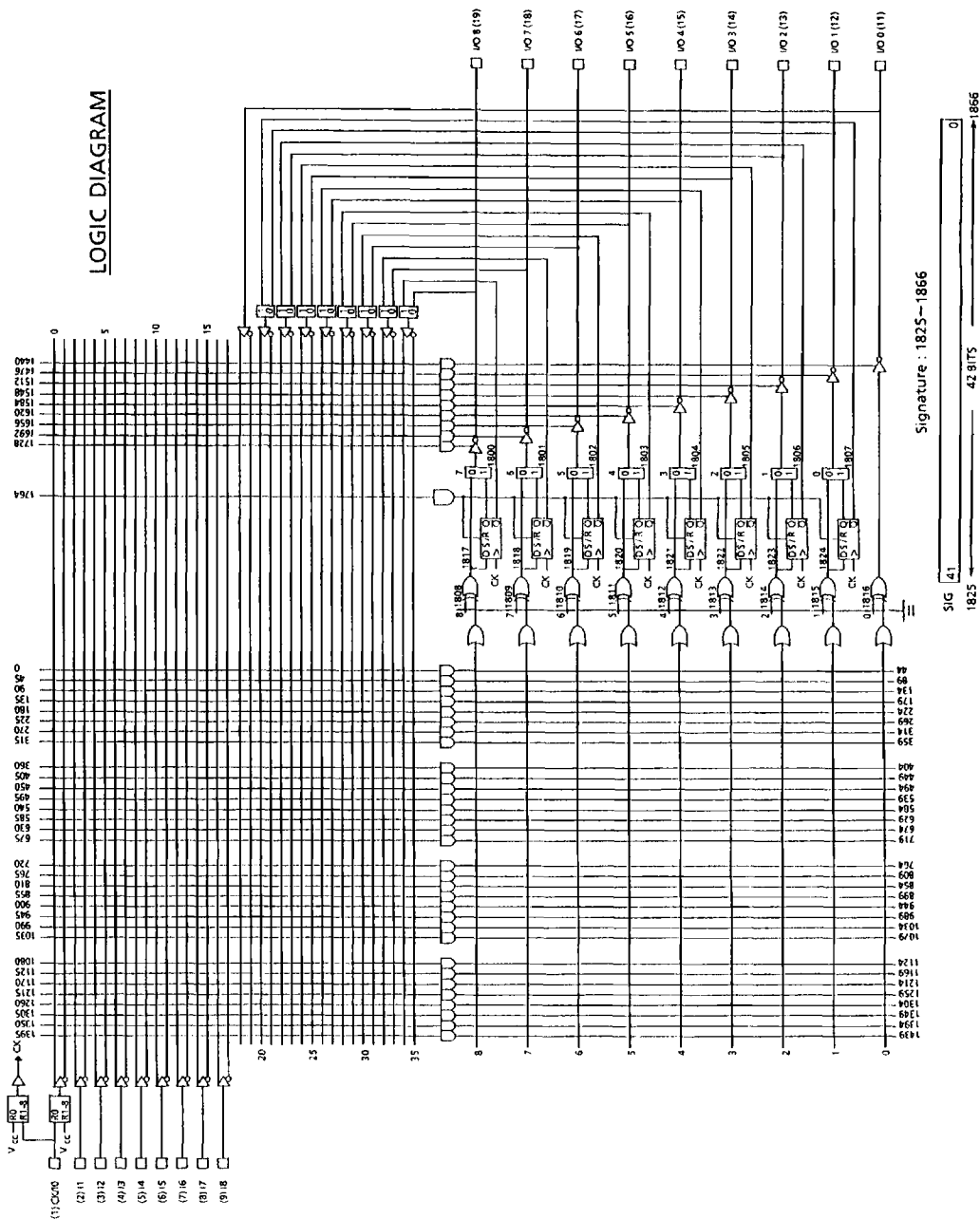
- CK / I/O Clock input (when register is selected)
- I1~I8 Dedicated to input
- I/O0 Input/Output (without register output)
- I/O1~I/O8 Input/Output (with register output)

FUNCTION DIAGRAM



TC9809P, TC9809FW

LOGIC DIAGRAM



ARCHITECTURE

1. MEMORY CELLS

Programmable memory cells are divided into the following six types : AND array, OR array, output control array, set/reset control array, flag, and user signature.

Setting program data to 1 disconnects signals to an AND/OR array : setting to 0 connects. In all erase mode, all bits are set to 1.

(1) AND array (36×32)

Total of 42 product terms (32 AND terms, 9 output control terms, and 1 set/reset control term)

(2) OR array (32×9)

32 AND terms input to 9 OR terms.

(3) Output control array (36×9)

Output from this array enables CMOS output (I/O0~I/O8).

(4) Set/reset control array (36×1)

Any input pin can be set to sync set/reset. When the AND output of signals input to this cell array becomes high, initial states for registers are set. When a register is selected and no input pin is set to sync set/reset, write 0 to all bits of this array in order to set AND output to low.

(5) Flag cell

A. Register selection cell 8 bits 0 : Does not select register.

B. Output polarity selection cell ... 9 bits 0 : Inverted output

C. Initial register setting cell 8 bit 0 : Sets register internal Q output to low.

(6) User signature cell

User can program a 42-bit memory array to store any data. Programming the security bit (security cell) disables access of cells other than the signature cell.

2. Macro cells

TC9809 has 8 macro cells containing D-type flip/flops (register).

1) Output polarity of OR array

Nine exclusive OR gates control the output polarity of the OR array in units of bits. These gates are user-programmable : setting program data to 0 inputs the output signal from the OR array as non-inverted ; setting program data to 1, as inverted.

2) Register selection

The eight output registers can be independently selected. Setting the program data to 1 selects an output register ; setting to 0 does not select an output register.

When an output register is selected, the CK/I0 pin (pin 1) is automatically set to clock input. The output is not fed back ; \bar{Q} output is fed back instead. V_{CC} is supplied to the memory cell corresponding to pin 1.

If an output register is not selected, pin 1 (like I1~I8) is set to dedicated data input. The register operates when the clock pulse goes positive. The registers have a set/reset function (described later).

3) Initial state of registers at power-up

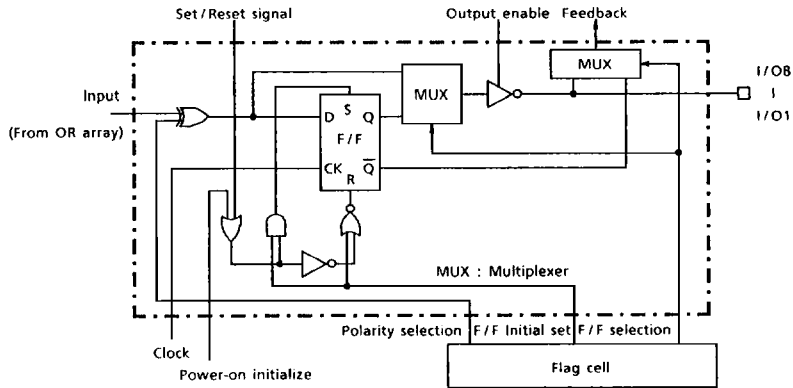
The user can program reset or preset of register outputs at power-up using 8 bits of the register initial state setting address in units of flip/flops. Setting program data to 1 presets internal Q output of flip/flop ; setting to 0 resets internal Q output.

4) Feedback circuit

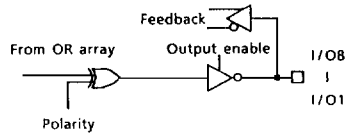
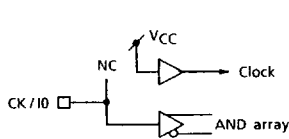
As described above, the user can program combinational output or registered output for I/O1 (pin 12) to I/O8 (pin 19).

The feedback signals are related to output selection. With combinational output, the output is fed back as is. With registered output, \bar{Q} output is fed back. Note that programming the output control array sets the I/O pins to input except when registered output is selected. (Q is output to the I/O pins or they are set to high impedance.)

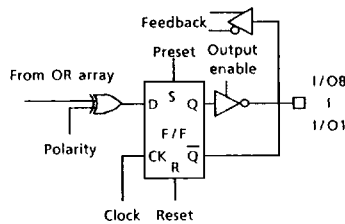
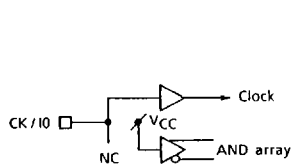
Macro Cell



A) Not selected (Program data is "0")



B) Selected (Program data is "1")



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 35	mA
DC V_{CC} /Ground Current	I_{CC}	± 70	mA
Power Dissipation	P_D	500 (DIP) * / 300 (SOL)	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temperature (10s)	T_L	300	°C

* 500mW in the range of $T_a = -40 \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.75~5.25	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt/dv	0~20 ($V_{CC} = 5 \pm 0.25\text{V}$)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYM-BOL	TEST CIR-CUIT	TEST CONDITION	Ta = 25°C			Ta = -40 ~85°C		UNIT		
				V _{CC}	MIN.	TYP.	MAX.	MIN.		MAX.	
High-level input voltage	V _{IH}	—		5.0 ± 0.25	2.0	—	—	2.0	—	V	
Low-level input voltage	V _{IL}	—		5.0 ± 0.25	—	—	0.8	—	0.8	V	
High-level output voltage	V _{OH}	—	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 μA	4.75	4.65	4.75	—	4.65	—	V
				I _{OH} = -6 mA	4.75	4.43	4.56	—	4.38	—	
Low-level output voltage	V _{OL}	—	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	4.75	—	0.0	0.1	—	0.1	V
				I _{OL} = 6 mA	4.75	—	0.18	0.26	—	0.33	
3-State output off-state current	I _{OZ}	—	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.25	—	—	± 0.5	—	± 5.0	μA	
Input leakage current	I _{IN}	—	V _{IN} = V _{CC} or GND	5.25	—	—	± 0.1	—	± 1.0		
Quiescent current	I _{CCSB}	—	V _{IN} = V _{CC} or GND Standby	5.25	—	—	4.0	—	40.0	μA	
Operating current	I _{CCOP}	—	f _{IN} = 1MHz Operating	5.25	—	—	—	—	40.0	mA	

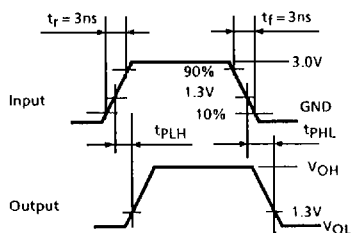
TC9809P, TC9809FW

AC ELECTRICAL CHARACTERISTICS ($C_L = 25\text{pF}$, Input $t_r = t_f = 3\text{ns}$)

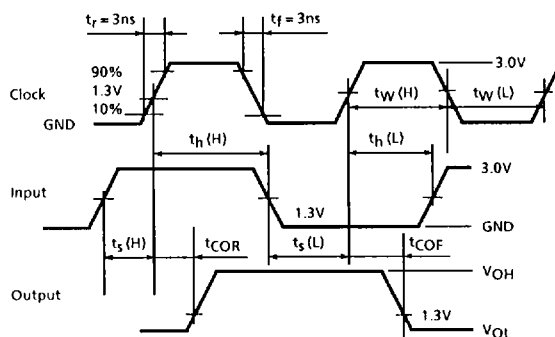
PARAMETER	SYM-BOL	TEST CIR-CUIT	TEST CONDITION	Ta = 25°C			Ta = -40 ~ 85°C		UNIT	
				V _{CC}	MIN.	TYP.	MAX.	MIN.		MAX.
Propagation Delay Time (Input, I/O-Output)	t _{PLH} t _{PHL}	—		5 ± 0.25	—	19	25	—	29	ns
Propagation Delay Time (Clock-Output)	t _{COR} t _{COF}	—		5 ± 0.25	—	9	15	—	17	ns
Propagation Delay Time (Set/reset Output)	t _{PLH} t _{PHL}	—		5 ± 0.25	—	19	25	—	29	ns
Output Enable Time	t _{PZL} t _{PZH}	—		5 ± 0.25	—	15	25	—	29	ns
Output Disable Time	t _{PLZ} t _{PHZ}	—		5 ± 0.25	—	21	29	—	34	ns
Minimum Pulse Width	t _W (L) t _W (H)	—		5 ± 0.25	—	—	5	—	6	ns
Minimum Set-up Time	t _S	—		5 ± 0.25	—	—	24	—	28	ns
Minimum Hold Time	t _H	—		5 ± 0.25	—	—	0	—	0	ns
Minimum Removal Time	t _{rem}	—		5 ± 0.25	—	—	13	—	15	ns
Maximum Clock Frequency	f _{MAX}	—		5 ± 0.25	25	—	—	22	—	MHz

Switching Characteristic Test Waveform

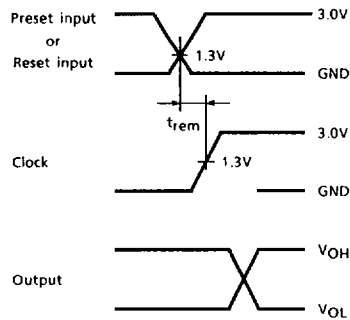
1) t_{PD} (t_{PLH}, t_{PHL})



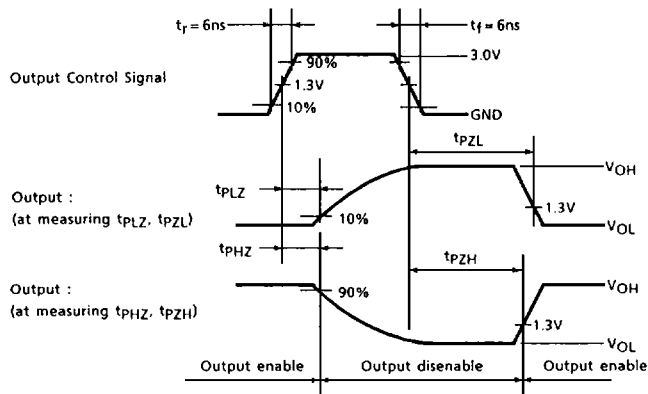
2) t_{CO} (t_{COR}, t_{COF}, t_S, t_H, t_W)



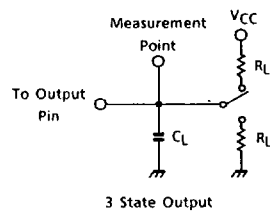
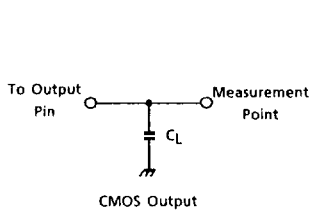
3) t_{rem}



4) t_{PLZ} , t_{PHZ} , t_{PZL} , t_{PZH}



5) Output Test Connection Diagram



Note) C_L includes the capacitance of probe.