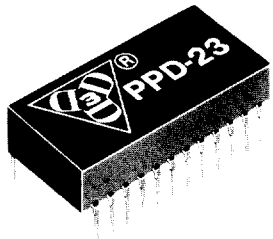
Programmable Pulse Discriminator

SERIES: PPD-23
(3 BIT) TTL Interfaced

data delay devices, inc.

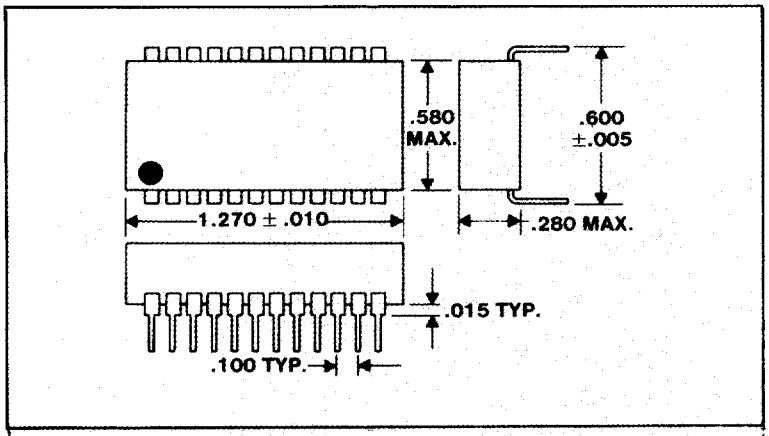


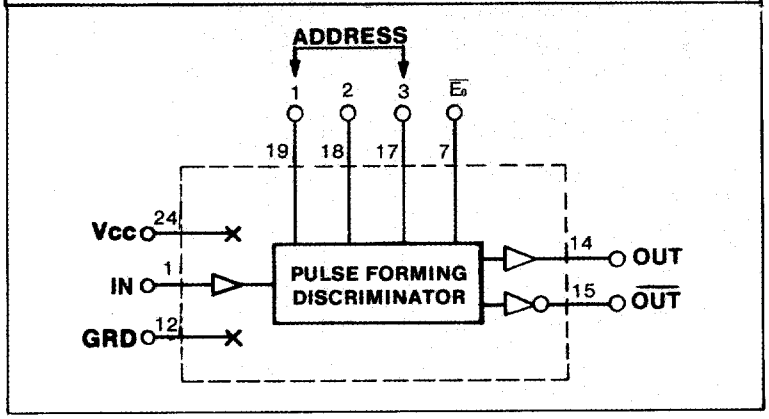
Features:

- **Discriminates against precisely programmed pulse widths.**
- **3-bit address.**
- **24 pins DIP.**
- **Low profile.**

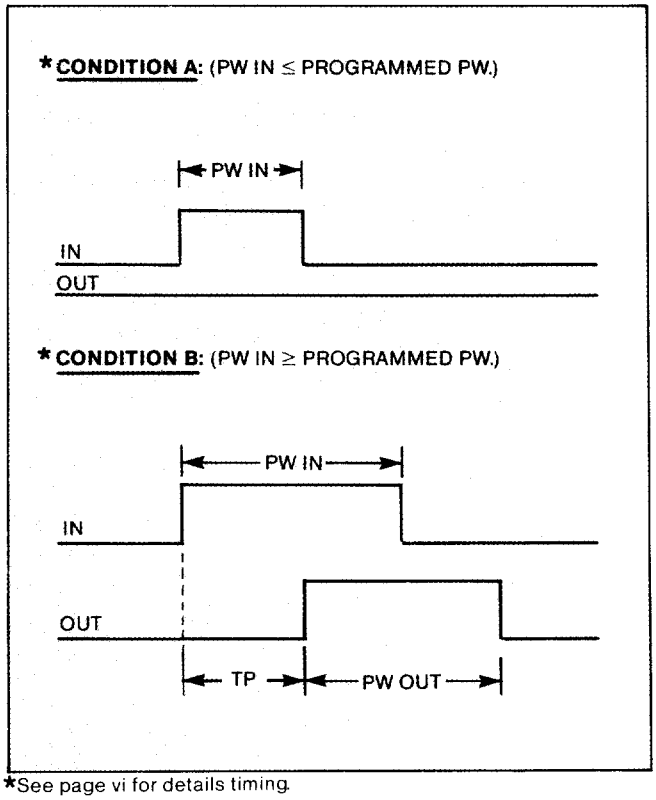
Specifications:

- **Inherent pulse width (PW_0):** 5 ns typ.
- **Supply voltage:** 5 Vdc ± 5%.
- **Operating temperatures:** 0°C to 70°C.
- **Temperature coefficient:** 100 PPM/°C.
- **Power Dissipation:** 850 mw max.
- **DC parameters:** See TTL-Standard Schottky Logic Table on Page 6.





PW IN = Input pulse width
PW OUT = Output pulse = PW IN − 4 ns
TP = Propagation delay = PW Programmed + 6 ns



*See page vi for details timing.

Part Number	Incremental Pulse Width Per Step (ns)	Total Programmed Pulse Width (ns)
PPD-23-1	1 ± .4	7
PPD-23-2	2 ± .4	14
PPD-23-3	3 ± .5	21
PPD-23-5	5 ± .6	35
PPD-23-10	10 ± 1.0	70
PPD-23-15	15 ± 1.3	105
PPD-23-20	20 ± 1.5	140
PPD-23-40	40 ± 2.0	280
PPD-23-50	50 ± 2.5	350

Contact us for specific requirements. We customize.

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