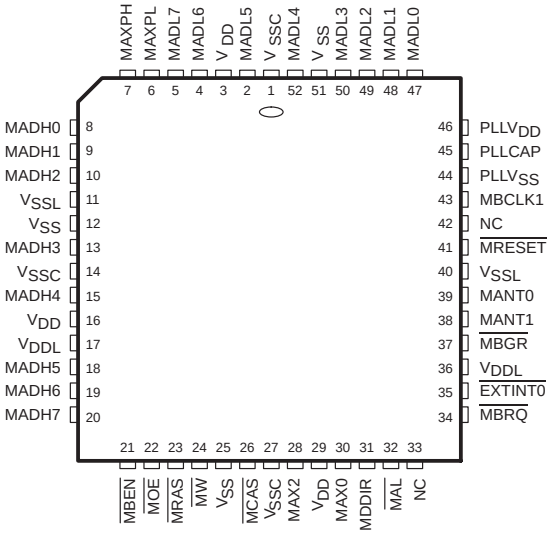
SPWS011A − MARCH 1995 − REVISED AUGUST 1995

- **Frame-Processing Accelerator for TI380C2x and TI380C3x**
- **Supports TI380C2x and TI380C3x Token-Ring™ Adapters**
- **Supports TI380C2x Ethernet™ Adapters**
- **Supports 4- or 6-MHz Adapter Local Bus Operation**
- **Interfaces Directly to TI380C2x Network Commprocessors**
- **Hardware Capture of Network Statistics**
- **Increases Adapter-Frame-Processing Rate up to 28K Frames per Second**
- **Single 5-V Supply**
- **0.8-μm CMOS Technology**
- **52-Pin Plastic Leaded Chip Carrier (FN)**
- **Operating Temperature Range 0°C to 70°C**

FN PACKAGE
(TOP VIEW)



description

The TI380FPA frame processing accelerator (FPA) provides hardware to accelerate the processing rate of frames by the network communications processor (commprocessor). It supports a 4-MHz or 6-MHz adapter local bus operation. The CPU of a normal TI380C2x or TI380C3x adapter is responsible for frame transport between network and host, gathering adapter and network statistics, local-network-management protocols, and medium-access-control (MAC) protocols. The TI380FPA puts the performance bottlenecks of frame transport and statistics gathering into dedicated hardware, leaving the CPU to run MAC and management protocols.

The TI380FPA is responsible for:

- Management of all commprocessor protocol handler (PH) operations. The FPA manages all receive- and transmit-frame queues.
- Management of adapter buffers. The FPA manages all adapter memory buffers, allocating them to the appropriate queues as required.
- Management of host direct memory access (DMA) by way of the commprocessor system interface (SIF) DMA controller.
- Management of frame transfers to the host. The FPA manages queues of frames to and from the host, manages rx/tx list information, and coordinates the two.
- Gathering adapter and network statistics in dedicated hardware counters.

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TEXAS INSTRUMENTS
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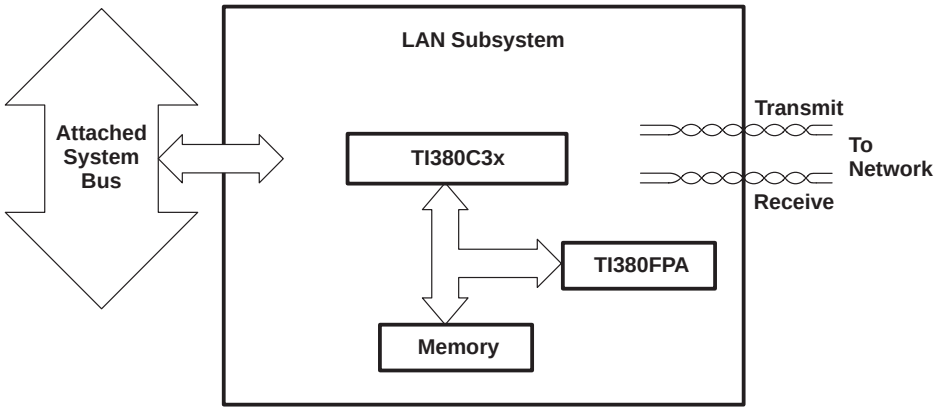

Figure 1. Network-Commprocessor Applications Diagram

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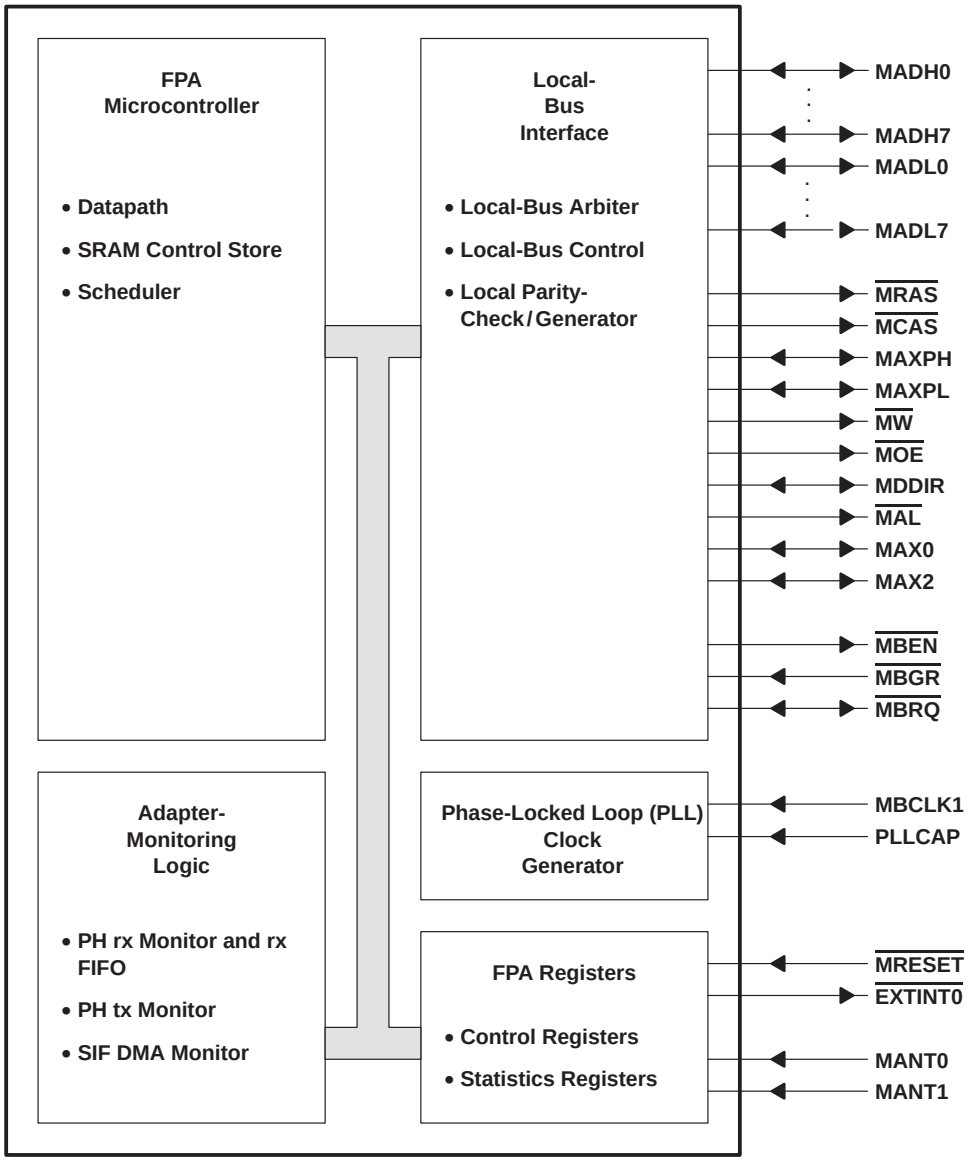
functional block diagram

TI380FPA attaches directly to the adapter local memory bus of a TI380C2x or TI380C3x commprocessor. Generally, FPA pins should be directly connected to like-named pins of the TI380C2x and TI380C3x.



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Pin Functions

PIN NAME	PIN NO.	I/O†	DESCRIPTION
$\overline{\text{EXTINT0}}$	35	O	FPA interrupt request (see Note 1)
MADH0 MADH1 MADH2 MADH3 MADH4 MADH5 MADH6 MADH7	8 9 10 13 15 18 19 20	I/O	Local-memory address, data, and status bus - high byte. For the first quarter of the local-memory cycle, MADH0−MADH7 carry address bits AX4 and A0 to A6; for the second quarter, they carry status bits; and for the third and fourth quarters, they carry data bits 0 to 7. The most significant bit is MADH0, and the least significant bit is MADH7. Memory Cycle Signal: 1Q AX4,A0−A6; 2Q Status; 3Q D0−D7; 4Q D0−D7
MADL0 MADL1 MADL2 MADL3 MADL4 MADL5 MADL6 MADL7	47 48 49 50 52 2 4 5	I/O	Local-memory address, data, and status bus - low byte. For the first quarter of the local-memory cycle, MADL0−MADL7 carry address bits A7 to A14; for the second quarter, they carry address bits AX4 and A0 to A6; and for the third and fourth quarters, they carry data bits 8 to 15. The most significant bit is MADL0, and the least significant bit is MADL7. Memory Cycle Signal: 1Q A7−A14; 2Q AX4,A0−A6; 3Q D8−D15; 4Q D8−D15
$\overline{\text{MAL}}$	32	O	Memory-address latch. $\overline{\text{MAL}}$ is a strobe signal for sampling the address at the start of the memory cycle; it is used by SRAMs and EPROMs. The full 20-bit word address is valid on MAX0, MAXPH, MAX2, MAXPL, MADH0−MADH7, and MADL0−MADL7. Three 8-bit transparent latches can be used to retain a 20-bit static address throughout the cycle. Rising edge = No signal latching Falling edge = Allows the above address signals to be latched
MANT0 MANT1	39 38	I	Test pin inputs. MANT0 and MANT1 should be left unconnected (see Note 2). Module-in-place test mode is achieved by tying MANT0 and MANT1 to ground. In this mode, all TI380FPA output pins are in the high-impedance state and internal pullups on all TI380FPA inputs are disabled (except MANT0 and MANT1).
MAX0	30	I/O	Local-memory-extended address bit. MAX0 drives AX0 at row-address time, which can be located by $\overline{\text{MRAS}}$. Normally, MAX0 drives A12 at column address and data time for all cycles. Memory Cycle Signal: 1Q AX0; 2Q A12; 3Q A12; 4Q A12
MAX2	28	I/O	Local-memory-extended address bit. MAX2 drives AX2 at row address time, which can be located by $\overline{\text{MRAS}}$. Normally, MAX2 drives A14 at column address and data time for all cycles. Memory Cycle Signal: 1Q AX2; 2Q A14; 3Q A14; 4Q A14
MAXPH	7	I/O	Local-memory-extended address and parity-high byte. For the first quarter of a memory cycle, MAXPH carries the extended address bit AX1; for the second quarter of a memory cycle, MAXPH carries the extended address bit AX0; and for the last half of the memory cycle, MAXPH carries the parity bit for the high-data byte. Memory Cycle Signal: 1Q AX1; 2Q AX0; 3Q Parity; 4Q Parity

† I = input, O = output

NOTES: 1. Pin has an open-collector output. $\overline{\text{EXTINT0}}$ should have an individual 1-kΩ pullup resistor. A 4.7-kΩ resistor can lead to transmit underruns in the adapter system and should not be used. For this reason, a 1-kΩ resistor is specified.

2. Pin has an internal pullup device to maintain a high-voltage level when left unconnected (no etch or loads). Alternatively, both pins tied together can be pulled high through a single 4.7-Ω pullup resistor.

Pin Functions (Continued)

PIN NAME	PIN NO.	I/O†	DESCRIPTION
MAXPL	6	I/O	Local-memory-extended address and parity-low byte. For the first quarter of a memory cycle, MAXPL carries the extended address bit AX3; for the second quarter of a memory cycle, MAXPL carries extended address bit AX2; and for the last half of the memory cycle, MAXPL carries the parity bit for the low-data byte. Memory Cycle Signal: 1Q AX3, 2Q AX2, 3Q Parity, 4Q Parity
MBCLK1	43	I	Local-bus clock 1. MBCLK1 is referenced for all local-bus transfers.
$\overline{\text{MBEN}}$	21	O	Buffer enable. $\overline{\text{MBEN}}$ enables the bidirectional buffer outputs on the MADH, MAXPH, MAXPL, and MADL buses during the data phase. $\overline{\text{MBEN}}$ is used in conjunction with MDDIR, which selects the buffer output direction. H = Buffer output disabled L = Buffer output enabled
$\overline{\text{MBGR}}$	37	I	Local bus grant. $\overline{\text{MBGR}}$ indicates that the FPA has been granted access to the adapter local-memory bus.
$\overline{\text{MBRQ}}$	34	I/O	Local bus request. $\overline{\text{MBRQ}}$ is used by the FPA to request bus-master access to the adapter local-memory bus. The FPA also monitors $\overline{\text{MBRQ}}$ to allow it to defer to other higher-priority bus requests (see Note 1).
$\overline{\text{MCAS}}$	26	O	Column-address strobe for DRAMs. The column address is valid for the 3/16 of the memory cycle following the row-address portion of the cycle. $\overline{\text{MCAS}}$ is driven low every memory cycle while the column address is valid on MADL0−MADL7, MAXPH, and MAXPL, except when one of the following conditions occurs: 1) When the address accessed is a TI380C2x or TI380C3x internal register (>01.0100 − >01.01FF). 2) When the address accessed is in the TI380C2x or TI380C3x external device-address range (>01.0200 − >01.02FF). This address range includes the FPA registers. 3) When the FPA ROM bit is set, and the address accessed is in adapter ROM-address range (>00.0000−>00.FFFE or >1F.0000−>1F.FFFE).
MDDIR	31	I/O	Data direction. MDDIR is used as a direction control for bidirectional bus drivers. MDDIR becomes valid before $\overline{\text{MBEN}}$ becomes active. H = TI380FPA memory bus write L = TI380FPA memory bus read
$\overline{\text{MOE}}$	22	O	Memory output enable. $\overline{\text{MOE}}$ is used to enable the outputs of the DRAM memory during a read cycle. $\overline{\text{MOE}}$ is high for EPROM or BIA ROM read cycles. 1) When the address read is a TI380C2x or TI380C3x internal register (>01.0100−>01.01FF). 2) When the address read is in the TI380C2x or TI380C3x external device-address range (>01.0200−>01.02FF). This address range includes the FPA registers. 3) When the FPA ROM bit is set, and the address read is in adapter ROM-address range (>00.0000−>00.FFFE or 1F.0000−1F.FFFE). H= Disable DRAM outputs L = Enable DRAM outputs
$\overline{\text{MRAS}}$	23	O	Row-address strobe for DRAMs. The row address lasts for the first 5/16 of the memory cycle. $\overline{\text{MRAS}}$ is driven low every memory cycle while the row address is valid on MADL0−MADL7, MAXPH, and MAXPL for both RAM and register-access cycles.
$\overline{\text{MRESET}}$	41	I	Memory bus reset. $\overline{\text{MRESET}}$ is the reset signal provided by the TI380C2x or TI380C3x and is used to reset and initialize the FPA internal logic. While $\overline{\text{MRESET}}$ is asserted, all FPA output pins are in the high-impedance state.

† I = input, O = output

NOTE 1: Pin has an open-collector output. $\overline{\text{EXTINT0}}$ should have an individual 1-kΩ pullup resistor. A 4.7-kΩ resistor can lead to transmit underruns in the adapter system and should not be used. For this reason, a 1-kΩ resistor is specified.

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Pin Functions (Continued)

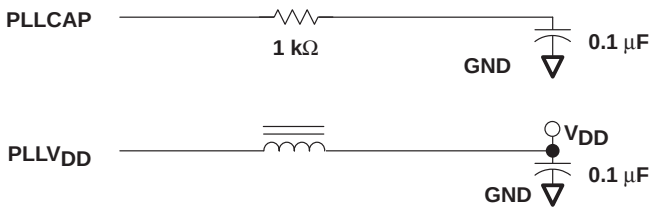
PIN NAME	PIN NO.	I/O†	DESCRIPTION
$\overline{MW}$	24	O	Local-memory write. $\overline{MW}$ is used to specify a write cycle on the local-memory bus. The data on the MADH0−MADH7 and MADL0−MADL7 buses is valid while $\overline{MW}$ is low. DRAMs latch data on the falling edge $\overline{MW}$, while SRAMs latch data on the rising edge of $\overline{MW}$. H = Not a local memory-write cycle L = Local memory write-cycle
NC	33 42		No connect. Do not connect these pins.
PLLCAP	45	I	Phase-locked loop (PLL) tuning capacitor (see Note 3).
V_{DDL}	17 36	I	Positive-supply voltage for digital logic. All V_{DDL} pins must be attached to the common-system power-supply plane.
V_{DD}	3 16 29	I	Positive-supply voltage for output buffers. All V_{DDL} pins must be attached to the common-system power-supply plane.
$PLLV_{DD}$	46	I	Positive-supply voltage for phase-locked loop (see Note 4).
V_{SSC}	1 14 27	I	Ground reference for output buffers (clean ground). All V_{SSC} pins must be attached to the common-system-ground plane.
V_{SSL}	11 40	I	Ground reference for digital logic. All V_{SSL} pins must be attached to the common-system-ground plane.
V_{SS}	12 25 51	I	Ground connections for output buffers. All V_{SS} pins must be attached to common-system-ground plane.
$PLLV_{SS}$	44	I	Ground reference for phase-locked loop. Attach to the common-system-ground plane.

† I = input, O = output

NOTES: 2. Pin has an internal pullup device to maintain a high-voltage external level when left unconnected. Alternatively, both pins tied together can be pulled high through a single 4.7-Ω pullup resistor.

3. The PLLCAP requires the following connection: These components must be placed as close as possible to PLLCAP.

4. Isolate $PLLV_{DD}$ to a separate PLL power pad with ferrite bead separation from the common-system power-supply plane. A 0.1-µF decoupling capacitor on $PLLV_{DD}$ is also necessary as shown. These components must be placed as close as possible to $PLLV_{DD}$.



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instructions for reading TI380FPA silicon revision code

The TI380FPA contains a register which returns a hard-wired value reflecting the revision of the TI380FPA silicon. The register can be read only before the CPHALT bit (in the SIFACL register) is cleared and the bring-up diagnostics (BUD) begins executing.

The following steps should be taken to read the revision register:

1. Set the ARESET bit in the SIFACL register (bit 8) to 1.
2. Wait a minimum of 14 μs for the reset to take place.
3. Clear the ARESET bit and set the CPHALT bit in the same write to the SIFACL register.
4. One hundred μs after step 3, read adapter memory location 01.023E to obtain the silicon revision level.

Steps 1 through 3 are explained in more detail in the *TMS380 Second-Generation Token-Ring User's Guide* (literature number SPWU005).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 5) . . . . . − 0.6 to 7 V
Input voltage range (see Note 5) . . . . . − 0.3 V to 20 V
Output voltage range . . . . . − 2 V to 7 V
Power dissipation . . . . . 0.5 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 5: Voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage (see Note 6)	0	0	0	V
V_{IH}	High-level input voltage	2.0		V_{DD}+0.3	V
V_{IL}	Low-level input voltage, TTL-level signal (see Note 7)	−0.3		0.8	V
I_{OH}	High-level output current			−400	µA
I_{OL}	Low-level output current (see Note 8)			2	mA
T_A	Operating free-air temperature	0		70	°C

NOTES: 6. All V_{SS} pins should be routed to system ground to minimize inductance.
7. The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used for logic-voltage levels only.
8. Output current of 2 mA is sufficient to drive five low-power Schottky TTL loads or ten advanced low-power Schottky TTL loads (worst case).

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS (SEE NOTE 9)		MIN	MAX	UNIT
V_{OH}	High-level output voltage, TTL-level signal (see Note 10)	V_{DD} = MIN,	I_{OH} = MAX	2.4		V
V_{OL}	Low-level output voltage, TTL-level signal	V_{DD} = MIN,	I_{OL} = MAX		0.6	V
I_O	High-impedance output current	V_{DD} = MAX,	V_O = 2.4 V		20	µA
		V_{DD} = MAX,	V_O = 0.4 V		− 20	
I_I	Input current, any input or input/output pin	V_I = V_{SS} to V_{DD}			± 20	µA
I_{DD}	Supply current	V_{DD} = MAX			110	mA
C_i	Input capacitance, any input	f = 1 MHz,	Others at 0 V		15	pF
C_o	Output capacitance, any output or input/output	f = 1 MHz,	Others at 0 V		15	pF

NOTES: 9. For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions.
10. The following signals require an external pullup resistor: $\overline{\text{EXTINT0}}$ and $\overline{\text{MBRQ}}$.

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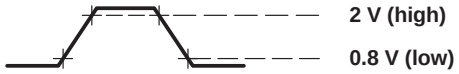
test measurement

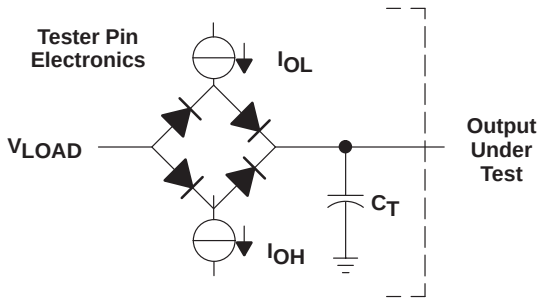
Outputs are driven to a minimum high-logic level of 2.4 V and to a maximum low-logic level of 0.6 V. These levels are compatible with TTL devices.

Output transition times are specified as follows: for a high-to-low transition on either an input or output signal, the level at which the signal is said to be no longer high is 2 V, and the level at which the signal is said to be low is 0.8 V. For a low-to-high transition, the level at which the signal is said to be no longer low is 0.8 V, and the level at which the signal is said to be high is 2 V, as shown below.

The rise and fall times are not specified but are assumed to be those of standard TTL devices, which are typically 1.5 ns.



The test load circuit shown in Figure 2 represents the programmable load of the tester-pin electronics, that are used to verify timing parameters of TI380FPA output signals.



Where: I_{OL} = 2 mA DC-level verification (all outputs)

I_{OH} = 400 μA (all outputs)

V_{LOAD} = 1.5 V, typical dc-level verification
0.7 V, typical timing verification

C_T = 65 pF, typical load-circuit capacitance

Figure 2. Test-Load Circuit

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timing parameters

The timing parameters for all the pins of TI380FPA are shown in the following tables and are illustrated in the accompanying figures. The purpose of these figures and tables is to quantify the timing relationships among the various signals. The parameters are numbered for convenience.

static signals

The following table lists signals that are not allowed to change dynamically and have no timing associated with them. They should be strapped high or low as required.

SIGNAL	FUNCTION
MANT0	Test pin for TI manufacturing test†
MANT1	Test pin for TI manufacturing test†

† For unit-in-place test

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as shown below:

DR	DRVR	RS	
DRN	$\overline{\text{DRVR}}$	VDD	V_{DDL}
OSC	OSCIN		
SCK	SBCLK		

Lower-case subscripts are defined as follows:

c	cycle time	r	rise time
d	delay time	sk	skew
h	hold time	su	setup time
w	pulse duration (width)	t	transition time

The following additional letters and phrases are defined as follows:

H	High	Z	High impedance
L	Low	Falling edge	No longer high
V	Valid	Rising edge	No longer low

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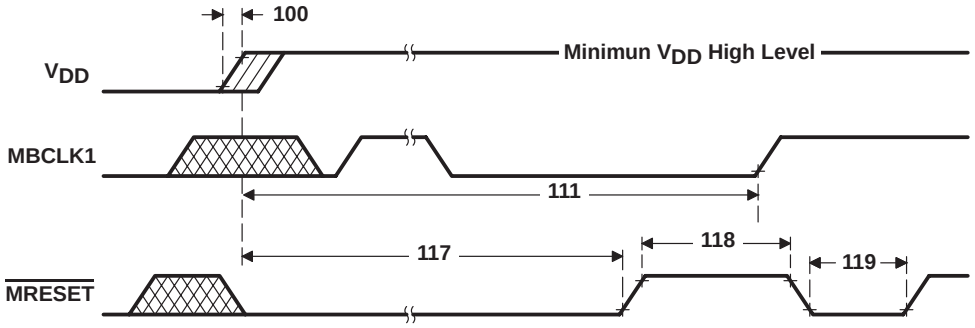
power up, MBCLK1, $\overline{\text{MRESET}}$ timing

NO.			MIN	MAX	UNIT
100†	$t_{r(VDD)}$	Rise time, 1.2 V to minimum V_{DD}-high level		1	ms
111†	$t_{d(CKV)}$	Delay time, minimum V_{DD}-high level to MBCLK1 valid		3	ms
117†	$t_{h(VDDH-RSL)}$	Hold time, $\overline{\text{MRESET}}$ low after V_{DD} reaches minimum high level	5		ms
118†	$t_{w(RSH)}$	Pulse duration, $\overline{\text{MRESET}}$ high	14		µs
119†	$t_{w(RSL)}$	Pulse duration, $\overline{\text{MRESET}}$ low	14		µs

† This specification is provided as an aid to board design. This specification is not tested.



NOTE A: In order to represent the information on one illustration, nonactual phase and timebase characteristics are shown. Refer to specified parameters for precise information.

Figure 3. Power Up, MBCLK1, and $\overline{\text{MRESET}}$ Timing

clock timing: MBCLK1

t_M is the cycle time of one-eighth of a local-memory cycle (20.83 ns minimum).

NO.		MIN	MAX	UNIT
1	Period of MBCLK1	83.3		ns
2	Pulse duration, MBCLK1 high	33		ns
3	Pulse duration, MBCLK1 low	33		ns
4	Transition time, MBCLK1	5		ns

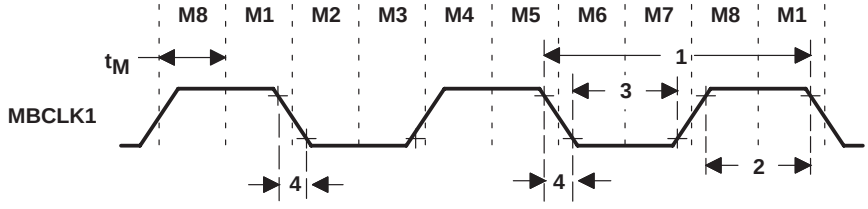


Figure 4. Clock Timing: MBCLK1

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FPA-bus-master timing: $\overline{\text{MAL}}$, $\overline{\text{MRESET}}$, and ADDRESS

t_M is the cycle time of one-eighth of a local-memory cycle (20.83 ns minimum).

NO.		MIN	MAX	UNIT
8	Setup time, address/enable on MAX0 and MAX2 before MBCLK1 no longer high	t_M-9		ns
9	Setup time, row address on MADL0−MADL7, MAXPH, and MAXPL before MBCLK1 no longer high	t_M-14		ns
10	Setup time, address on MADH0−MADH7 before MBCLK1 no longer high	t_M-14		ns
11	Setup time, $\overline{\text{MAL}}$ high before MBCLK1 no longer high	t_M-13		ns
12	Setup time, address on MAX0 and MAX2 before MBCLK1 no longer low	$0.5t_M-9$		ns
13	Setup time, column address on MADL0−MADL7, MAXPH, and MAXPL before MBCLK1 no longer low	$0.5t_M-9$		ns
14	Setup time, status on MADH0−MADH7 before MBCLK1 no longer low	$0.5t_M-9$		ns
126	Delay time, MBCLK1 no longer low to $\overline{\text{MRESET}}$ valid	0	20	ns
129	Hold time, column address/status after MBCLK1 no longer low	t_M-7		ns

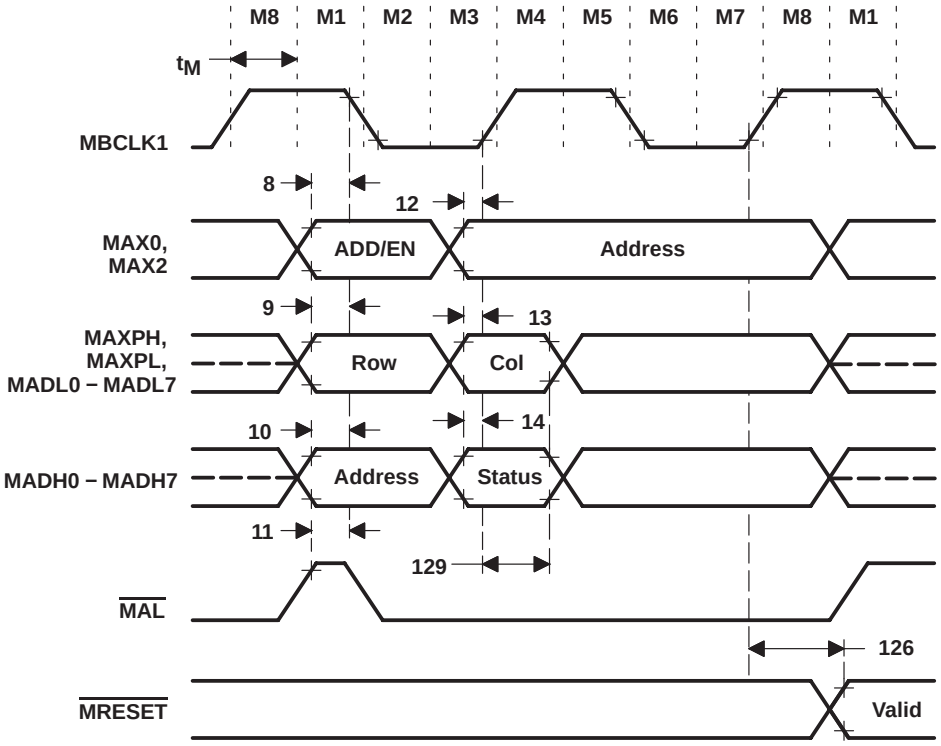

Figure 5. FPA-Bus-Master Timing: $\overline{\text{MAL}}$, $\overline{\text{MRESET}}$, and ADDRESS

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FPA-bus-master timing: $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, and $\overline{\text{MAL}}$ to ADDRESS

t_M is the cycle time of one-eighth of a local-memory cycle (20.83 ns minimum).

NO.		MIN	MAX	UNIT
15	Setup time, row address on MADL0−MADL7, MAXPH, and MAXPL before $\overline{\text{MRAS}}$ no longer high	$1.5t_M - 11.5$		ns
16	Hold time, row address on MADL0−MADL7, MAXPH, and MAXPL after $\overline{\text{MRAS}}$ no longer high	$t_M - 6.5$		ns
17	Delay time, $\overline{\text{MRAS}}$ no longer high to $\overline{\text{MRAS}}$ no longer high in the next memory cycle	$8t_M$		ns
18	Pulse duration, $\overline{\text{MRAS}}$ low	$4.5t_M - 9$		ns
19	Pulse duration, $\overline{\text{MRAS}}$ high	$3.5t_M - 9$		ns
20	Setup time, column address (MADL0−MADL7, MAXPH, and MAXPL) and status (MADH0−MADH7) before $\overline{\text{MCAS}}$ no longer high	$0.5t_M - 9$		ns
21	Hold time, column address (MADL0−MADL7, MAXPH, and MAXPL) and status (MADH0−MADH7) after $\overline{\text{MCAS}}$ low	$t_M - 9$		ns
22	Hold time, column address (MADL0−MADL7, MAXPH, and MAXPL) and status (MADH0−MADH7) after $\overline{\text{MRAS}}$ no longer high	$2.5t_M - 6.5$		ns
23	Pulse duration, $\overline{\text{MCAS}}$ low	$3t_M - 9$		ns
24	Pulse duration, $\overline{\text{MCAS}}$ high, refresh cycle follows read or write cycle	$2t_M - 9$		ns
25	Hold time, row address on MADL0−MADL7, MAXPH, and MAXPL after $\overline{\text{MAL}}$ low	$1.5t_M - 9$		ns
26	Setup time, row address on MADL0−MADL7, MAXPH, and MAXPL before $\overline{\text{MAL}}$ no longer high	$t_M - 9$		ns
27	Pulse duration, $\overline{\text{MAL}}$ high	$t_M - 9$		ns
28	Setup time, address/enable on MAX0 and MAX2 before $\overline{\text{MAL}}$ no longer high	$t_M - 9$		ns
29	Hold time, address/enable of MAX0 and MAX2 after $\overline{\text{MAL}}$ low	$1.5t_M - 9$		ns
30	Setup time, address on MADH0−MADH7 before $\overline{\text{MAL}}$ no longer high	$t_M - 9$		ns
31	Hold time, address on MADH0−MADH7 after $\overline{\text{MAL}}$ low	$1.5t_M - 9$		ns

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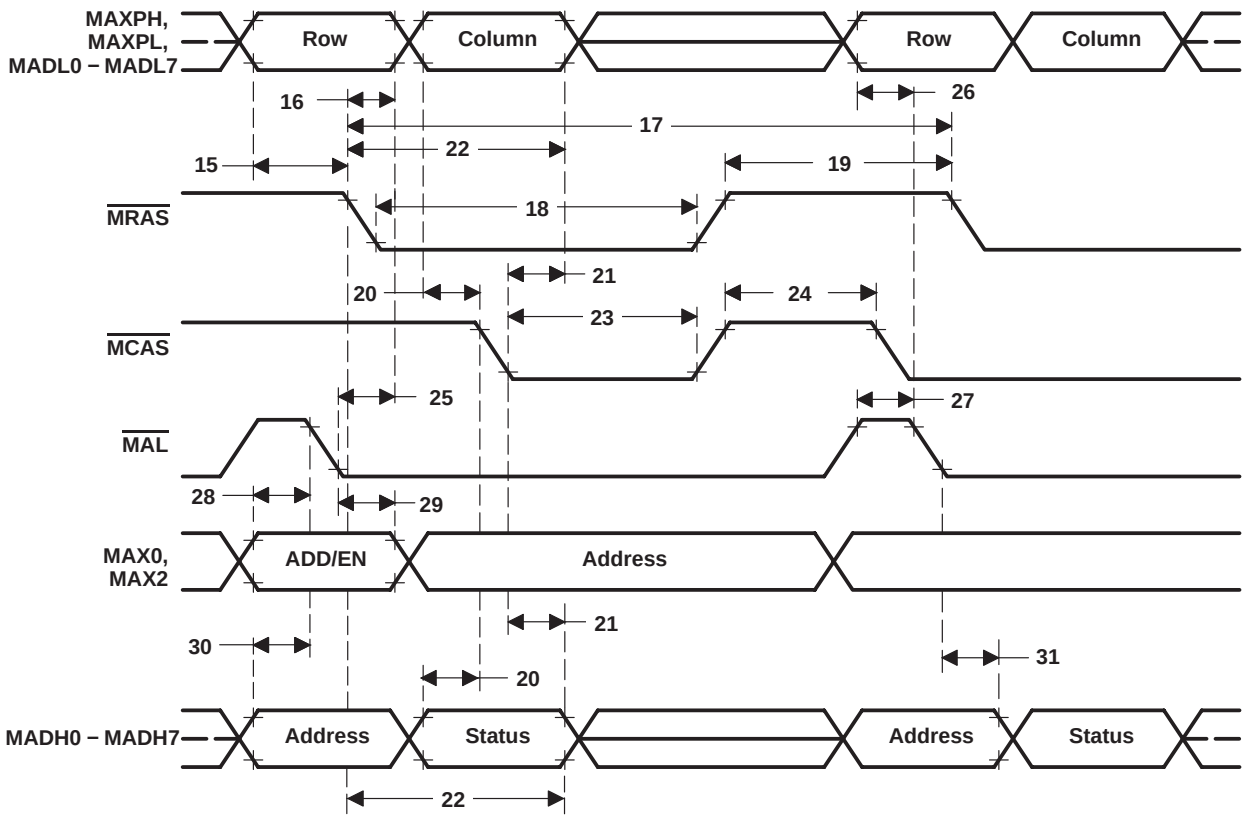

Figure 6. FPA-Bus-Master Timing: $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, and $\overline{\text{MAL}}$ to ADDRESS

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FPA-bus-master timing: read cycle

t_M is the cycle time of one-eighth of a local-memory cycle (20.83 ns minimum).

NO.		MIN	MAX	UNIT
32	Access time, address/enable valid on MAX0 and MAX2 to valid data/parity		$6t_M - 23$	ns
33	Access time, address valid on MAXPH, MAXPL, MADH0−MADH7, and MADL0−MADL7 to valid data/parity		$6t_M - 23$	ns
35	Access time, $\overline{\text{MRAS}}$ low to valid data/parity		$4.5t_M - 21.5$	ns
36	Hold time, valid data/parity after $\overline{\text{MRAS}}$ no longer low	0		ns
37†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0−MADH7 and MADL0−MADL7 after $\overline{\text{MRAS}}$ high (see Note 11)	$2t_M - 10.5$		ns
38	Access time, $\overline{\text{MCAS}}$ low to valid data/parity		$3t_M - 23$	ns
39	Hold time, valid data/parity after $\overline{\text{MCAS}}$ no longer low	0		ns
40†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0−MADH7, and MADL0−MADL7 after $\overline{\text{MCAS}}$ high (see Note 11)	$2t_M - 13$		ns
41	Delay time, $\overline{\text{MCAS}}$ no longer high to $\overline{\text{MOE}}$ low		$t_M + 13$	ns
42†	Setup time, address/status in the high-impedance state on MAXPH, MAXPL, MADL0−MADL7, and MADH0−MADH7 before $\overline{\text{MOE}}$ no longer high	0		ns
43	Access time, $\overline{\text{MOE}}$ low to valid data/parity		$2t_M - 25$	ns
44	Pulse duration, $\overline{\text{MOE}}$ low	$2t_M - 9$		ns
45	Delay time, $\overline{\text{MCAS}}$ low to $\overline{\text{MOE}}$ no longer low	$3t_M - 9$		ns
46	Hold time, valid data/parity in after $\overline{\text{MOE}}$ no longer low	0		ns
47†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0−MADH7, and MADL0−MADL7 after $\overline{\text{MOE}}$ high (see Note 11)	$2t_M - 15$		ns
48†	Setup time, address/status in the high-impedance state on MAXPH, MAXPL, MADL0−MADL7, and MADH0−MADH7, before $\overline{\text{MBEN}}$ no longer high	0		ns
49	Access time, $\overline{\text{MBEN}}$ low to valid data/parity		$2t_M - 25$	ns
50	Pulse duration, $\overline{\text{MBEN}}$ low	$2t_M - 9$		ns
51	Hold time, valid data/parity after $\overline{\text{MBEN}}$ no longer low	0		ns
52†	Hold time, address in the high-impedance state on MAXPH, MAXPL, MADH0−MADH7, and MADL0−MADL7 after $\overline{\text{MBEN}}$ high (see Note 11)	$2t_M - 15$		ns
53	Hold time, MDDIR high after $\overline{\text{MBEN}}$ high, read follows write cycle	$1.5t_M - 12$		ns
54	Setup time, MDDIR low before $\overline{\text{MBEN}}$ no longer high	$3t_M - 9$		ns
55	Hold time, MDDIR low after $\overline{\text{MBEN}}$ high, write follows read cycle	$3t_M - 12$		ns

† This specification has been characterized to meet stated value. This parameter is not tested.

NOTE 11: The data/parity that exists on the address lines will most likely achieve the high-impedance state sometime later than the rising edge of $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, $\overline{\text{MOE}}$, or $\overline{\text{MBEN}}$ (between MIN and MAX of timing parameter 36) and will be a function of the memory being read. The MIN time given represents the time from the rising edge of $\overline{\text{MRAS}}$, $\overline{\text{MCAS}}$, $\overline{\text{MOE}}$, or $\overline{\text{MBEN}}$ to the beginning of the next address and does not represent the actual high-impedance state on the address bus.

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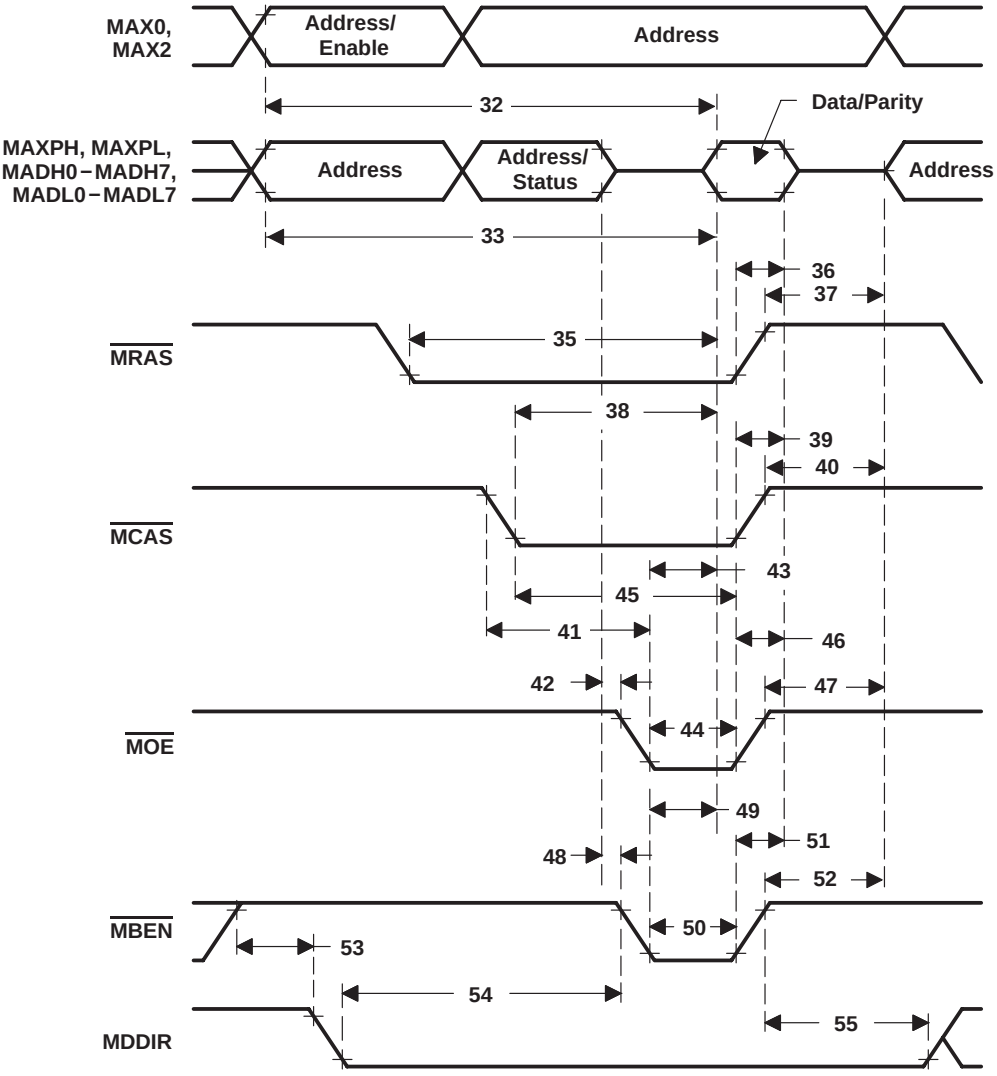

Figure 7. FPA-Bus-Master Timing: Read Cycle

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FPA-bus-master timing: write cycle

t_M is the cycle time of one-eighth of a local-memory cycle (20.83 ns minimum).

NO.		MIN	MAX	UNIT
58	Setup time, $\overline{MW}$ low before $\overline{MRAS}$ no longer low	$1.5t_M - 9$		ns
60	Setup time, $\overline{MW}$ low before $\overline{MCAS}$ no longer low	$1.5t_M - 6.5$		ns
63	Setup time, valid data/parity before $\overline{MW}$ no longer high	$0.5t_M - 11.5$		ns
64	Pulse duration, $\overline{MW}$ low	$2.5t_M - 9$		ns
65	Hold time, data/parity out valid after $\overline{MW}$ high	$0.5t_M - 10.5$		ns
66	Setup time, address valid on MAX0 and MAX2 before $\overline{MW}$ no longer low	$7t_M - 11.5$		ns
67	Hold time, $\overline{MRAS}$ low to $\overline{MW}$ no longer low	$5.5t_M - 9$		ns
69	Hold time, $\overline{MCAS}$ low to $\overline{MW}$ no longer low	$4t_M - 11.5$		ns
70	Setup time, $\overline{MBEN}$ low before $\overline{MW}$ no longer high	$1.5t_M - 13.5$		ns
71	Hold time, $\overline{MBEN}$ low after $\overline{MW}$ high	$0.5t_M - 6.5$		ns
72	Setup time, MDDIR high before $\overline{MBEN}$ no longer high	$2t_M - 9$		ns
73	Hold time, MDDIR high after $\overline{MBEN}$ high	$1.5t_M - 12$		ns

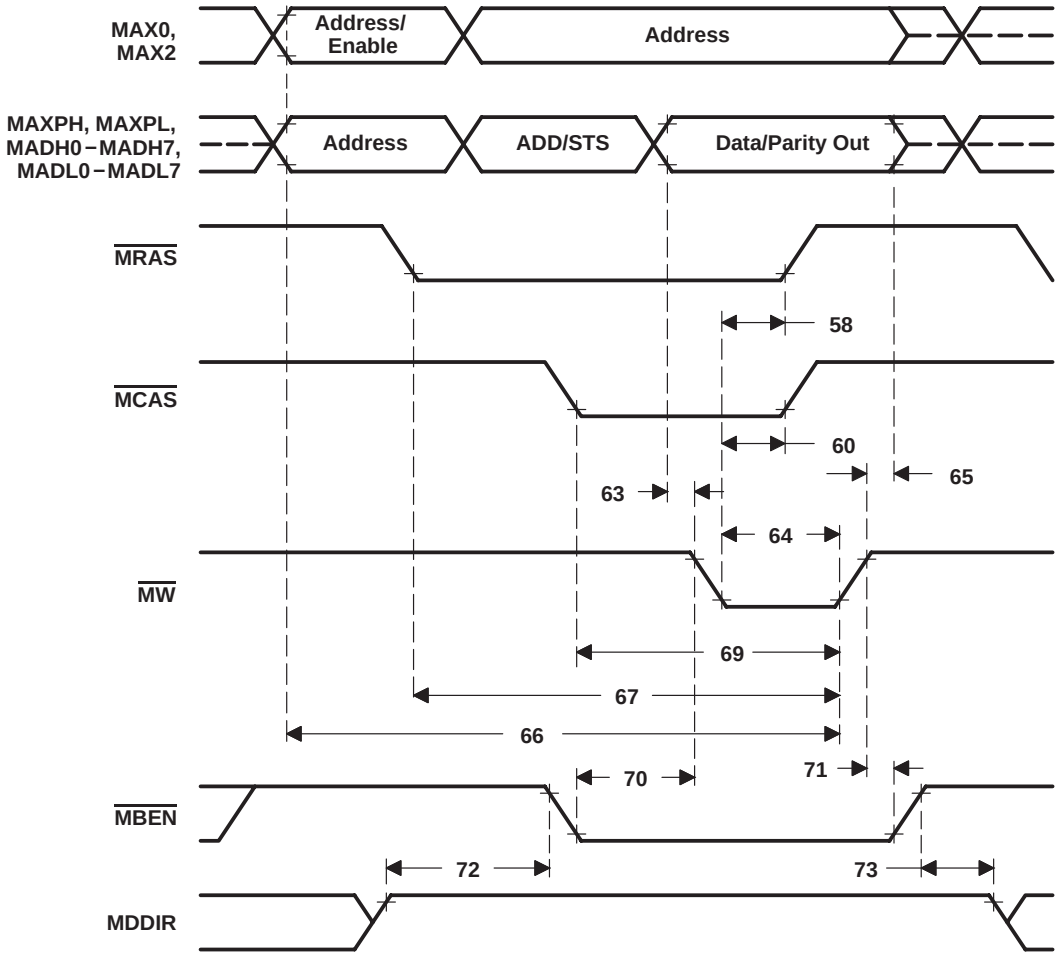

Figure 8. FPA-Bus-Master Timing: Write Cycle

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PARAMETER MEASUREMENT INFORMATION

FPA-slave timing: read cycle

t_M is the cycle time of one-eighth of a local-memory cycle (20.83 ns minimum).

NO.		MIN	MAX	UNIT
84	Setup time, address on MAX0, MAX2 before MBCLK1 falling edge, FPA-slave read	10		ns
85	Hold time, address on MAX0, MAX2 after MBCLK1 falling edge, FPA-slave read	0		ns
86	Setup time, valid address before MBCLK1 falling edge, FPA-slave read	10		ns
87	Hold time, valid address after MBCLK1 falling edge, FPA-slave read	0		ns
88	Setup time, address in the high-impedance state before MBCLK1 falling edge, FPA-slave read	0		ns
89	Setup time, data/parity valid after MBCLK1 falling edge, FPA-slave read	$0.5t_M + 10$		ns
90	Hold time, data/parity valid after MBCLK1 falling edge, FPA-slave read	$2t_M$		ns
91	Setup time, data/parity in the high-impedance state after MBCLK1 falling edge, FPA-slave read	$2t_M + 9$		ns
92	Setup time, MDDIR low after MBCLK1 falling edge, FPA-slave read	$t_M − 15$		ns
93	Hold time, MDDIR low after MBCLK1 falling edge, FPA-slave read	t_M		ns

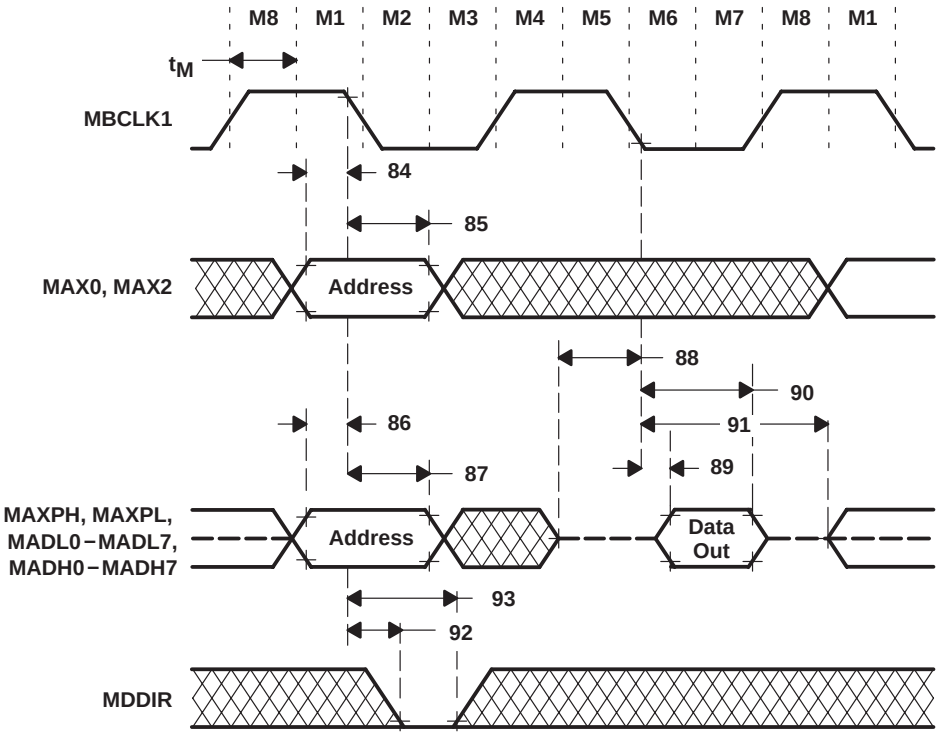

Figure 9. FPA-Slave Timing: Read Cycle

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PARAMETER MEASUREMENT INFORMATION

FPA-slave timing: write cycle

t_M is the cycle time of one-eighth of a local-memory cycle (20.83 ns minimum).

NO.		MIN	MAX	UNIT
84	Setup time, address on MAX0, MAX2 before MBCLK1 falling edge, FPA-slave read	10		ns
85	Hold time, address on MAX0, MAX2 after MBCLK1 falling edge, FPA-slave read	0		ns
86	Setup time, valid address before MBCLK1 falling edge, FPA-slave read	10		ns
87	Hold time, valid address after MBCLK1 falling edge, FPA-slave read	0		ns
96	Setup time, valid data/parity after MBCLK1 falling edge, FPA-slave write	t_M − 15		ns
97	Hold time, valid data/parity after MBCLK1 falling edge, FPA-slave write	t_M		ns
98	Setup time, MDDIR high after MBCLK1 falling edge, FPA-slave write	t_M − 15		ns
99	Hold time, MDDIR high after MBCLK1 falling edge, FPA-slave read	t_M		ns

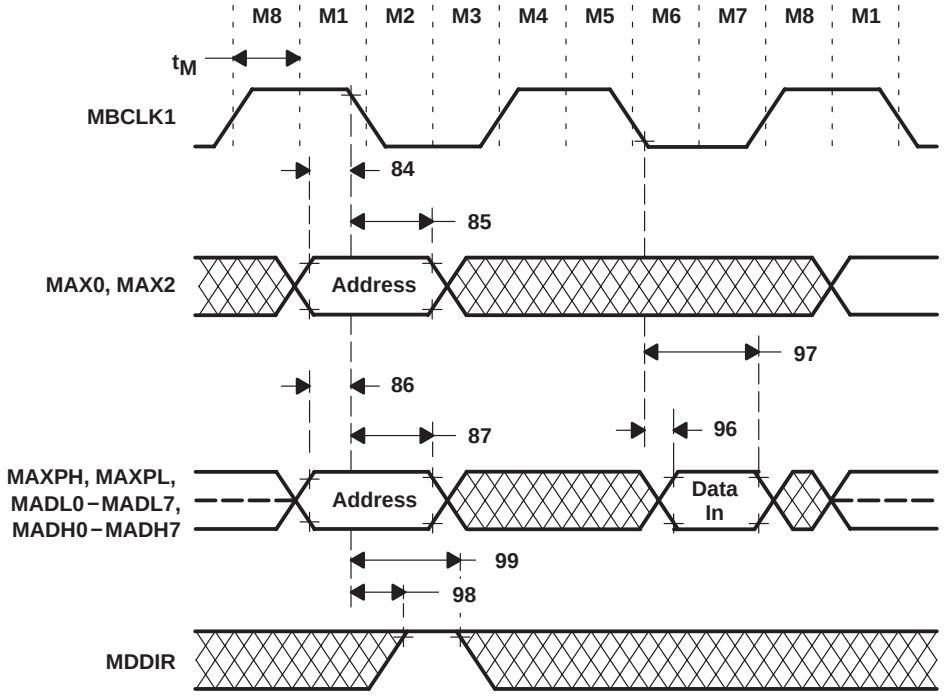

Figure 10. FPA-Slave Timing: Write Cycle

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FPA-slave timing: status monitoring

t_M is the cycle time of one-eighth of a local-memory cycle (20.83 ns minimum).

NO.		MIN	MAX	UNIT
100	Setup time, valid bus status on MADH0−MADH7 after MBCLK1 falling edge, FPA-slave cycle	$2t_M - 5$		ns
101	Hold time, valid bus status on MADH0−MADH7 after MBCLK1 falling edge, FPA-slave cycle	$2t_M + 10$		ns

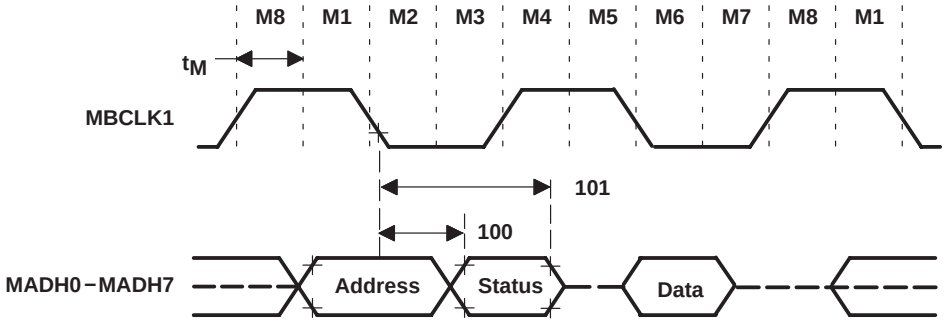

Figure 11. FPA-Slave Timing: Status Monitoring

FPA-bus arbitration: arbitration handshake

t_M is the cycle time of one-eighth of a local-memory cycle (20.83 ns minimum).

NO.		MIN	MAX	UNIT
76	Setup time, $\overline{\text{MBRQ}}$ output low before MBCLK1 falling edge, FPA-bus request	10		ns
77	Hold time, $\overline{\text{MBRQ}}$ output low after MBCLK1 falling edge, FPA-bus request	$3t_M$		ns
78	Delay time, $\overline{\text{MBGR}}$ low after MBCLK1 falling edge, bus granted to FPA	10		ns
81	Setup time, $\overline{\text{MBRQ}}$ input valid before MBCLK1 falling edge, request override	0		ns
82	Hold time, $\overline{\text{MBRQ}}$ input valid before MBCLK1 falling edge, request override	t_M		ns
83	Delay time, $\overline{\text{MBGR}}$ high after MBCLK1 falling edge, bus taken from FPA	0		ns

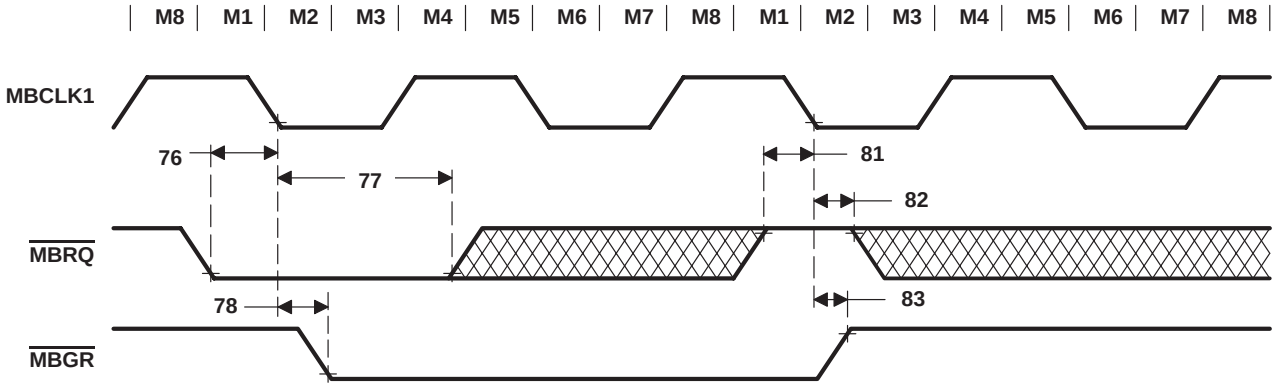

Figure 12. FPA-Bus Arbitration: Arbitration Handshake

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FPA-bus arbitration: FPA takes control of bus

t_M is the cycle time of one-eighth of a local-memory cycle (20.83 ns minimum).

NO.		MIN	MAX	UNIT
79	Setup time, FPA in the high-impedance state after MBCLK1 rising edge, bus resume	$2t_M - 13$		ns
80	Delay time, MBCLK1 falling edge to FPA valid, bus resume		$2t_M + 9$	ns

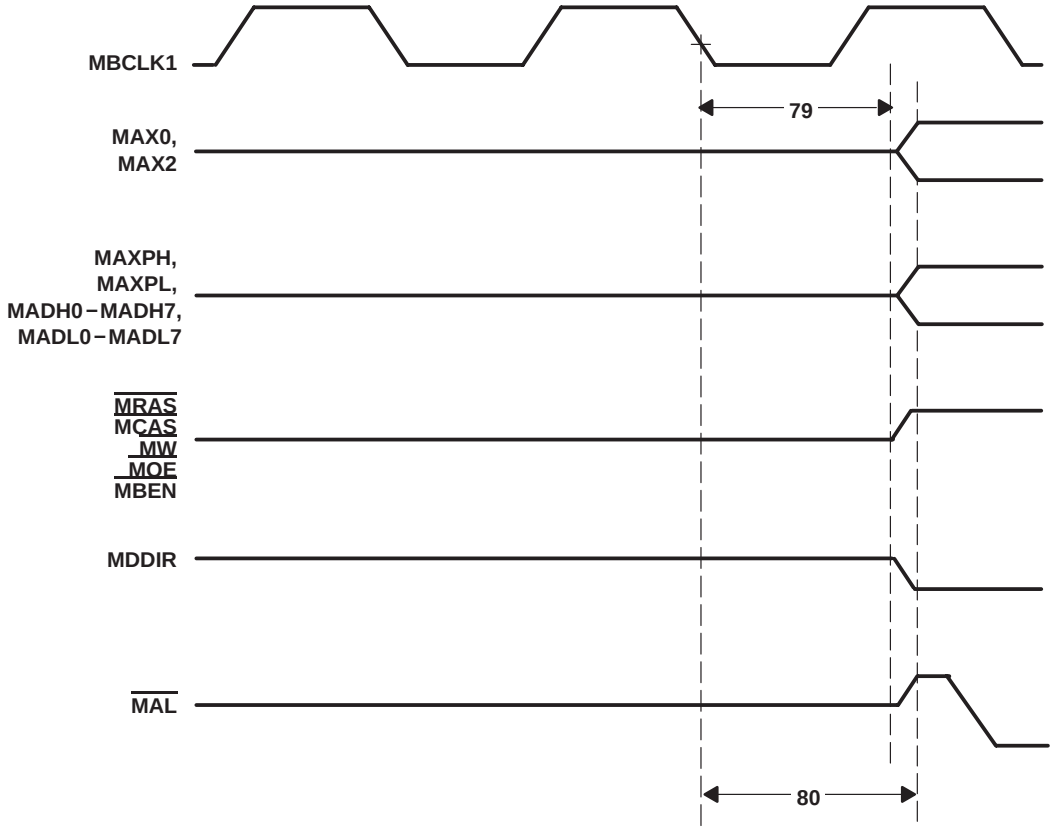

Figure 13. FPA-Bus Arbitration: FPA Takes Control of Bus

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FPA-bus arbitration: FPA releases control of bus

t_M is the cycle time of one-eighth of a local-memory cycle (20.83 ns minimum).

NO.		MIN	MAX	UNIT
74	Hold time, FPA after MBCLK1 falling edge, bus release	$2.5t_M - 13$		ns
74a	Hold time, $\overline{\text{MBEN}}$ valid after MBCLK1 falling edge, bus release	$3t_M - 13$		ns
75	Delay time, MBCLK1 falling edge to FPA in the high-impedance state, bus release		$2.5t_M$	ns
75a	Delay time, MBCLK1 falling edge to $\overline{\text{MBEN}}$ in the high-impedance state, bus release		$3t_M$	ns

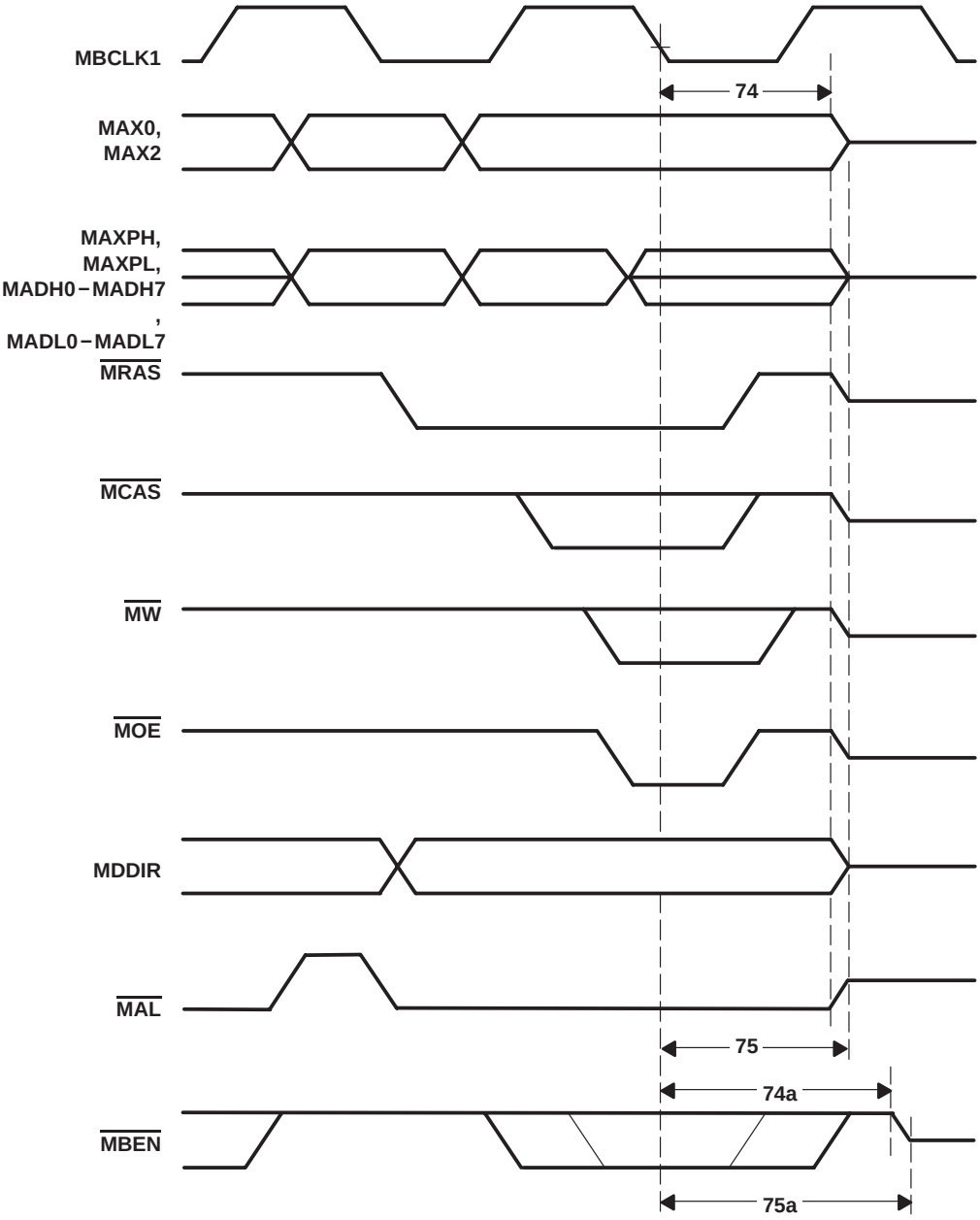

Figure 14. FPA-Bus Arbitration: FPA Releases Control of Bus

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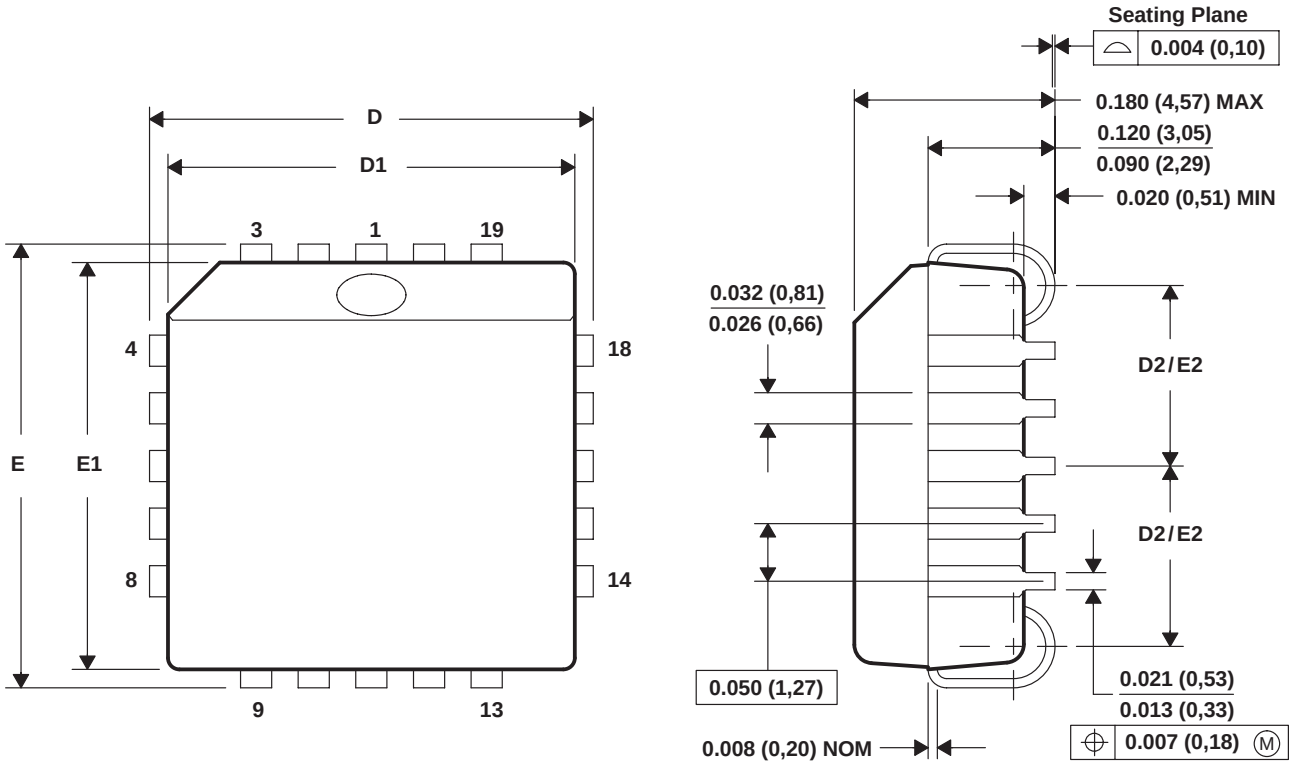
MECHANICAL DATA

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

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