PF051-05

SMM2364C

CMOS 64K-BIT MASK ROM

- ●**Low Supply Current**
- ●**Access Time 350ns/450ns**
- ●**8,192 Words×8 Bits Asynchronous**

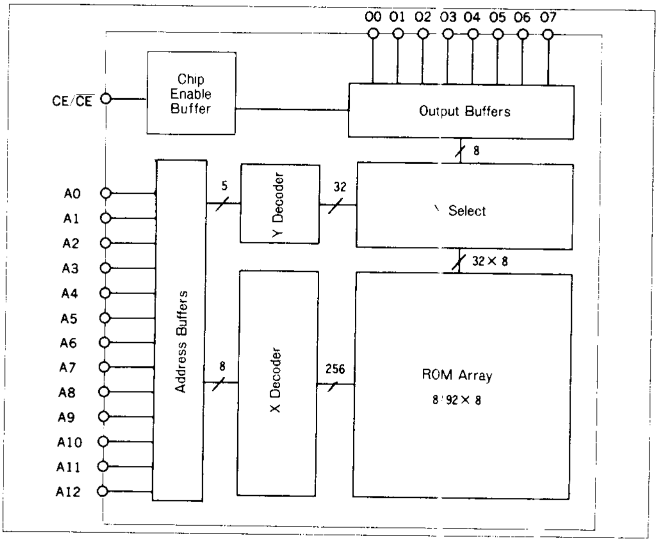
■DESCRIPTION

The SMM2364C is an 8,192 words × 8 bits asynchronous, static, mask programmable ROM on a monolithic CMOS chip and is characterized by fast access time and very low power dissipation. The nature "static" of the memory eliminates the need of an external clock. Both the input and output are TTL compatible. The 3-state output and mask programmable chip enable provide easy system design and easy expansion of the memory capacity. These features make the SMM2364C usable for wide-ranged applications, especially as a memory for low power dissipation devices using microprocessors.

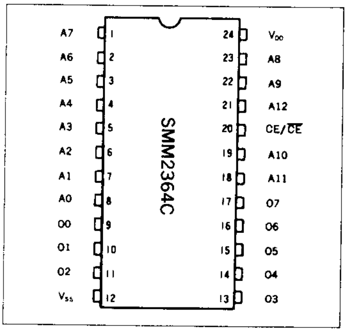
■FEATURES

- ●Access time·································350/450ns
- ●Low supply current·····························standby : 0.1 μA (Typ)
  operation: 15mA/12mA (Typ)
- ●Completely static
- ●Single power supply·····························5V ±10%
- ●TTL compatible inputs and outputs
- ●3-state output with wired-OR capability
- ●Package···24-pin DIP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

A0 to A12	Address Inputs
CE/$\overline{CE}$	Chip Enable
O0 to O7	Data Outputs
V_{DD}	Power Supply (+5V)
V_{SS}	Power Supply (0V)

ABSOULTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to 7.0	V
Input voltage	V_I	−0.3 to V_{DD}+0.3	V
Output voltage	V_O	−0.3 to V_{DD}+0.3	V
Power dissipation	P_D	1.0	W
DC output current	I_O	10	mA
Operating temperature	T_{opr}	−65 to 150	°C
Storage temperature	T_{stg}	−10 to 70	°C
Soldering temperature and time	T_{sol}	260°C, 10 s (at lead)	—

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD}= +5V±10%, V_{SS}=0V, Ta=−10 to +70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}		2.2	—	V_{DD}+0.3	V
Low level input voltage	V_{IL}		−0.3	—	0.8	V
Input leakage current	I_{LI}	$0 \leqq V_I \leqq V_{DD}$	−1.0	—	1.0	μA
Standby supply current	I_{DDS}	CE=V_{SS}+0.2 or $\overline{CE}$=V_{DD}−0.2	—	—	40	μA
Operating supply current	I_{DDO}	with output open	—	15*/12	40*/30	mA
Output leakage current	I_{LO}	$0 \leqq V_O \leqq V_{DD}$	−1.0	—	1.0	μA
High level output voltage	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	V
Low level output voltage	V_{OL}	I_{OL}=2.0mA	—	—	0.4	V
Input capacitance	C_I	f=1 MHz	—	—	7	pF
Output capacitance	C_O	f=1 MHz	—	—	10	pF

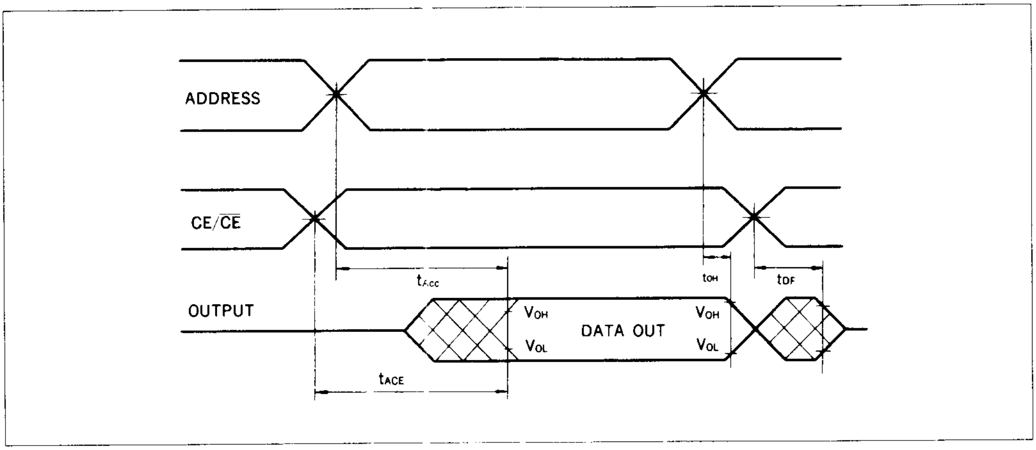
*at access time 350ns

AC Characteristics

(V_{DD}= +5V±10%, V_{SS}=0V, Ta=−10 to +70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address access time	t_{ACC}	C_L= 1TTL+100pF V_{IH}=2.2V, V_{IL}=0.8V V_{OH}=2.2V, V_{OL}=0.8V tr=tf=10ns	—	—	350/450	ns
$\overline{CE}$ access time	t_{ACE}		—	—	350/450	ns
Output floating	t_{DF}		-	—	150	ns
Output hold time	t_{OH}		0	—	—	ns

Timing Chart



■ FUNCTIONS

●Truth Table

CE	$\overline{CE}$	A0 to A12	O0 to O7	MODE
L	H	X	Hi-Z	Standby
H	L	Stable	Output data	Read

(X : H or L)

●Read mode

Data can be read by simply setting an address with CE held at "H" or $\overline{CE}$ at "L".

●Stanby mode

Setting CE at "L" or $\overline{CE}$ at "H" initiates the standby mode. In this mode, the output impedance goes high and all address inputs are disabled. Within the chip, no circuit allows current folw and only the leakage current exists.

●Specifying CE/$\overline{CE}$

CE/$\overline{CE}$ is mask programmable and may be selected for either active level. When ordering, specify the active level of CE/$\overline{CE}$.

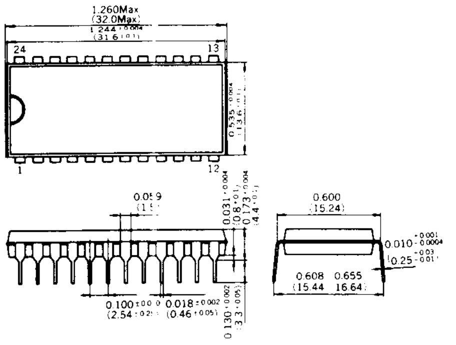
[NOTE] RECOMMENDATIONS

1. The SMM2364C is a mask programmable ROM on a CMOS chip. In the data read mode, transient current will frow in the chip at the time of transistor transition. For protection of such transients, it is recommended to connect a high-frequency capacitor and an electrolytic capacitor between the power supplies V_{DD} and V_{SS}.
2. The input and output of the SMM2364C are TTL compatible. It is recommended that, when the chip is connected to TTL, pull-up resistors be connected to the CE/CE and address input terminal.

■ PACKAGE DIMENSIONS

C24

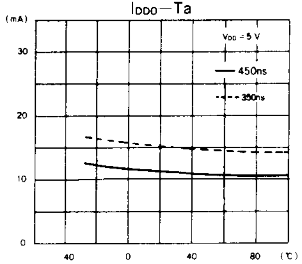
24-pin DIP



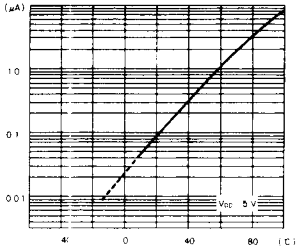
unit : inch
(mm)

■CHARACTERISTICS CURVES

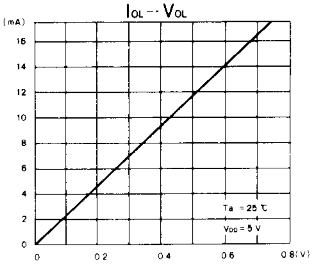
I_{DDO}—Ta



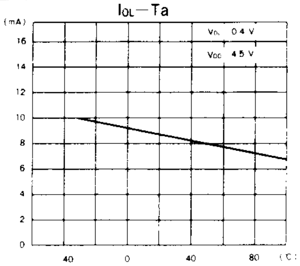
I_{DDS} Ta



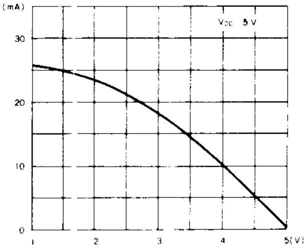
I_{OL}—V_{OL}



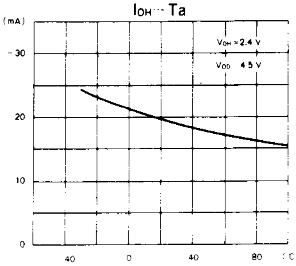
I_{OL}—Ta



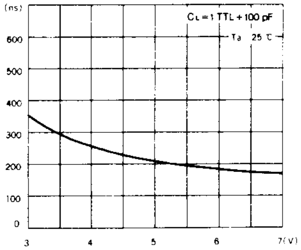
I_{OH}—V_{OH}



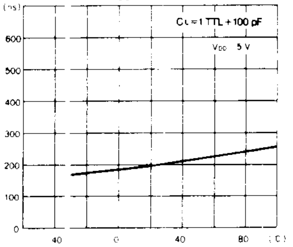
I_{OH}—Ta



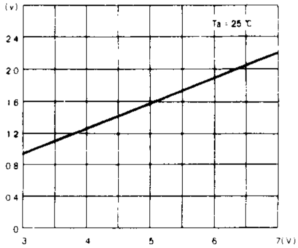
t_{ACC}—V_{DD}



t_{ACC}—Ta



V_{IH}—V_{DD}



V_{IL}—V_{DD}