D2804, MARCH 1984—REVISED SEPTEMBER 1987

- Carry-Out Output for Cascading
- Divide-by-N Counting
- DC Clock Input Circuit Allows Slow Rise Times
- Power-Up Reset
- Pin-Out Compatible with 'HC4022
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

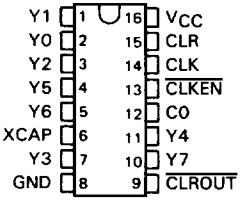
The 'HC7022 is a four-stage divide-by-8 Johnson counter with eight decoder outputs and a carry-out bit. High-speed operation and spike-free outputs are obtained by use of the Johnson octal counter configuration.

The eight decoder outputs are normally low and go high only at their respective octal time periods. A high signal on CLR asynchronously clears the octal counter and sets the carry output and Y0 high. With $\overline{\text{CLKEN}}$ low, the count is advanced on a low-to-high transition at CLK. Alternatively, if CLK is high, the count is advanced on a high-to-low transition at $\overline{\text{CLKEN}}$. Each decoded output remains high for one full clock cycle. The carry output C0 is high while Y0, Y1, Y2, or Y3 is high, then is low while Y4, Y5, Y6, or Y7 is high.

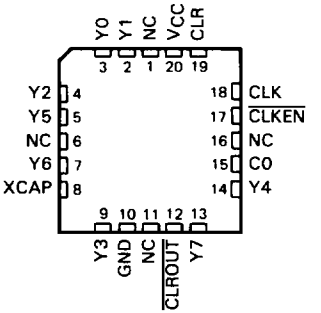
This part is similar to the 'HC4022; the main difference is that it includes a power-up-clear circuit to reset the counter during the power-up of the device. The active-low open-drain clear output, $\overline{\text{CLROUT}}$, can be used to clear or rest external circuitry. The pulse duration of the power-up reset circuit can be controlled with an external capacitor C_{ext} connected to pin XCAP. If XCAP is connected to V_{CC}, the power-up reset function is bypassed.

The SN54HC7022 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC7022 is characterized for operation from −40°C to 85°C.

SN54HC7022 . . . J PACKAGE
SN74HC7022 . . . DW OR N PACKAGE
(TOP VIEW)

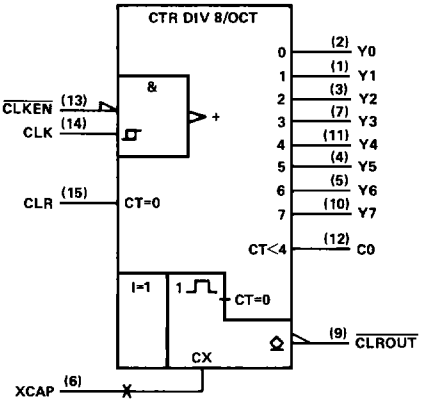


SN54HC7022 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

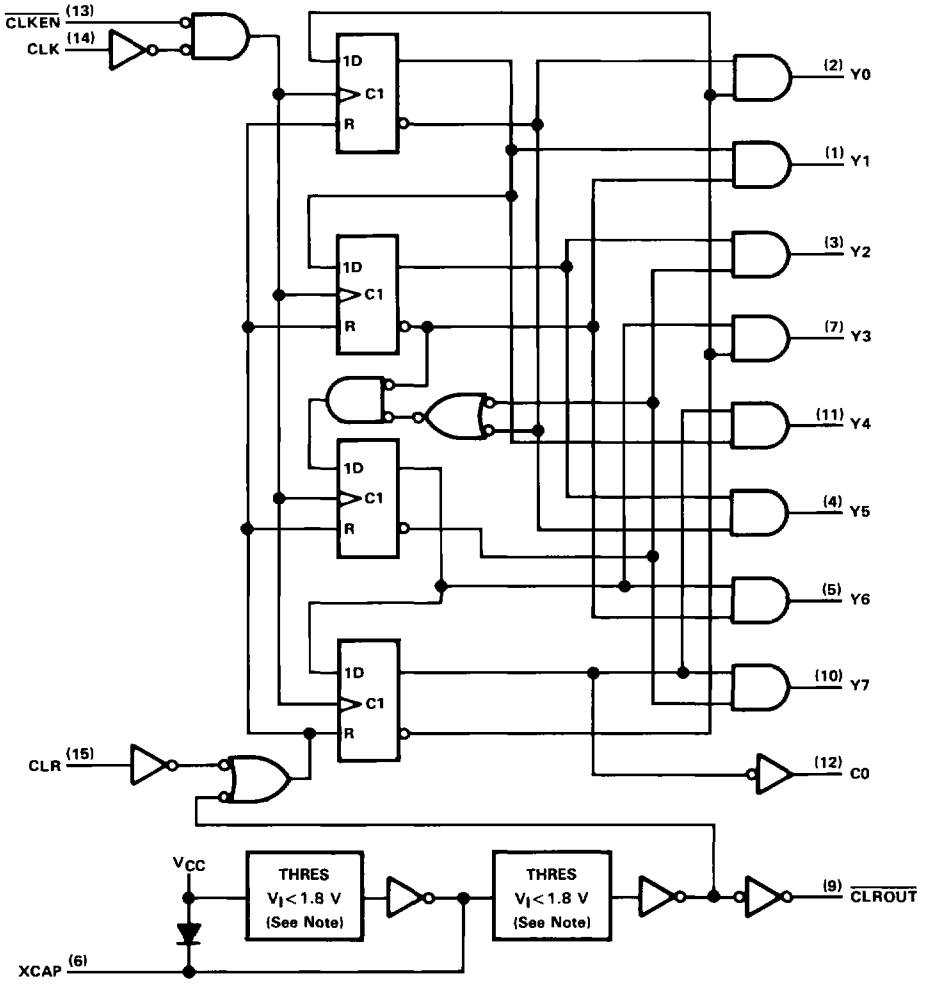
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

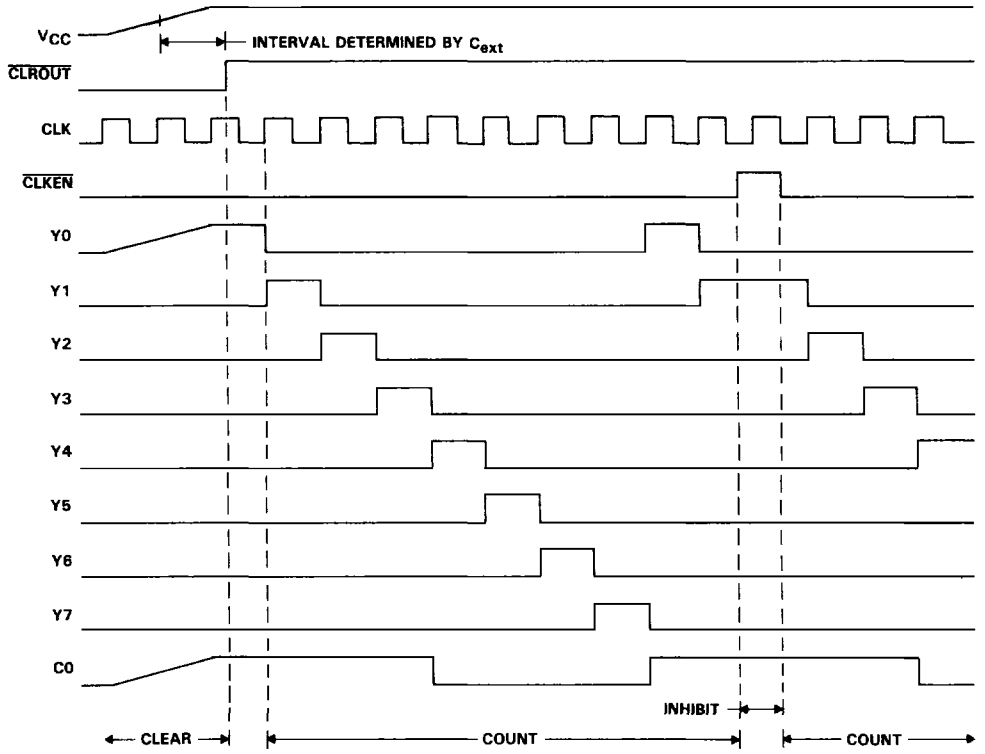
Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



Note: The output of each threshold detector is logically high until the input voltage exceeds the threshold level, typically 1.7 volts.
Pin numbers shown are for DW, J, and N packages.

typical power-up clear, count, and inhibit sequences



absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND pins . . . . . ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or N package . . . . . 260°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC7022			SN74HC7022			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC7022		SN74HC7022		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH} (Totem-pole outputs)	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
I_{OH} (Open-drain outputs)	V_I = V_{IH} or V_{IL}, V_O = V_{CC}	6 V		0.01	0.5		10		5	μA
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC7022		SN74HC7022		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	CLK↑ or $\overline{CLKEN}$‡	2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	CLK high or low† or $\overline{CLKEN}$ high or low‡	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
		CLR high	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time	$\overline{CLKEN}$ low before CLK↑† or CLK high before $\overline{CLKEN}$↓‡	2 V	50		75		63		ns
			4.5 V	10		15		13		
			6V	9		13		11		
		CLR inactive before CLK↑‡$\overline{CLKEN}$↓‡	2 V	50		75		63		
			4.5 V	10		15		13		
			6 V	9		13		11		
t_h	Hold time	$\overline{CLKEN}$ low after CLK↑† or CLK high after $\overline{CLKEN}$↓‡	2 V	5		5		5		ns
			4.5 V	5		5		5		
			6V	5		5		5		

†These conditions apply if clocking is being performed via the CLK input.
‡These conditions apply if clocking is being performed via the $\overline{CLKEN}$ input.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC7022		SN74HC7022		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{max}			2 V	6	10		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	55		25		29		
t_{pd}	CLK	Any Y or CO	2 V		115	230		343		290	ns
			4.5 V		23	46		69		58	
			6 V		20	39		58		49	
t_{pd}	$\overline{CLKEN}$	Any Y or CO	2 V		125	250		373		315	ns
			4.5 V		25	50		75		63	
			6 V		21	43		63		54	
t_{pd}	CLR	Any Y	2 V		115	230		343		290	ns
			4.5 V		23	46		69		58	
			6 V		20	39		58		49	
t_{PLH}	CLR	CO	2 V		115	230		343		290	ns
			4.5 V		23	46		69		58	
			6 V		20	39		58		49	
t_t		Any output	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	60 pF typ

Note 1: Load circuits and voltage waveforms are shown in Section 1.