BIPOLAR HIGH-SPEED 6-BIT FLASH A/D CONVERTER

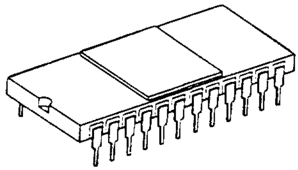
DESCRIPTION

The TS 8366 is a monolithic bipolar 6-bit parallel flash analog-to-digital converter designed for applications requiring very high-speed conversion.

The TS 8366 uses 64 parallel comparators to digitize fast moving analog input signals without external sample-and-hold circuits or input buffers. An overflow bit can be used.

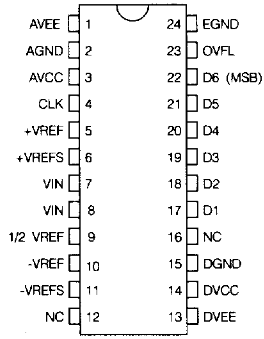
With encode rates up to 350 MHz, the TS 8366 is specified to operate from commercial to military temperature range with an analog input frequency of 100 MHz, making it ideal for a variety of applications and environments.

The TS 8366 is packaged in hermetic ceramic 24-pin DIL configuration and also available in die form.



C
DIL 24
(Ceramic package)

PIN CONNECTIONS
(Top view)
DIL CERAMIC - 24 PINS



Note : For details see «Pin Description»

MAIN FEATURES

- 6-bit resolution.
- Up to 350 MHz sampling rate.
- 5.6 effective bits at F_S = 200 MHz and F_{in} = 100 MHz.
- Low power : 0.9 W.
- Dual power supply : 5 V and − 5.2 V.
- − 55°C / + 125°C specified.
- Guaranteed monotonicity.
- High slew rate of input stages.
- Compatible with ECL 10 K.
- Overflow bit.
- No sample & hold required.

APPLICATIONS

- Military systems.
- Radar pulse analysis.
- Electronic countermeasures.
- Transient recorders.
- Smart munitions.
- Communication/signal intelligence.

THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES

ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Positive supply voltages (Note 2)	AV_{CC}, DV_{CC}	+ 4 to + 6	V
Negative supply voltages (Note 2)	AV_{EE}, DV_{EE}	− 6.2 to − 4.2	V
Upper reference voltage	$+V_{REF}$, $+V_{REFS}$	+ 0.3	V
Mid point reference current	I (1/2 V_{REF})	15	mA
Lower reference voltage	$-V_{REF}$, $-V_{REFS}$	− 3	V
Reference voltage range	$+V_{REF}$ to $-V_{REF}$	3.2	V
Analog input (Note 2)	V_{IN}	− 3 to + 0.3	V
Digital input voltage (Note 2)	CLK	V_{EE} to + 0.3	V
Digital output currents	I_D	30	mA
Junction temperature	T_j	175	°C
Storage temperature	T_{stg}	− 65 to + 150	°C
Operating temperature range	T_{case}	− 55 to + 125	°C
Lead temperature (soldering 10 s)	T_{leads}	+ 260	°C
Maximum difference between negative supply	AV_{EE} to DV_{EE}	± 0.5	V

Note 1 : Absolute maximum ratings are limiting values applied individually while other parameters are within specified operating conditions.
Long exposure to maximum rating may affect device reliability.
Note 2 : With respect to AGND = DGND = EGND.

USER WARNING

The power supplies must be applied before all the other signals to prevent damage from occuring on the device.

To prevent reliability problem and dynamic performance damage, high speed transition on power supply must be avoided.

SPECIFICATIONS

Electrical operating characteristics

$AV_{CC} = DV_{CC} = +5\ V$; $AV_{EE} = DV_{EE} = -5.2\ V$; $R_L = 100\ \Omega$ to $-2\ V$; $T_C = 25°C$ (unless otherwise specified)

Parameter	T_{case}	Test level	Min.	Typ.	Max.	Unit
RESOLUTION				6		Bits
DIGITAL INPUTS AND OUTPUTS						
Logic compatibility				ECL 10 K		
Clock input						
• Logic «0» voltage	full	IV			−1.5	V
• Logic «1» voltage	full	IV	−1.1			V
Output data						
• Logic «0» voltage (Note 1)	full	II, D			−1.5	V
• Logic «1» voltage (Note 2)	full	II, D	−1.1			V
• Output delay (Note 3)		IV		2.5		ns
MAXIMUM CLOCK FREQUENCY		III	300	350		MHz
ANALOG INPUT						
Voltage range		V		V_{REF}		V
Input capacitance		IV		10		pF
Input resistance		V		12		kΩ
Analog bandwidth (Note 4)		V		300		MHz
REFERENCE INPUT						
Differential reference voltage		I, D		2	3	V
Reference ladder resistance		I, D	35	50	65	Ω
	full	II	25		75	Ω
POWER REQUIREMENTS						
Power supply						
• Positive supply		I, D	4.5	5	5.5	V
	full	II	4.5	5	5.5	V
• Negative supply		I, D	−5.7	−5.2	−4.7	V
	full	II	−5.7	−5.2	−4.7	V
Power dissipation (Note 5)						
• Positive supply		I, D		600	750	mW
• Negative supply		I, D		300	400	mW
THERMAL RESISTANCE		V				
Junction-to-ambient (still air)				45		°C/W
Junction-to-case				5		°C/W
ACCURACY (Note 6)						
Integral nonlinearity		I, D		0.15	0.3	LSB
	full	II			0.5	LSB
Differential nonlinearity		I, D		0.15	0.3	LSB
	full	II			0.5	LSB
Monotonicity and no missing codes	full	IV	Guaranteed over specified temperature range			

SPECIFICATIONS (Continued)

Electrical operating characteristics

$AV_{CC} = DV_{CC} = +5\,V$; $AV_{EE} = DV_{EE} = -5.2\,V$; $R_L = 100\,\Omega$ to $-2\,V$; $T_C = 25°C$ (unless otherwise specified)

Parameter	Test level	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS (Note 7)					
Signal to noise ratio					
F_S = 300 MHz F_{in} = 1 MHz	III	36.6	37.2		dB
F_S = 200 MHz F_{in} = 99 MHz	III	34.3	35.5		dB
F_S = 10 MHz F_{in} = 1.5 MHz	D	35.5	36.4		dB
Total harmonic distorsion					
F_S = 300 MHz F_{in} = 1 MHz	III	45	56		dB
F_S = 200 MHz F_{in} = 99 MHz	III	40	44		dB
F_S = 10 MHz F_{in} = 1.5 MHz	D	45	51		dB
Number of effective bits					
F_S = 300 MHz F_{in} = 1 MHz	III	5.8	5.9		Bits
F_S = 200 MHz F_{in} = 99 MHz	III	5.4	5.6		Bits
F_S = 10 MHz F_{in} = 1.5 MHz	D	5.6	5.75		Bits
Aperture uncertainty	V		25		pS

Note 1 : With I_{OUT} = 2 mA.
Note 2 : With I_{OUT} = 12 mA.
Note 3 : See timing diagram.
Note 4 : The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.
Note 5 : F_S = 10 MHz - F_{in} = 1.5 MHz.
Note 6 : Histogram based on sampling of 1.5 MHz sinusoïdal analog signal with and encode rate of 10 MHz.
Note 7 : Dynamic measurements are performed with an analog input signal 1 dB below full scale.

EXPLANATION OF TEST LEVELS

Test level	
I	100 % production tested.
II	100 % production tested at + 25°C, and sample tested at specified temperature
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
D	100 % probe tested on wafer at T_{amb} = 25°C.

TIMING DIAGRAM

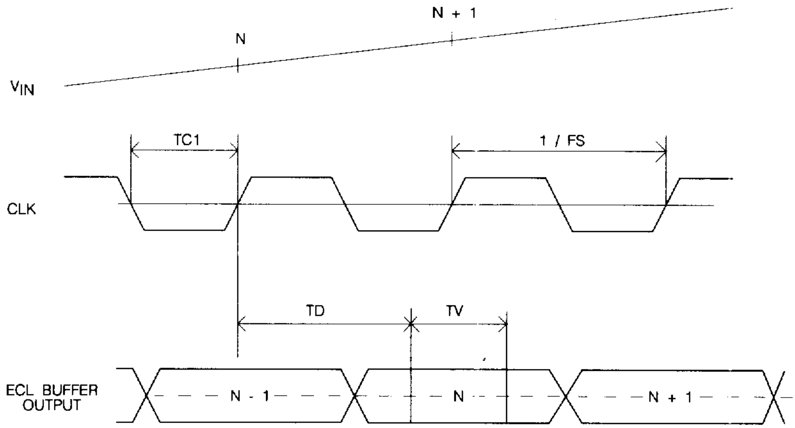


Figure 1

SWITCHING PERFORMANCES (Notes 1 and 2)

Parameter	Symbol	Typ.	Unit
Minimum clock period	1/FS	3	ns
Minimum time for comparison	TC1	1.5	ns
Output delay between CLK and outputs (Note 3)	TD	4	ns
Minimum output validity time (Note 3)	TV	1.5	ns

Note 1 : See definitions of terms.
Note 2 : $AV_{EE} = DV_{EE} = -5.2\ V$; $AV_{CC} = DV_{CC} = +5\ V$; $+V_{REF} = +0\ V$; $-V_{REF} = -2\ V$.
Note 3 : Outputs terminated through 100 Ω to −2 V. $C_{load} < 10\ pF$, clock command rise/fall time should be less than 2 ns in normal operating.

FUNCTIONAL BLOCK DIAGRAM

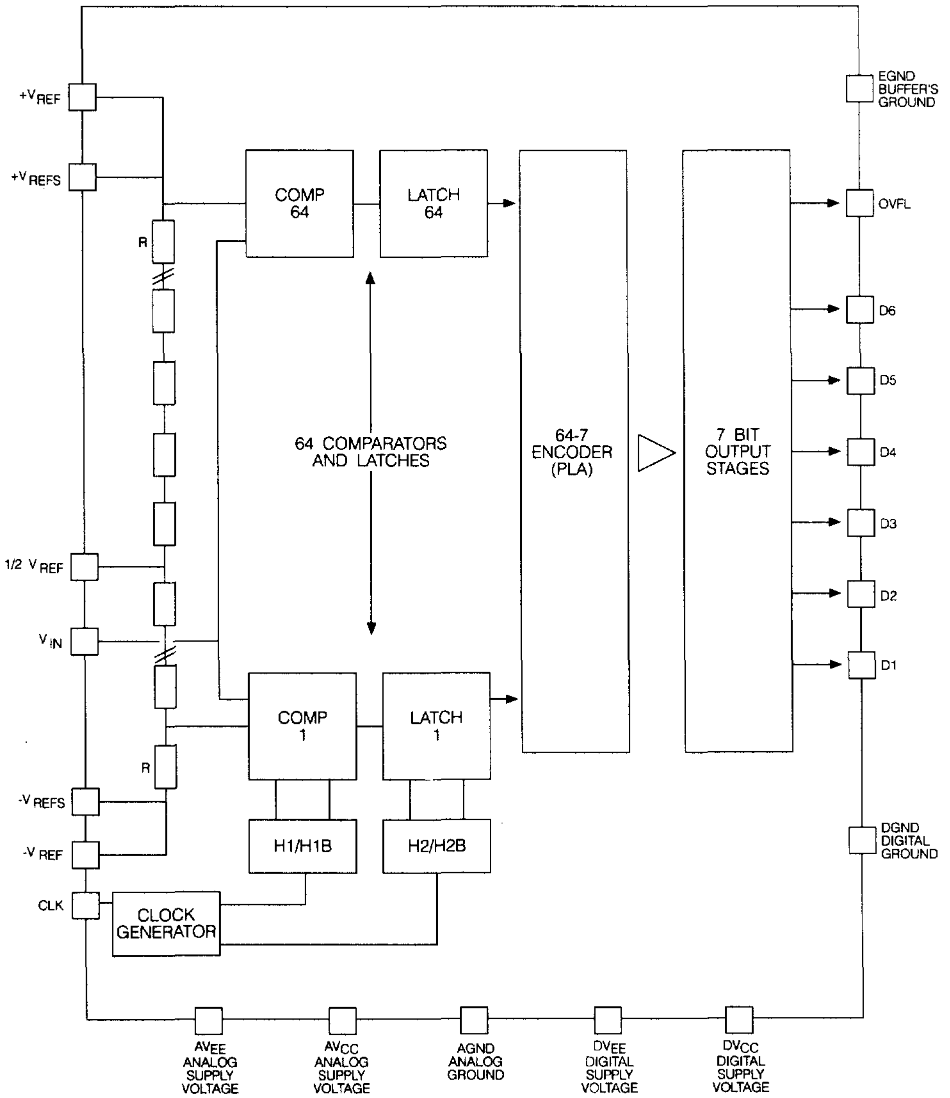


Figure 2

PIN DESCRIPTION

Pin DIL	Symbol	Function	Description
1	AV_{EE}	Negative analog supply	
2	AGND	Analog ground	
3	AV_{CC}	Positive analog supply	
4	CLK	Clock input	ECL 10 K level compatibility
5	$+V_{REF}$	Positive reference voltage input	
6	$+V_{REFS}$	Positive reference voltage sense	
7	V_{IN}	Analog input	
8	V_{IN}	Analog input	
9	$1/2\ V_{REF}$	Reference midpoint	Access to the midpoint tap on the resistance ladder
10	$-V_{REF}$	Negative reference voltage input	
11	$-V_{REFS}$	Negative reference voltage sense	
12	NC	Not internally connected	
13	DV_{EE}	Negative digital supply	
14	DV_{CC}	Positive digital supply	
15	DGND	Digital ground	
16	NC	Not internally connected	
17	D1	Digital data output (LSB)	ECL 10 K level compatibility (pins 17–23)
18	D2	Digital data output	
19	D3	Digital data output	
20	D4	Digital data output	
21	D5	Digital data output	
22	D6	Digital data output (MSB)	
23	OVFL	Overflow data output	
24	EGND	Digital output ground	

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THEORY OF OPERATION

The block diagram (see page 6) shows a conventional flash converter structure. This architecture enables very high-speed operation, without external sample and hold.

The analog input signal is fed to all comparators, and is compared to a set of 64 reference levels (6 bits + overflow), derived from a resistor ladder network. Midpoint tap (1/2 V_{REF}) of the reference ladder is provided for linearity adjustment or transfer function modification.

A set of 64 AND latches following the comparator array indicates the appropriate quantization level of the analog input signal. An encoder stage provides output data in binary code, followed by high speed ECL buffers.

APPLICATIONS

User warning

The power supplies must be applied before all the other signals to prevent damage from occuring on the device.

Functional description

The TS 8366 operates with analog input signals varying between ± V_{REF} reference voltages, (Nominally $+V_{REF}$ = 0 V, $-V_{REF}$ = − 2 V), applied across an internal resistor ladder.

Maximum differential Reference voltage is 3 V, so external reference generator circuit must limit the voltage to this value to avoid permanent damage caused to the TS 8366 by excessive current densities.
The offset errors caused by input (± V_{REF}) access resistances, can be cancelled using voltage sense lines (± V_{REFS} pins). (Maximum sense current : < 1mA).

The typical input capacitance of the TS 8366 is 10 pF, which can be driven directly by most 50 Ω signal sources.

Full logic ECL input clock signals are recommended for the TS 8366, with fast rise and fall times (500 ps), especially when digitizing high frequency input waveforms.
Although the TS 8366 is designed and tested to operate with a 50% clock cycle, dynamic performance at high data rates can be improved by changing the clock duty cycle.

Output data is ECL 10K logic compatible.
The overflow bit (OVFL) turns to ECL logic 1 when input signal exceeds $+V_{REFS}$ sense voltage, and output data (D1 to D6) is set to ECL logic 0.

Timing

Output Data changes on rising edge of clock signal, (CLK1), (Comparators in latch mode), after output propagation delay TD (Typ = 4 ns). Output Data should be latched on falling edge of Clock signal (CLK1), after tracking of output propagation delay, by an external delayed clock signal.

Packaging

The TS 8366 is mounted in ceramic 24-pins DIL package.
Sockets may be used for prototype evaluation, but should be avoided afterwards, because it leads to limitations of TS 8366 dynamic performance, and increased decoupling difficulties.

TYPICAL EVALUATION CIRCUIT (see page 9)

Designs involving the TS 8366 must follow a few precautions to ensure optimum performance. The following design suggestions are essentially meant to avoid many of the high speed design problems.

Multilayer printed circuit board is recommended, because it enables compact implementation and allows easy design of low impedance continuous Supply and Ground planes.
All ground pins should be connected to the ground plane as close to the package as possible.
Proper supply decoupling by high resonant frequency chip capacitors close to the device, and high quality tantalum capacitor at each power supply incoming, is especially recommended.

The length of digital input/output signal paths should be matched and kept short, to avoid propagation delay mismatches, increased output bits time skew, and over or undershoot caused by reflections.

So long as propagation delay along the line is shorter than digital signal rise or fall time, the reflection has little effect on the waveform.
However, if long interconnection lengths cannot be avoided, proper design of transmission line impedance with adapted ECL termination loads has to be observed.
Chip resistors (100 Ω to − 2V) are recommended for ECL pulldown output terminations.

50 Ω impedance microstrip line with 50 Ω termination chip resistors should be used to drive analog and clock input pins. (Pins 7, 8 and 8)

High-speed ECL quad latches should be used to extend the validity time of the digital outputs and simplify their acquisition.

TYPICAL EVALUATION CIRCUIT

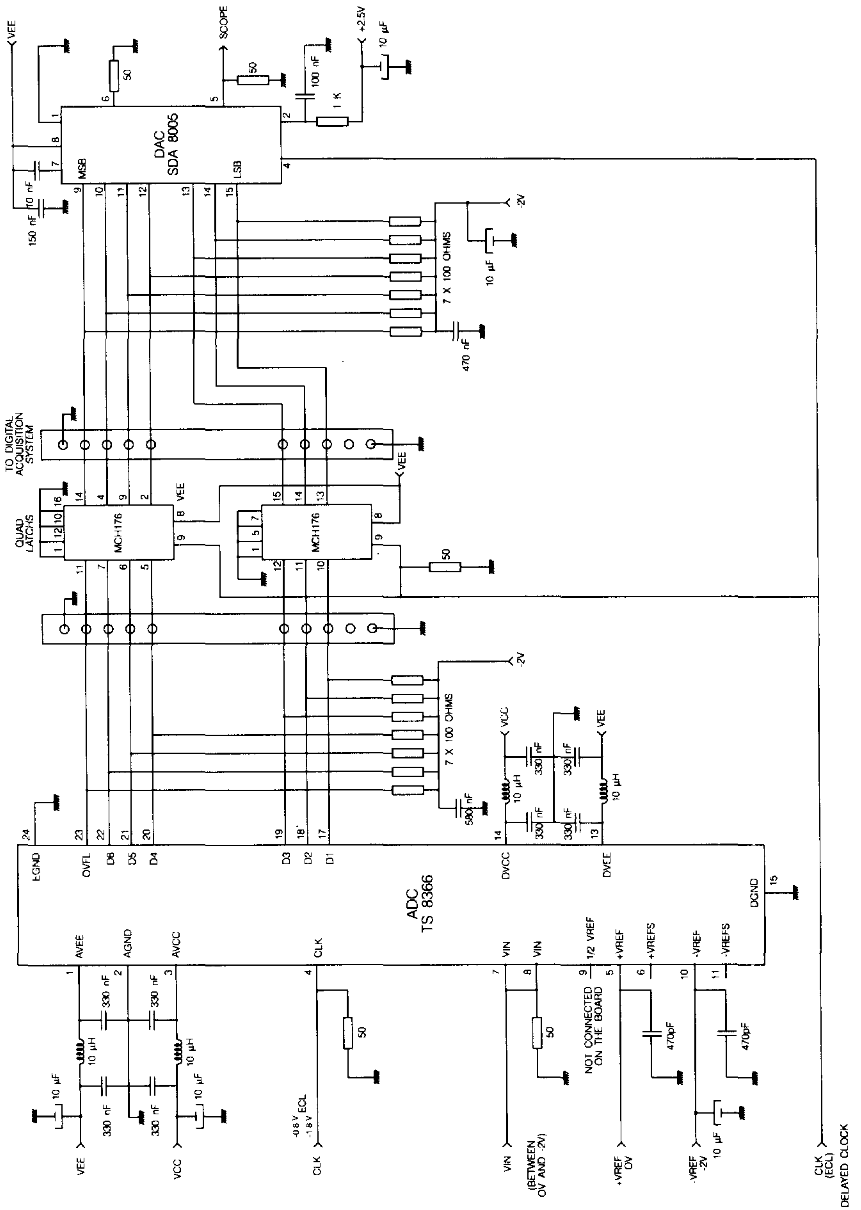


Figure 3

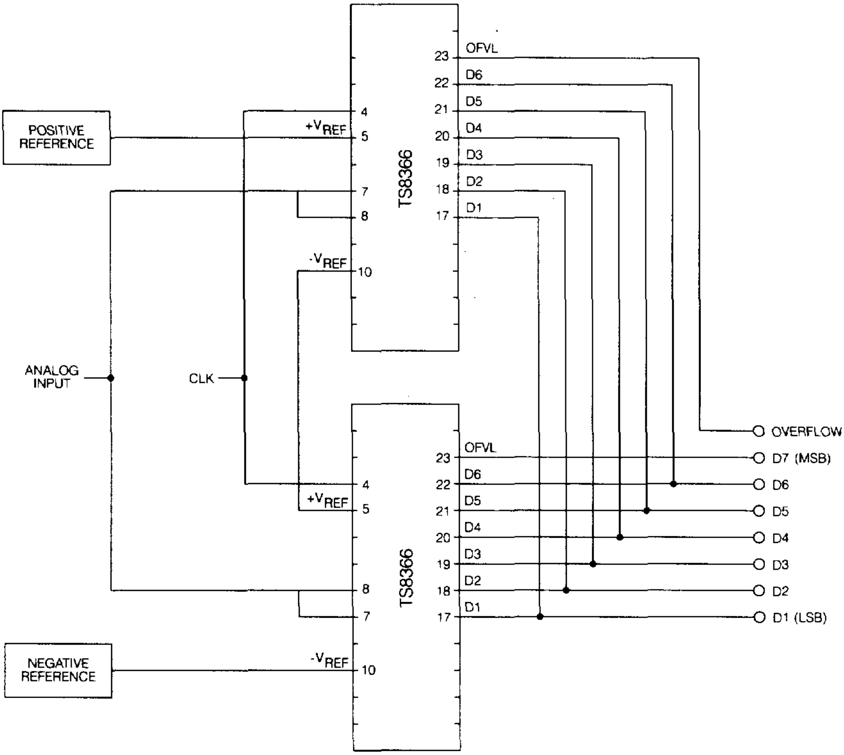


Figure 4 : Connections for 7 bit operation.

TYPICAL CURVES

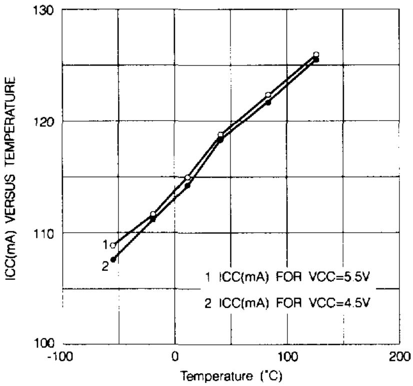


Figure 5 : I_{CC} vs. temperature.

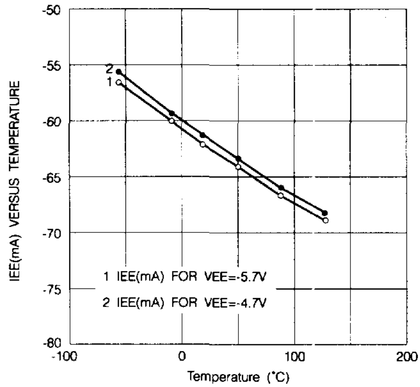


Figure 6 : I_{EE} vs. temperature.

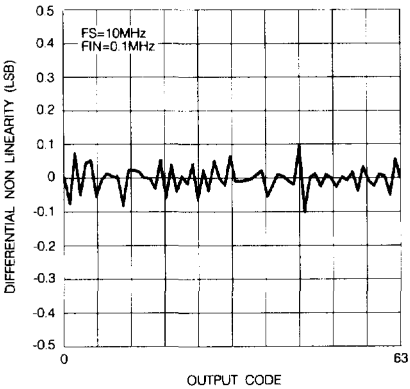


Figure 7 : Differential nonlinearity vs. output code.

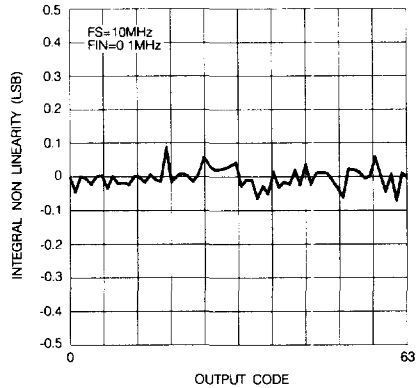


Figure 8 : Integral non linearity vs. output code.

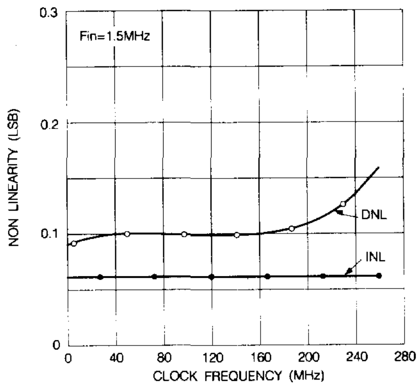


Figure 9 : INL and DNL vs. clock frequency.

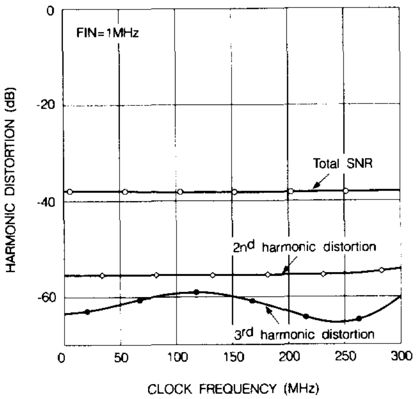


Figure 10 : Distortion vs. sampling rate 2nd and 3rd harmonics.

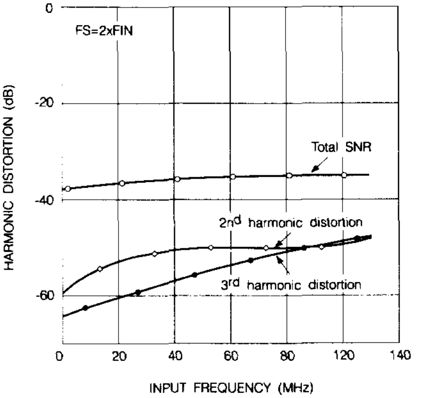


Figure 11 : Distortion vs. input 2nd and 3rd harmonics frequency.

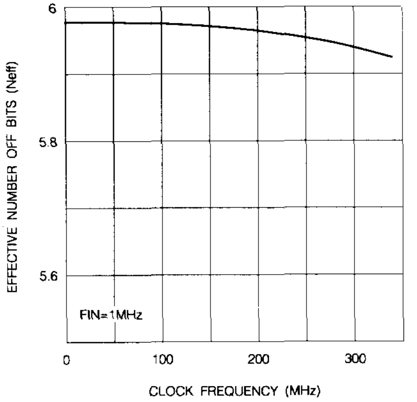


Figure 12 : Number of effective bits vs. sampling rate.

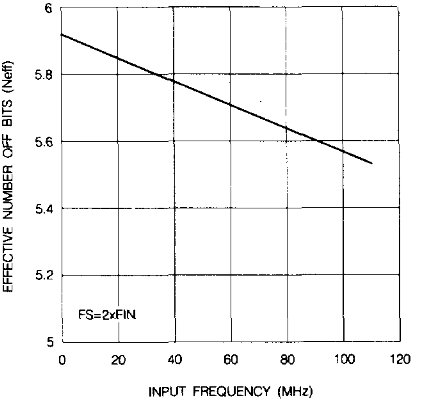


Figure 13 : Number of effective bits vs. input frequency.

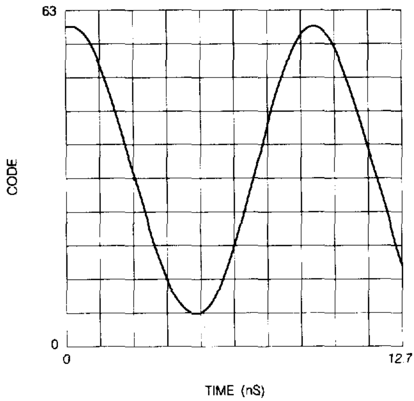


Figure 14 : Reconstructed waveform 220 MHz sampling rate 109.4 MHz input frequency.

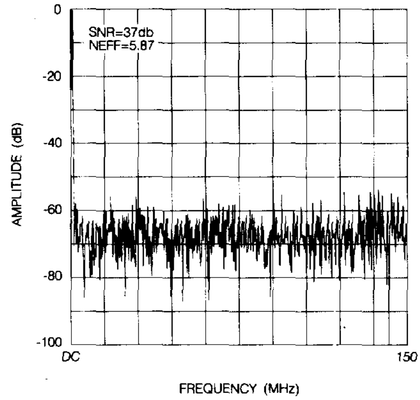


Figure 15 : 1024 point FFT of TS 8366 output at 300 MHz sampling rate, 1 MHz input frequency.

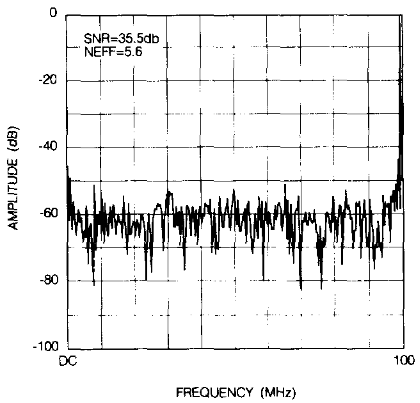


Figure 16 : 1024 point FFT of TS 8366 output at 200 MHz sampling rate, 99 MHz input frequency.

DEFINITION OF TERMS

Signal-to-noise ratio (SNR)
determined by FFT analysis,

$$SNR = 10.\log \left[\frac{P(F_{IN})}{P_n} \right] = 10.\log \left[\frac{A^2(F_{IN})}{\Sigma A^2(j)} \right]_{j \neq F_{in}}$$

with :
- $P(F_{IN})$ spectral power of the input frequency F_{IN},
- P_n noise power, which is defined as the sum of the powers of all spectral components, except F_{IN},
- A(j) amplitude of the spectral component of frequency j.

Total harmonic distorsion (THD)
determined by FFT analysis,

$$THD = 10.\log \left[\frac{P(F_{IN})}{P_{hn}} \right] = 10.\log \left[\frac{A^2(F_{IN})}{\Sigma A^2(k.F_{IN})} \right] \text{ with } k \geqslant 2$$

with : P_{hn} harmonic noise power, which is defined as the sum of the powers of all harmonics of F_{IN}.

Number of effective bits (N_{eff})
determined by FFT analysis,

$$N_{eff} = \frac{SNR - 1.76}{6.02}$$

Gain error (G_e)

$$G_e = \frac{G - G_O}{G_O}$$

with :
- G_O slope of theoretical straight line of the ADC transfer function.
- G slope of the real best-fit straight line.

Integral nonlinearity (INL)
Measured after trimming the offset and gain errors to zero.

The integral nonlinearity for an output code i, INL (i), is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition.

The ADC integral nonlinearity INL is the maximum value of all $|INL(i)|$.

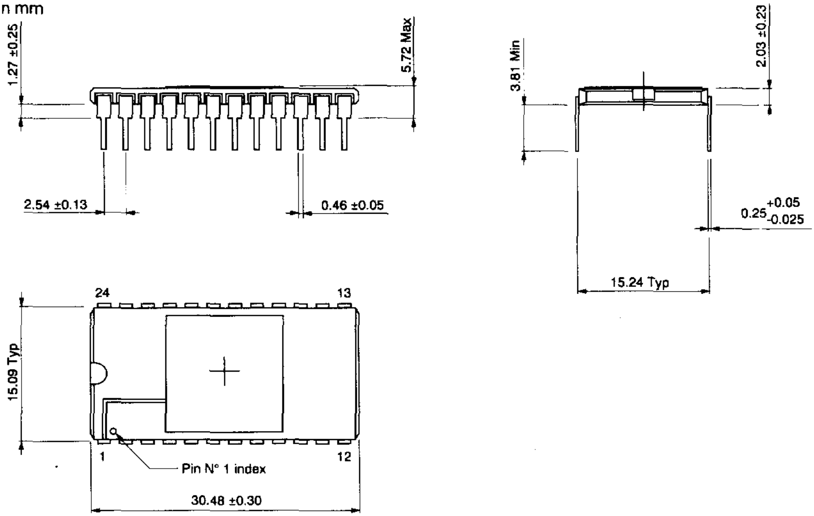
Differential nonlinearity (DNL)
Measured after trimming the offset and gain errors to zero.

The differential nonlinearity for an output code i, DNL(i), is the difference between the measured step size of code i and the ideal LSB step size.

The ADC differential nonlinearity DNL is the maximum value of all $|DNL(i)|$.

MECHANICAL PACKAGE DATA
DIL 24 - Ceramic Side Brazed package

Dimensions in mm



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DIE MECHANICAL INFORMATION : JTS 8366
Pad layout : V536

Pad size : 0.120 x 0.120 mm

Die size : 3.750 x 2.760 mm

Die thickness : 380 μm

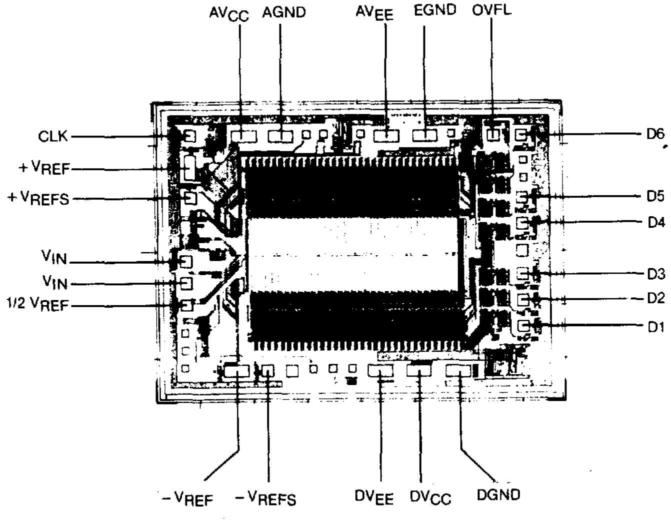
Metallization : Si (Back side)
Al-Si-Ti (Front side)

Passivation : Nitride

Revision : A

Qualification lot package : DIL 24

Back side potential : AV_{EE}



ORDERING INFORMATION

Packaged device

TS 8366 M C 8 B / C

- TS — TCS (1) prefix
- 8366 — Device or family
- M — Temperature range

Temperature range :
M : –55, +125°C
V : –40, +85°C
C : 0, +70°C

- C — Package

Package :
C : DIL ceramic - 24 pins

- 8 — Lead finish

Lead finish :
8 : Gold plated

- B / C — Quality level

Quality level :
- - : Standard
B/C : MIL-STD-883, class B

Die form

J TS 8366 – 1 V A

- J — Die prefix
- TS — TCS prefix (1)
- 8366 — Generic part number
- 1 — Back side metallization

Back side metallization
1 = Nacked Si

- V — Screening levels

Screening levels (2)
V : Visual inspection

- A — Revision of the mask set

Temperature range
– : Tamb = 25°C

Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.
Note 2 : For availability of the different available versions contact your TCS sales office.