EM 6621

NEW!
MFP Version EM6521
(Multiple Field Programmable)

4-Bit Microcontroller

Features

- Low Power - 3 µA active mode
  - 0.6 µA standby mode
  - 0.2 µA sleep mode
  @ 1.5V, 32kHz, 20°C
- Low Voltage - 1.2 to 3.6V
- 2 clocks per instruction cycle
- 72 basic instructions
- ROM 4k x 16 bit
- RAM 128 x 4 bit
- Max. 12 inputs (3 ports) port A, port B, port SP
- Max. 8 outputs (2 ports) port B, port SP
- Voltage level detector, 8 levels software selectable from 1.2 V up to 4.0 V
- Melody, 7 tones + silence inclusive 4-bit timer
- Universal 10-bit counter / PWM / event counter
- Prescaler down to 1 second (crystal = 32 kHz)
- 1/1000 s 12 bit binary coded decimal counter with hard or software start/stop function
- LCD 20 segments, 3 or 4 times multiplexed
- 3 wire serial port , 8 bit, master and slave mode
- 5 external interrupts (port A, serial interface)
- 8 internal interrupts (3 x prescaler, BCD counter 2x10-bit counter, melody timer, serial interface)
- Timer watchdog and oscillation supervisor

Description

The EM66XX series is an advanced single chip low cost CMOS 4-bit microcontroller. It contains ROM, RAM, LCD driver, power on reset, watchdog timer, oscillation detection circuit, 10-bit up/down and event counter, 1ms BCD counter, prescaler, voltage level detector (VLD), serial interface and several clock functions. The low voltage feature and low power consumption make it the most suitable controller for battery, stand alone and mobile equipment. The EM66XX series is manufactured using EM's Advanced Low-Power (ALP) CMOS Process.

Typical Applications

- Timing device
- Automotive controls with display
- Intelligent display driver
- Measurement equipment
- Domestic appliance
- Interactive system with display
- Timer / sports timing devices
- Bicycle computers
- Safety and security devices

Figure 1. Architecture

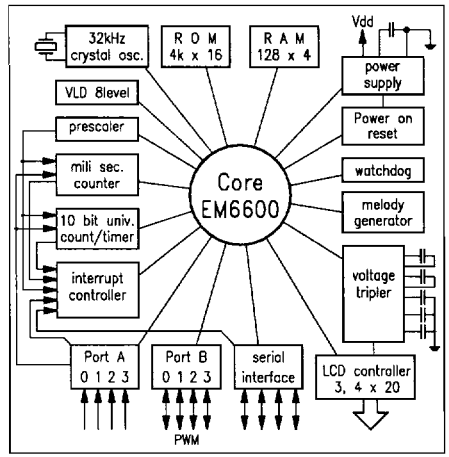
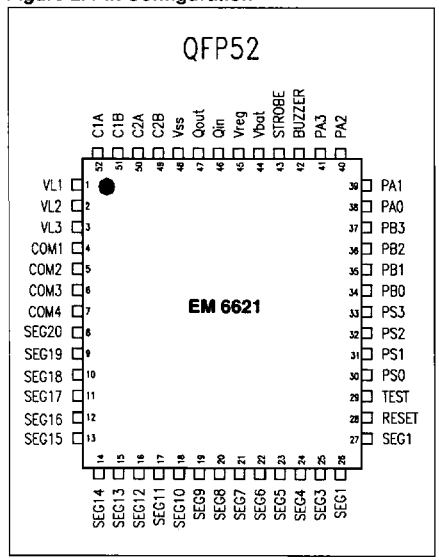


Figure 2. Pin Configuration



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EM6621 at a glance

• Power Supply
- Low-voltage low-power architecture including internal voltage regulator
- 1.2 ... 3.6 V battery voltage
- 2.1 µA in active mode (25 °C)
- 0.50 µA in standby mode (LCD off, 25 °C)
- 0.15 µA in sleep mode (25 °C)
- 32 kHz Oscillator

• RAM
- 64 x 4 bits, direct addressable
- 64 x 4 bits, indexed addressable

• ROM
- 4k x 16 bits, metal mask programmable

• CPU
- 4 bit RISC architecture
- 2 clock cycles per instruction
- 72 basic instructions

• Main Operating Modes and Resets
- Active mode (CPU is running)
- Standby mode (CPU in Halt)
- Sleep mode (no clock, reset state)
- Initial reset on power on (POR)
- Watchdog reset (logic and oscillation watchdogs)
- Reset terminal
- Reset with input combination on port A (register selectable)

• Prescaler
- 15 stage system clock divider down to 1 Hz
- 3 interrupt requests; 1 Hz, 32 Hz or 8 Hz, blink
- Prescaler reset (4 kHz to 1 Hz)

• Liquid Crystal Display Driver (LCD)
- 20 segments 3 or 4 times multiplexed
- Internal or external voltage tripler
- Free segment allocation architecture (metal 2 mask)
- LCD switch off for power save

• 8-Bit Serial Interface
- 3 wire (clock, data in, data out) master/slave mode
- READY output during data transfer
- Maximum shift clock is equal to the main system clock
- Interrupt request to the CPU after 8 bits data transfer
- Supports different formats (i.e. EEPROM ST93C46A)
- Can be configured as a parallel 4 bit input/output port
- Direct input read on the port terminals
- All outputs tristatable
- Selectable pull-downs in input mode
- CMOS or N-channel open drain outputs
- Weak pull-up selectable in N-Channel open drain mode

• 4-Bit Input Port A
- Direct input read on the port terminals
- Debounced or direct interrupt requests from each input
- Interrupt request on positive or negative edge
- Pull-up or pull-down or none selectable by register
- Test variables (software) for conditional jumps
- PA[0] and PA[3] are inputs for the event counter
- PA[3] is start/stop input for the milli-second counter
- Reset with input combination (register selectable)

• 4-Bit Bi-directional Port B
- All different functions bit wise selectable
- Direct input read on the port terminals
- Data output latches
- CMOS or N-channel open drain outputs
- Pull-down or pull-up selectable
- Weak pull-up in N-channel open drain mode
- Selectable PWM, 32 kHz, 1 kHz and 1 Hz output

• Melody Generator
- Dedicated buzzer terminal
- 7 tones plus silence output
- Output tristatable
- Internal 4-bit timer, usable also in standalone mode
- 4 different timer input clocks
- Timer with autoreload or single run
- Timer interrupt request on 0

• Voltage Level Detector
- 8 different levels from 1.2 to 4.0 V
- Busy flag during measure

• 10-Bit Universal Counter
- 10, 8, 6 or 4 bit up/down counting
- Parallel load
- Event counting (PA[0] or PA[3])
- 8 different input clocks
- Full 10 bit or limited (8, 6, 4 bit) compare function
- 2 interrupt requests (on compare and on 0)
- Hi-frequency input on PA[3] and PA[0]
- Pulse width modulation (PWM) output possible on PB[3]

• Milli-Second Counter
- 3 digits binary coded decimal counter (12 bits)
- PA[3] input signal pulse width and period measurement
- Internal 1000Hz clock generation
- Hardware or software controlled start stop mode
- Interrupt request on either 1/10 s or 1 s

• Interrupt Controller
- 5 external and 8 internal interrupt request sources
- Each interrupt request individually maskable
- Each interrupt flag individually resettable
- Automatic reset of each interrupt request register read
- General interrupt request to CPU can be disabled
- Automatic enabling of general interrupt request flag when going into HALT mode